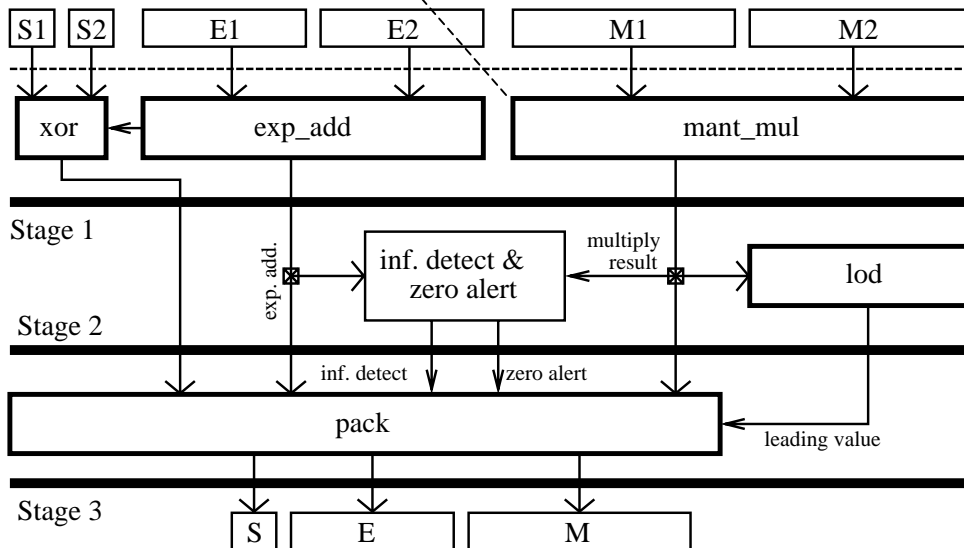
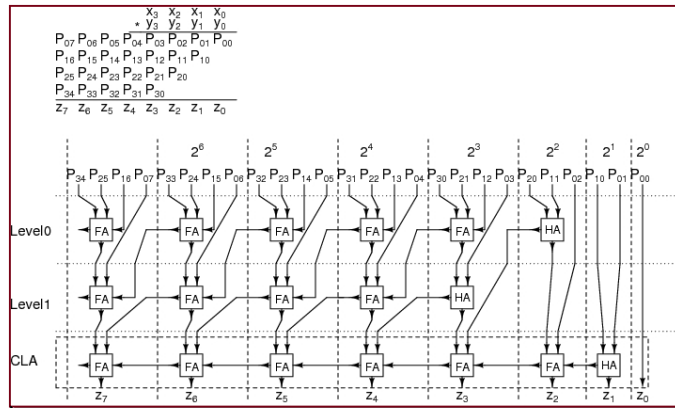


## Booth-encoded Wallace-Tree Multiplier



# Studien-, Bachelor-, Master-, Diplomarbeit



TECHNISCHE  
UNIVERSITÄT  
DARMSTADT



LOEWE – Landes-Offensive zur Entwicklung  
Wissenschaftlich-ökonomischer Exzellenz

### Topic

Design and Implementation of Wallace-Tree Multiplier.

### Description

A 32-bit Wallace-Tree Digital Multiplier will be designed and simulated by using VHDL or Verilog HDL. The Multiplier is one of important components that will be used to implement a high-performance pipeline floating-point (FP) multiplier. The critical path of the FP multiplier is located in the multiplication stage. There are some techniques that can be used to realize a digital multiplier such as Wallace-Tree method. This method is famous and enables us to pipeline the multiplication process in order to shorten the critical path. The performance and logic area of the Wallace-Tree Multiplier will be analysed by using Design Vision tool from Synopsys.

### Skills

- Knowledge of Digital/Logic Circuit.
- Knowledge of VHDL or Verilog HDL.

### Contact

If you have interest in the topic please feel free to contact us.

The Art of

Adapting

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