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MES
Institute of Micro-electronic Systems

Welcome Address from the General Chair

Prof. Dr. Dr. h.c. mult. Manfred Glesner

Technische Universität Darmstadt

The European Workshop on Microelectronics Education (EWME) represents a series of conferences and gathers a unique forum of educators and researchers around the globe to discuss new developments in microelectronics education. The conference takes place every two years and in the years between the IEEE Microelectronics System Education (MSE) Conference is held in the USA, usually as a preconference to the Design Automation Conference DAC. EWME and MSE are the major international conferences on educational innovations in a broad range of topics in micro- and nano-electronics. The previous conferences of EWME were held in Grenoble (1996), Noordwijkerhout (1998), Aix-en-Provence (2000), Barcelona (2002), Lausanne (2004), Stockholm (2006) and Budapest (2008).

This year's EWME2010 is also special for several other reasons: more than 60 years after the invention of the transistor and more than 50 years after the invention of the integrated circuit we recently celebrated the 20 year anniversary of the EUROCHIP/EUROPRACTICE-Organization. Such service organizations reflect at its best the rapid changes which we experience in the changes of the value chain in microelectronics. EUROPRACTICE together with its sister organizations like CMP Grenoble, MOSIS in the USA, CMC in Canada, IDEC in Korea and others around the globe has helped numerous students, researchers and enterprises to get a fast-turn-around-chip-fabrication for their designs.

Today a lot of the fascination associated with microelectronics has passed away, industry has dramatically changed and the students in EE and CS encounter a completely different industrial landscape. The progress as predicted by the Moore's Law is still advancing and we will see new electronic systems following the "More-Moore"-path, the "More-than-Moore"-path or "Beyond Moore's Law". With these directions we see exciting developments and research topics arising in the future.

We are proud that the call-for-papers for the conference has found a very high resonance from educators and researchers around the world. In several invited talks the future of micro- and nano-electronics is discussed, how we go on with the services, what new infrastructures we need for academia to deliver to industry top educated undergraduate and graduate students. Special emphasis has been given to emerging technologies like nano-electronics, organic electronics and going from Kirchhoff to Maxwell.

As in many conferences a workshop like EWME2010 is only possible thanks to the excellent efforts of the organizing and steering committees. I would like to thank all of the members of the two committees, especially Bernard Courtois (CMP, Grenoble) who is promoting the conference since its beginning.

But I am especially extremely grateful to the members of my Institute of Microelectronics Systems at Technische Universität Darmstadt: Sebastian Pankalla, Francois Philipp, Christopher Spies and Ping Zhao, who helped in all problems of the detailed organizational efforts, even when we had to move during the days of the peak work to a new building.

Finally we would like to thank all our sponsoring companies which generously supported the conference: Fujitsu, Cadence, Intel, Mentor-Graphics, Eve, Xilinx, CST and XFAB and to the patronizing organisations Verband der Elektrotechnik Elektronik und Informationstechnik (VDE) and its Technical Society Informationstechnische Gesellschaft (ITG) and to the European Design and Automation Association(EDAA).

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Table of Contents (Sessions and Papers)

Invited paper:

“EUROCHIP-EUROPRACTICE- 20 Years of Design Support for European Universities” 1
Carl Das *(IMEC)*, John McLean *(STFC)*

"Microelectronics Education in the South of Brazil and Outcomes" Ricardo Reis *(Universidade Federal do Rio Grande do Sul)* 7

"Maxwell meets Kirchhoff – From Circuits Towards Fields" 12
Irina Munteanu *(Technische Universität Darmstadt)*

Session I: Education with Industry Needs in Mind

“Teaching VLSI Design Considering Future Industrial Requirements“ 18
Matthias Hanke, Thomas Schuster, Tim Kranich, Mladen Berekovic , *(Technische Universitaet Braunschweig)*
Ralf Goettsche, *(High Performance Computing Intel GmbH Braunschweig)*

“Industrial Testing Education at Undergraduate Level: A Datasheet and Diagnosis Based Labs Approach” 23
Béatrice Pradarelli, CRTC, Pole CNFM de Montpellier
Laurent Latorre, Pascal Nouet
(LIRMM / Université Montpellier II / CNFM)

Poster Session I

“SAME goes back to school” 27
Gilles Jacquemod *(University of Nice – Sophia antipolis)*, Jacques-Olivier Piednoir *(Cadence Design Systems)*

“Teaching Analog Design Concepts in Deep Submicrometric Technologies” 31
Juan Jesus Ocampo-Hidalgo *(Universidad Autonoma Metropolitana)*, Jesus E. Molinar-Solis *(Universidad del Estado de Mexico)*, Andres Ferreyra-Ramirez *(Universidad Autonoma Metropolitana)*

"Teaching Cognitive-Inspired Design of Sequential Circuits" 35
Binyamin Abramov *(TAU, Israel)*, Osnat Keren *(BIU, Israel)*,
Ilya Levin *(TAU, Israel)*

"Microelectronics Education at MIEM: from Materials to System on Chip/Board" 39
D. V. Bykov, Konstantin O. Petrosyants, I. A. Kharitonov
(MIEM, Russian Federation)

"A New Joint Research and Teaching Project on Micro-and Power Electronics" 45
Gerhard Gruhler *(Reutlingen University)*, Jörg Schulze
(University of Stuttgart), Markus Lang *(Robert Bosch GmbH)*

Session II: E-Learning

"E-Learning Environment for WEB-Based Study of Testing" 47
R.Ubar, A.Jutman, J.Raik, S.Devadze, M.Jenihhin,
I.Aleksejev, A.Chepurov, A.Chertov, S.Kostin, *TU Tallinn*
H.-D. Wuttke, *(TU Ilmenau)*

"Introduction to Fault analysis at Logic Level – An Educational Approach based on DSCH" 53
Belgacem Hamdi (*ISSAT*), Etienne Sicard, *(INSA-Dgei, University of Toulouse)*

"Interactive eLearning courses" 58
Lubica Stuchlíková, Jana Benkovská, Ján Šebok
(Faculty of Electrical Engineering and Information Technology, Slovak University of Technology)

"eLearning as a support in education of young experimenters" 64
Ján Šebok, Lubica Stuchlíková, Michal Nemec, Jana
Benkovská, Ladislav Harmatha, Daniel Donoval
(Slovak University of Technology)

"EURO-DOTS : A new EC Support Action for Doctoral Training in Europe" 70
Michel Declercq, *(EPFL Lausanne*)
Herman Maes, *(IMEC Leuven*)

Session III: Teaching Nano-Scale Design

"Old IDESA and New IDESA-2: European Training Programs for Implementation of DSM CMOS ASICs" 74

Wieslaw Kuzmicz, *(Warsaw University of Technology)*
Bart Demey, *(IMEC)*

"Teaching CMOS Circuit Design in Nanoscale Technologies Using Microwind" 78
Etienne Sicard and Sonia Ben Dhia, *(University of Toulouse,* Syed Mahfuzul Aziz, *(University of South Australia)*

"A Pilot Course in Vital Electronics" 84
Jerry Gulley (Strategic Security Alliance), Friedrich Holl (Fachhochschule Brandenburg), Ted Kochanski (IEEE Boston), and Andrzej Rucinski *(University of New Hampshire)*

"EuroTraining-Supporting University Programmes in Nanoelectronics" 86
Ivan Ring Nielsen *(Technoconsult ApS DK-2970 Hoersholm)*
Erik Bruun *(Technical University of Denmark)*

Session IV: Teaching System Design

"Learning-by-Gaming in HW/SW Codesign" 89
Vadim Pesonen, Maksim Gorev, Kalle Tammemäe *(Department of Computer Engineering Tallinn University of Technology)*

"*Teaching the Principles of System Design, Platform Development and Hardware Acceleration"* 94
Tim Kranich, Thomas Schuster, Matthias Hanke, Mladen Berekovic, *(Institut fuer Datentechnik, Technische Universitaet Braunschweig)*, Ralf Goettsche, *(Intel GmbH Braunschweig)*

"*The Model Railroad as an Inspiring Platform for Microelectronics Education"* 98
Ralf Salomon, Ralf Joost, and Wiebke Schwelgengräber *(University of Rostock)*

"Multimedia in Optoelectronics and Sensorics" 102
J. Rybár, L. Stuchlíková, J. Kováè Jr., J. Kováè *(Dept. of Microelectronics, Slovak University of Technology)*

Special Session : Microelectronics Education at German Universities of Applied Sciences

"Microelectronic Education by Doing The MPC-Group of Baden Württemberg" 108

Dr. Dirk Jansen, *(University of Applied Science Offenburg)*

Poster-Session II

"FPGA implementation of a real time multi-resolution edge detection video filter" 113
Jeremie Hamon *(PHELMA Grenoble Institute of Technology)*, Vincent Fristot *(PHELMA Grenoble Institute of Technology)*, Robin Rolland *(CIME-Nanotech)*

"Export Mobile Device Display Content" 117
Moritz Prinz, Sebastian Vagedes, Kristian Wessels, Peter Glösekötter *(Muenster University of Applied Science)*, Edmund Coersmeier *(Task9 GmbH)*, Josef Decking *(Muenster University of Applied Science)*

"Synopsys' Interoperable Process Design Kit" 119
Vazgen Melikyan *(Synopsys Armenia CJSC)*, Rich Goldman *(Synopsys Inc.)*, Karen Bartleson *(Synopsys Inc.)*, Troy Wood *(Synopsys Inc.)*

"Integrating Microlectronics Into A Distant Learning Course" 122
Bernhard Hoppe *(University of Applied Sciences Darmstadt)*:

Session V: Teaching Hardware Description Languages

"Aalog and Mixed-Signal Modeling with VHDL-AMS" 127
Abdulhadi Shoufan, Sorin Alexander Huss *(Technische Universität Darmstadt)*

"Platform for VHDL Visulization" 131
Zheng Lu, Abdulhadi Shoufan, Guido Rößling *(Technische Universität Darmstadt)*

Session VI: Course Programs"

"A CDIO-Oriented Master's Program in Integrated Electronic System Design" 135
Kjell Jeppson, Lena Peterson, Lars Svensson, Per Larsson-Edefors *(Chalmers University of Technology)*

"Initiation of a Course Package based on the Bologna process with Support of the Department of Educational Development" 141
Tobias Schwalb, Adnene Gharbi, Klaus D. Müller-Glaser, Marianne Aders, Anke Diez *(Karlsruhe Institute of*

Technology)

Session VII: Teaching Electromagnetic Field Dynamics

"The Dangers of a Simple Usage of Microwave Software" 145
Ulrich Rohde *(Synergy Microwave Inc.)*, Hans Hartnagel *(Technische Universität Darmstadt)*

"An Educational Approach to Electromagnetic Compatibility of Integrated Circuits" 177
Etienne Sicard, Alexandre Boyer *(INSA Toulouse)*

Session VIII: Inspiring Highschool and First-Semester Students

"*Adapting to a Changing Highschool Population"* 180
Cora Salm, Jan Eikel, Erik Faber, Ferdi van der Heijden, Mathieu Odijk *(University of Twente)*

"Introducing Computer Systems Related Topics in the First Study Semester" 185
Maksim Gorev, Vadim Pesonen, Peter Ellervee *(Tallinn University of Technology)*

EUROCHIP-EUROPRACTICE

20 Years of Design Support for European Universities

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Abstract—**The EUROPRACTICE CAD and IC Service has enabled over 650 European universities and research institutes to enjoy access to advanced microelectronics-based design tools and prototyping services over a period of 20 years. EUROPRACTICE services have been used by virtually all of the major universities and research institutes in Europe engaged in microelectronics-based design to underpin their training and research activities.**

Keywords-CMOS, VLSI, CAD, EDA, deep submicron, Microsystems, training

I. INTRODUCTION

In 1989 the European Commission launched the VLSI Design Training Action in order to help European universities train students in VLSI design. The objective was to select 50 universities and provide them with a lecturer post, modern IC CAD tools, low cost IC prototyping and an IC tester. A Service Center, called EUROCHIP, was established to select, negotiate, coordinate and provide these services. In 1995, the Action ended after about 400 European universities had taken up IC design. In 1995, the EUROCHIP project was followed-on by the EUROPRACTICE project, funded by the EC. The goal was to continue the offering of CAD tools and IC prototyping services to the European universities, extend these services to include Microsystems, and also to expand the service to offer industry (mainly SME's and start-up companies) low-cost MPW IC prototyping services plus a service for low volume IC fabrication. Today, after 20 years of successful continuous operation, about 650 European universities and research institutes are using the service and in addition about 200 companies have been able to have their IC designs prototyped and produced in volume.

II. EUROCHIP (1989-1995)

The Service Center EUROCHIP was established in 1989 in order to provide 50 selected European universities with industrial CAD tools for IC design, MPW prototyping and a tester. The Service Center EUROCHIP was set up by a consortium of experienced national centers: IMEC in Belgium, RAL in UK, DTU in Denmark, GMD in Germany, CMP in France and later on also CNM in Spain.

This consortium joined individual forces and started a pan-European service, unique world-wide. The call for 50 selected universities got a huge response and in addition to the 50 selected universities, another 68 universities joined on a pay-as-use basis. This was the first time that universities across the whole of Europe could get access to the same set of CAD tools and IC technologies. This was the basis for the start of true pan-European microelectronics education support. The service started off by selecting 4 CAD packages and 3 IC technologies (3µ, 2µ CMOS). The EUROCHIP Service organized training courses in modern IC design. Standard cell libraries and design kits, fitting the CAD tools, from the foundries were made available. As a result the first designs from the universities were prototyped in 1990.

Over the 6 years of EUROCHIP operation, the Service continually grew and expanded its offering in CAD tools and IC technologies and by 1995 about 400 universities were making use of the Service.

III. EUROPRACTICE (1995 – TODAY)

In 1995, the European Commission launched a new call for a continuation of the service for universities but also for an extension of the fabrication service to small and medium companies. As a result of the call, a new consortium was formed with some industrial partners (that had offered for a few years a similar service to industry – ChipShop). The new service was called EUROPRACTICE and was coordinated by experienced partners: IMEC in Belgium, RAL in UK, Fraunhofer IIS in Germany, Nordic VLSI in Norway and Delta in Denmark. The service offering was significantly extended. A wider range of CAD tools were offered including tools for MCM and Microsystems design. The IC technology portfolio was expanded with more advanced IC technologies, for example 0.8µ down to 0.25µ CMOS, and also BiCMOS, SiGe and high voltage options were introduced. In 2000, the EUROPRACTICE service had reached such a level of maturity in its offering towards companies that the EC decided to only continue to fund the service for the universities. Companies could further make use of the service but only on a fully-paid financial basis. Consequently the consortium changed to reflect the new business model and since 2000 the

EUROPRACTICE IC Service is coordinated by IMEC in Belgium, RAL in UK and Fraunhofer IIS in Germany. Today, after 20 years of continuous operation, about 650 European universities and research institutes are EUROPRACTICE members. The level of complexity of design methods, CAD tools and IC technologies has increased dramatically and will further increase as new design methods and technologies emerge. EUROPRACTICE has successfully helped universities to increase their design capabilities by offering affordable access to the most modern CAD tools, affordable access to advanced (65nm) IC technologies and coupled train-the-trainer courses in MEMs and deep-submicron design.

More than 650 institutions in 44 countries close to Europe currently have a common design infrastructure which is an ideal basis for collaborative research projects. Additionally, designers can quickly become productive when moving between universities or from university to industry.

Although EUROPRACTICE is an EC-funded project, 85% of the project turnover is from the universities. This makes the project unique has contributed to its longevity.

IV. EVOLVING REQUIREMENTS

European academia and has always had a strong capability in Microelectronic design, and EUROCHIP/EUROPRACTICE has provided access to the commercial design tools and processes required to develop those capabilities to the fullest.

The microelectronics design sector changes rapidly, and the EUROCHIP/EUROPRACTICE offering has had to constantly evolve to reflect these changes in order to remain relevant.

The original EUROCHIP scheme was entirely dedicated to IC fabrication. All CAD tools and processes were selected to provide an integrated flow to implementation and test. To this day, this integrated flow from design tools through design kits to IC fabrication is the mainstay of the EUROPRACTICE one stop service.

The mix of design types has changed over time. The emergence of programmable devices for teaching and research offered a viable platform for a class of digital designs that previously could only be realised on custom ICs. At the same time, the number of mixed signal designs and complex digital systems has increased, reflecting the strength of European industry and universities in areas such as communications and automotive electronics.

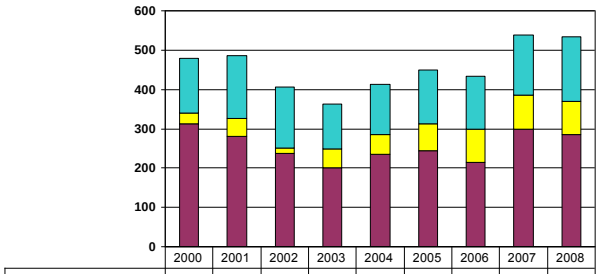
Today's EUROPRACTICE is still built around the strong central flow, usually defined by the reference flow described by the foundry, e.g. TSMC. Different combinations of tools can be used within the flow depending on the preference of the university, and all possible combinations are supported by EUROPRACTICE.

A wide range of tools not dedicated to IC fabrication are now part of the EUROPRACTICE portfolio. This are tools cover a wide range of areas, for example high level system design, PCB layout and analysis, and even device modelling (Technology CAD).

A. IC Design

The aim of EUROCHIP/EUROPRACTICE has always been to stimulate the adoption of new techniques and technologies. During EUROCHIP, this was done by making integrated flows available and using multi project wafers to reduce fabrication costs. With modern complex technologies, additional stimulation activities were required.

For Deep Sub-Micron (DSM) technologies of 90nm and below, the high cost of manufacture was a barrier for many universities. Even after a silicon subsidy was applied, the cost was not affordable for university projects. Aware that the technical demand was there, and that price was the problem, EUROPRACTICE was obliged to solve the problem. The solution was sub divide the minimum block size offered by the foundry, and allow universities to buy one of more sub blocks. After introducing this program, dubbed "mini@sic", there was a distinct increase in the number of designs submitted for the eligible technologies.



	2000	2001	2002	2003	2004	2005	2006	2007	2008
Industry + non-European univ/research	140	159	155	115	128	138	134	154	164
Europractice Research	27	46	13	48	52	69	84	87	85
Europractice Academic	313	281	237	200	234	243	215	298	285

Figure 1. Increase in prototyping due to mini@sic

After the introduction of the mini@sic program, it was clear that there were still some universities who were unable to contemplate designing with these DSM technologies. The reason cited for this was a lack of training on the specific problems of designing at or below 90nm. This problem was addressed by the EC training action, IDESA that addressed these issues, and gave practical tutorials illustrating DSM using tools and technologies from the EUROPRACTICE portfolio. This tightly coupled training action is only possible due to the commonality of tools and design kits across Europe.

B. FPGA Design

The early MPW runs of EUROCHIP featured large numbers of digital circuits, but by 1994 a new platform for digital design was beginning to emerge, the programmable device.

At first, these programmable devices whose software ran on low cost PCs rather than expensive UNIX workstations, were seen as a replacement for university tutorial sessions that had traditionally employed breadboards, with perhaps the possibility of some small student projects using the largest available devices. EUROCHIP introduced software and hardware from the programmable device vendors Altera and Xilinx to the portfolio but also introduced a wider range of PC based software to allow the fullest possible exploitation of the technology.

The programmable devices that required a separate hardware programmer gave way to the reprogrammable FPGAs that we know today, and sizes ramped up from a few thousand logic gates to tens of thousands and eventually millions. Steadily more and more digital design projects became feasible on FPGA, and digital ASICs were less essential for all but the most challenging projects. The software required to create designs on FPGA became more sophisticated as these large digital designs faced many of the same problems that large digital ASICs did. EUROPRACTICE sought to provide FPGA capable tools from vendors already within the portfolio to provide as much overlap between existing IC holdings and new FPGA holdings. Where available, all interfaces between existing tools and FPGAs were also made available.

Now, EUROPRACTICE users can implement a 64 bit microprocessor in an FPGA on a low cost development board using the same synthesis and verification environment used for IC design. Modern FPGAs can offer a quick implementation of an algorithmic or C based design, or a prototype of a more complex system.

C. MEMs

Micro Electrical Mechanical systems (MEMs) was a discipline largely confined to the laboratory at the beginning of EUROCHIP. In EUROPRACTICE, the MEMs activity that was growing in Europe was supported first by the introduction of tools for MEMs design. Where possible, these tools were selected to complement the existing IC layout tools available, so that universities could build upon their existing expertise and save the cost of buying additional layout tools.

The initial adoption of MEMs technology outside of a core group of universities was not as rapid as had been hoped, despite access to design tools and fabrication.

The obvious solution was to reuse the thinking from the IC history, and launch an integrated flow including a Multi Project Wafer service for MEMs. Today universities can submit designs to MPW runs on the Tronics MEMSSOI and three different processes from MEMSCAP. The current MEMs MPW and software offerings are already larger than the initial IC offering of EUROCHIP.

One of the challenges of designing MEMs is that detailed knowledge of the specific processes is required in order to obtain maximum design efficiency. To this end, the EC training action STIMESI was created. The original project ran between 2006 and ended in 2009. Short courses were offered in a wide range of MEMs areas at locations across Europe. Recently a second phase of the project was announced, this time focusing entirely on the MPW and software available via EUROPRACTICE in order to address the widest possible range of universities, and give them the best possible chance of exploiting what they have learnt.

D. System on Chip

As the geometries of ICs have shrunk, it has become practical, and for many applications, highly desirable, to incorporate one or more general purpose processors onto a die with other digital logic.

A major barrier when producing an SoC is the selection of a microprocessor. During the early phases of SoC adoption, EUROPRACTICE secured processor IP, along with the right to use that IP in a non commercial design with no licensing fee. This approach, while appropriate at the time was somewhat restrictive, in that universities were limited to a single architecture and a small selection of processes. As time moved on, EUROPRACTICE was able to support open standard busses and processor IP that could be synthesised for any process.

A recurring theme of these projects is that cost is always a consideration for universities. It can be difficult to justify the cost of creating an ASIC to demonstrate a working SoC, even for a project where the architecture of the SoC is the primary focus. As with digital ASICs before, the solution became available with high density FPGAs. EUROPRACTICE has supported SoCs on FPGAs since their earliest days, including the brief phase when FPGA manufacturers implemented fixed processors on the FPGA die. Ultimately synthesized processors became the best solution, and the rich library of system IP available on FPGAs makes this an excellent companion platform to ASICs for SoC development and research.

As large scale SoCs became viable, interest in system modelling also increased. Where previously this had largely been undertaken as a separate exercise unconnected to the implementation flow, the examination of architectural trade-offs between hardware and software, between single versus multi-core and in the optimal deployment of complex bus hierarchies has become a critical part of the design process. The introduction of system modelling languages like SystemC and System Verilog, and the tools to use them has attracted yet

another type of user to the scheme, hardware and software aware, but distinct from both.

Many of the systems designed using these languages are destined to remain theoretical, but a full path down to silicon or FPGA exists if required.

E. Embedded Software

Early systems that included software most often had either a microcontroller or a small microprocessor. In either case, it was quite feasible to write microcode by hand, or implement an assembler for the limited instruction set.

Modern SoCs run much more sophisticated code; they are far more likely to be running a video processing algorithm or TCP/IP stack than acting as a simple job scheduler. Developing the system software to run on these SoCs requires a more complex programming environment. In recent years, EUROPRACTICE has introduced embedded tool suites based on the Eclipse tools, as well as the ARM RealView developer suite. Now designers can develop not only the systems software, but also the application software, using compilers in a fully integrated development environment, with a comprehensive range of software IP.

In industry, it is common practice for the development application software for SoCs to begin as early in the design process as possible. Universities have embraced these tools for creating Virtual Platforms or Programmer's View models to give training on embedded systems programming, or to allow multi-disciplinary teams to work together on a mixed hardware/software project.

For some applications, there is no ideal processor available for a specific task. In this circumstance an Application Specific Instruction set Processor (ASIP) can be developed using tools within the EUROPRACTICE portfolio. Once the processor is specified, a full hardware description language can be generated and passed to a standard synthesis tool to create a gate level description. In addition, a full set of programming tools can be derived from the same source, giving an assembler, debugger and c-compiler unique to the processor.

Clearly these processor development tools are of interest not only to the IC design community, but also to those interested in teaching and researching processor architectures, so the EUROPRACTICE community continues to diversify.

V. MEMBERSHIP MODEL

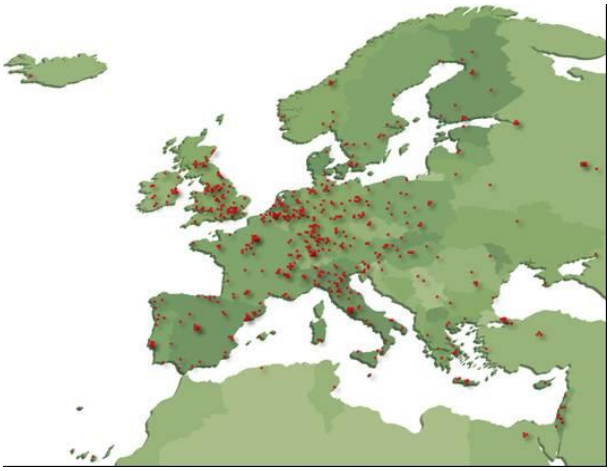


Figure 2. Current EUROPRACTICE members

The current EUROPRACTICE membership stands at more than 650 institutes in 44 countries close to Europe. The laws and business practices in these countries are all different; some are in the EU while others are not. Most of the countries have a local office, or appointed representative, of the commercial vendors that supply the software and device manufacturing capabilities to the scheme members. Despite this, all goods and services are supplied through the EUROPRACTICE consortium, and European academics have a single set of prices and terms that apply to all.

All universities sign up to the same Membership agreement, the same End User Agreements (EUAs) for software, and the same Non Disclosure Agreements (NDAs) for access to foundry design kits.

This is achieved by, where possible, having each university join the scheme as a single member, rather than one membership per department. This gives the university cost savings on membership and maintenance fees, but perhaps more importantly enables the commercial vendors to perceive that they have a corporate level account with the member university through the scheme. The scheme interacts with the commercial vendors at either head office or European office level, to ensure that the same terms and conditions can apply across such a wide and diverse region.

VI. OPEN EUROPEAN INFRASTRUCTURE

Figure 3. EDA Software Partners

As the beginning of EUROCHIP, the model was to provide design tools, design kits and access to fabrication as a single unified flow that was guaranteed to be compatible. This model can be supplemented by coupled training activities to provide a complete solution for Microelectronics based training.

Many things have changed since EUROCHIP, but this classic model still holds true today. Design kits are more complex, and design tools are perhaps more likely to come from multiple vendors in a single flow, but the basic model still holds true. Today's deep submicron flow follows this model, with IDESA, an allied, but separate, project providing the training. For MEMs, the training is available from STIMESI.

For the emerging photonics area, the route to fabrication is not within the EUROPRACTICE project, but via the ePIXfab an EC project to provide photonics MPW services. The tools available via EUROPRACTICE have been aligned with the requirements of this MPW service to provide a seamless flow for users.

Figure 4. Foundry and Design Kit Partners

The more established IC field has many options for fabrication, including other MPW services and direct foundry access. As often the decision on which technology to use is heavily influenced by collaborating partners, or specific technical advantages, EUROPRACTICE has always maintained good links with other fabrication providers, and cooperated with them to ensure compatibility between EUROPRACTICE tools and their processes.

Similarly the EUROPRACTICE MPW service is open to all. While European academic members benefit from a silicon subsidy, it is possible for universities to gain unsubsidized access without becoming a member, as can commercial companies. There is no requirement to use tools sourced via EUROPRACTICE to submit designs to the EUROPRACTICE MPW service.

EUROPRACTICE always strives to maintain open interfaces in the design tools and design kits that it provides. The commercial design tools and design kits supplied are exactly the same as those provided to industry, so if a design kit contains data for tools not available via EUROPRACTICE that data will be supplied. All EUROPRACTICE tools contain the same interfaces as when supplied to industry, so that a university is free to use design tools supplied by EUROPRACTICE in the same flow with design tools from other sources, even tools developed within the university.

VII. INDUSTRIAL IMPACT

Microelectronics is an important industry for the European economy, and keeping that industry healthy in an increasingly competitive global marketplace is a significant challenge. European universities are a vital part of the supply chain for European industry, both through the opportunities created by university research and the supply of highly skilled graduates that are the raw materials for future industrial success.

EUROPRACTICE provides universities with access to the same tools that are used in industry, the same design kits that are used in industry and the same processes that are used in industry. This common platform ensures that the skilled graduates being produced are far more immediately useful to industry, and that collaborative projects between universities and industry have a common basis on which to work.

To further facilitate cooperation with industry, all EUROPRACTICE MPW services are open to industry for prototype and small volume production.

EUROPRACTICE software is provided under a strict non commercial use policy, but by special arrangement, a university can apply for an extended license that, subject to approval, allows a collaborative project to be undertaken with an industrial partner.

In order for European industry to prosper in the future, it will need to continue to exploit emerging technologies as early and as efficiently as possible. This has driven EUROPRACTICE and its university customers to diversify into areas such as

photonics and microfluidics. By making tools and processes in these areas available as early as possible, EUROPRACTICE helps European universities be in the best position to establish industries around these new technologies.

VIII. The Future

The EUROPRACTICE scheme has always striven to remain as close as is practical to the leading edge of industry standard design flows, tools and processes. For this reason we are able to look into the near future with some reasonable confidence.

In the IC fabrication area, we will have already seen university access at the 65nm node. We would expect that within twelve months, it should be possible for universities to gain access to 40nm technologies. In accord with EUROPRACTICE principles, this technology would be available as a mini@sic process to allow affordable access to these advanced processes.

Photonics has emerged as an exciting area for designers in recent years. Although still in its early stages as a design discipline the EUROPRACTICE portfolio already has tools to perform optical analysis and tools that allow for the layout of photonics structures as custom structures or as standard structures from a library of optical components. These tools will complement the MPW service via ePIXfab.

New tools for C based design of circuits have recently become available, and further tools in this area will follow.

In increasingly important areas such as BioMEMs, universities are well placed to take advantage of the diverse EUROPRACTICE offering when designing heterogeneous systems. In addition to IC and MEMs design tools and fabrication options, EUROPRACTICE also has design tools for PCB design, including System-in-Package (SiP).

An interesting new development in the tool area are tools for evaluating the impact of design decisions on a final chip at a very early stage of the design process. Designs can be evaluated for traditional criteria such as power, but for the first time they can be evaluated on cost to manufacture. These tools will show the full cost of fabricating a chip, the likely yield and the number of devices that must be produced to achieve a given price point. These tools have a very direct application for those who produce large numbers of chips for large research projects, but also afford a great opportunity to illustrate the economic and business aspects of IC design as part of a modern curriculum.

IX. CONCLUSION

European Universities and Research Institutes have affordable, one-stop access to the best design tools, design flows and processes normally only available to the largest multi-national corporations. European fabless design companies have easy access to prototype and small volume fabrication, packaging and test. This common European microelectronics-based design infrastructure facilitates cooperation. Graduates entering industry from European universities are more appropriately trained and are more able to meet future challenges of industry.

As the requirements of European academia have evolved, so have the offerings of the scheme. The areas of study have diversified, and the EUROPRACTICE user community of today is far broader both geographically and thematically than could have been envisaged at the beginning of EUROCHIP.

Acknowledgment

The collaboration of all EUROCHIP and EUROPRACTICE project partners with the authors of this paper is gratefully acknowledged.

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Microelectronics Education in the South of Brazil and Outcomes

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***Abstract*—This paper presents a historical review and addresses the process established to start the development of a Microelectronics environment in the South of Brazil, based on the graduate and undergraduate education on microelectronics developed over the years at the Federal University of Rio Grande do Sul, at Porto Alegre. For example, one of the strategies was to found a Microelectronics research group at UFRGS and then promote the education of Microelectronics not only at the UFRGS Federal University, but also throughout the South of Brazil. The education process that was adopted at UFRGS will be presented. Under the Microelectronics Group initiative, a set of events (summer schools, conferences and workshops) was set up in the South, as an important action for the dissemination of the area within other universities and companies. The presence of students and faculty members in international activities had also an important effect. It will be presented the results of this process that were very significant, considering the microelectronics network that was established in the South of Brazil. The industrial milieu in the South of Brazil was also impacted by the Federal University activities. The paper addresses how the industrial environment progressed in Brazil – with retreats and forward moves - and the outcomes for the current industrial scenario. The impacts of this process in the development of the field in the whole country are also addressed.**

I. INTRODUCTION

The set up of the academic environment to support the development of the Information Technology Sector started in the UFRGS (Universidade Federal do Rio Grande do Sul) at Porto Alegre, in the beginning of the seventies. A group of professors from the Electrical Engineering Department, from the Data Processing Center and from the Physics Department started the Graduate Program on Computer Science. This Graduate Program had a strong group on conventional hardware design, where many dissertations finished by the development of pre-industrial prototypes of digital equipments. This initiative by the Federal University was responsible for the spin off of several companies that started an IT industrial environment in the state of Rio Grande do Sul. They worked more notably in the fields of industrial automation, data communication equipment and computers of the early 1970 vintage. Most of these companies exist till nowadays, since they were able to keep their internal capability to develop both their hardware and their own software technologies. After this transfer of technology to the industrial sector, there was recognition in the Graduate Program that the University, and the Graduate Program in Computing in particular, should work on new technologies that the industry would need in the future. So, it was clear that the technologies that the local industry in South America lacked were the complex of technologies and know-hows that had to do with microelectronics that is the integration of circuits onto a chip. In the mid-1970s the industry worldwide moved to VLSI era, which led later to the system-on-chip era. Then the head of the Graduate Program, professor Daltro Nunes, encouraged new students and provided the support for young researchers and faculty – most with the M.Sc. degrees acquired at UFRGS - to leave for Ph.D. programs abroad (most in France and Germany) in the field of microelectronics. So, by the end of years 70, some young researchers went abroad to prepare a PhD in the field of Microelectronics. The first destination was the ENSIMAG, Grenoble, where the ARCHI team leaded by professor François Anceau was starting researches in the field. Others went to other destinations like Stanford, Munich, Kaiserslautern, Karlsruhe and Louvain-la-Neuve. By the end of 1981 they started to return from Europe, Altamiro Susin being the first one that returned to Porto Alegre with a Docteur Ingénieur degree in Microelectronics by the Institut National Polytechnique de Grenoble (France). In 1983, the Microelectronics group at the Federal University was officially started as part of the Graduate Program in Computing. Early members were Altamiro Susin, Tiaraju Wagner and Ricardo Reis. At that time in Brazil other groups were also working in Microelectronics, in Sao Paulo and Campinas, in topics related to the fabrication of circuits. At the UFRGS Microelectronics group we decided to focus and promote the fields of IC Design and EDA development, by starting a new event that became the first national event in the field, the SBCCI, initially named Brazilian Symposium on Integrated Circuit Design, later changed to Symposium on Integrated Circuits and Systems Design. The first SBCCI

was organized by our group and held in Porto Alegre, from 7 to 11 November 1983 [1].

II. International Cooperation

Since the beginning of the Microelectronics Group, it was clear that we should use as reference for our research and educational activities, the international state-of-art in the field. At the very beginning of our group the participation and publication of papers in the main international conferences was encouraged. This was important to obtain some visibility of the group outside of the country and to expand the international ties of the group, which had commenced with the first Ph.D. thesis defended by Brazilians in France, Germany and, in one case, in the USA. The establishment of international cooperation was a mainstay of our team, in which all the students – at even the Master level – were encouraged to engage in. The first formal international cooperation was done with the ARCHI group of INPG, in 1980, using the framework of CAPES/COFECUB, a cooperation program established by French and Brazilian Governments, at the level of their Ministries of Education. Since then, several formal research cooperation projects were done with TIMA and LIRMM (France), Darmstadt and Karlsruhe (Germany), Louvain-la-Neuve (Belgium), INESC (Portugal), IMSE and Univ. Sevilla (Spain). Nowadays the international cooperation is also extended to the exchange of undergraduate students under cooperation programs with France, Germany and USA. Another important collaboration that UFRGS had since 1990 was under the cooperation programs that promoted the Ibero American or Latin American cooperation like ALFA Program, Cyted, Iberchip and others.

III. Undergraduate Scholarships

One very important factor of attraction for students to work in the field of microelectronics was the inclusion of undergraduate students as part of our research teams. The CNPq (Brazilian Science & Technology Support Agency) is the main provider of scientific initiation scholarships to undergraduate students. We engage in our research teams undergraduate students from Computer Engineering, Electrical Engineering and Computer Science. In Brazil, the students start their engineering undergraduate just after high school, with about 17 or 18 years old. The undergraduate courses takes about 4.5 to 5 years. We engage in our research projects, generally students that are in the third to the tenth semester. The engagement of young students is good, since gives more time to the students to increase their maturity in research. Some of them finish their undergraduate course with results that let them to be co-authors of papers in international conference or journals. Some have already a research experience and results that can be the basis for a master or PhD work. As they work in a research team, they are witness of the work of PhD and Master students, and they can have a daily interaction with the more experienced members of the research team. It is also possible to say that a large percentage of the PhD and Master students we had, started as undergraduate students in our research projects. A large number of the best PhD works where done by students that started working as undergraduate students in our research projects.

IV. CMP

In the beginning of the Microelectronics Group, one of the first challenges was to prove to local companies and funding agencies that our group had the knowledge and the capability to design a chip locally. Since Brazil never had a MOS-capable lab or company, the only route to silicon prototyping was through the other nations multi-project wafer programs. Then UFRGS became one of the first and regular users of the CMP Program established at INPG in France. In 1984 our group, with the work of a few Master and undergraduate students designed a simple controller chip that sent to fabrication in France through CMP, and that was later tested and used to control an elevator prototype exhibited in a large IT Expo in Rio de Janeiro.

V. Graduate Education

The Microelectronics Graduate Education started at the Master Level under the umbrella of the Graduate Program in Computer Science (at that time the Master Course could take up to four years of work, or even more). The first Master Student (1980) was Ingrid Jansch Porto, who designed a digital system in I2L, under the supervision of Anatolio Laschuk, to be fabricated in a bipolar facility in Brazil. The second one was Antonio Todesco (nowadays working at AMD, USA), his advisor being Altamiro Susin. The subject of his work was the development and design of a RISC microprocessor. Only later, in 1989, the PhD Program in Computer Science was started at UFRGS with an emphasis in Microelectronics. In 2002, as a response to a Ministry of Education CAPES action willing to set up Graduate Programs in Microelectronics, UFRGS started a multidisciplinary Graduate Program on Microelectronics with the participation of professors from the Electrical Engineering Department, Informatics Institute, Physics Institute and Chemistry Institute. In this Program the students have exposure to device fabrication, device physics, digital and analog design, EDA, and testing and characterization of semiconductors. There is at least one mandatory course in each of these subjects. The students have access to a small, academic clean-room with furnaces, lithography, implanters, metal deposition and all the essential steps to build integrated devices on silicon.

One action that is regularly done with PhD students is to promote their internship in research labs of international companies working on microelectronics or in research labs of universities in other countries. Several students also do PhD in “cotutelle” between two universities and receiving a PhD diploma from both universities or even one PhD diploma emitted and signed by both universities.

Micro and nanoelectronics is also part of the new Nanotechnology Center of the University.

VI. Undergraduate Education

The undergraduate courses started just after high school and takes in general five years. The selection process to be enrolled undergraduate course of UFRGS has in our fields about 10 to 15 candidates per position, we have in general good students. The students have to select their courses when applying for a position, so before the selection process that is based in 5-day exams. In the undergraduate courses the students have basic courses (Physics, Mathematics) in parallel to courses related their field of option. For example, students in Computer Engineering or Computer Science have a course on "Computer Organization" when they are in the first year of the University (17 or 18 years old). The undergraduate education courses, where microelectronics is included, are: Electrical Engineering, Computer Engineering and Computer Science. The main courses related to microelectronics are: Digital Circuits, Integrated Circuit Design I and II, Digital Systems, EDA, Analog Circuits. Each one of them takes 60 hours in one semester. In Integrated Circuits I and II the students have an experience in designing with professional EDA tools. It is important in our opinion to put the young students in contact with professional tools as soon as possible.

VII. Education Outcomes

In 1984, it was started a local event, named SIM, that started as a UFRGS Seminar on Microelectronics and that later becomes The South Symposium on Microelectronics with already 25 editions. Each student should prepare a short paper with 4 pages, in English, that will be part of formal proceedings. This is in general a first experience of a local student in presenting a paper in a conference. One important action was to motivate students and lectures from several universities in the State of Rio Grande do Sul to start activities in the field of microelectronics. One regional action was to set up in 1989 a series of regional summer schools in Computer Science/Engineering where microelectronics was always one of the subjects. The first edition was organized in the Federal University of Santa Maria. Later, in 1998, it was started a series of Regional Microelectronics Summer Schools (EMicro) organized each year in a different city of Rio Grande do Sul. The first edition was in the city of Pelotas (South Rio Grande do Sul). The EMicro has basic courses to students that don't have experience in the field as lectures in state-of-the-art topics given by researches from Brazil and from many other countries. The EMicro together with the SIM (South Symposium on Microelectronics) keeps moving each year between different locations of the State of Rio Grande do Sul. This fact is helping to promote the microelectronics and to attract new students to do a Master or PhD work. One important outcome is that nowadays there are professors with PhD in Microelectronics that are engaged in several universities of the State (like PUCRS, UFSM, UFPel, UCPel, UNIPampa, Unijuí, UERGS). We can say that it was constructed a Network of Microelectronics between these Universities.

VIII. Conference Organization

The starting of the SBCCI Symposium in 1983 [1] under the sponsorship of the Brazilian Computer Society (SBC) and organized by UFRGS, was an opportunity to promote the fields of Design, Test and EDA in Brazil. Moreover, the positive evolution of SBCCI in scope and quality also promoted an increasing relationship between the Brazilian research community in those domains with the International community. SBCCI provided, in a smaller scale here in Brazil, the same effect that the DATE event had in the European Community in Design, EDA and Testing. In 1998, SBCCI started to be published internationally by the IEEE Computer Society Press [2]. Later, as ACM SIGDA started also to co-sponsor the SBCCI Symposium, jointly with IEEE CASS, SBMicro and SBC, the SBCCI Proceedings moved to be published by ACM Press, as they are still today [3].

The UFRGS Microelectronics group also organized several editions of international conferences like IFIP EDAF (1994) on Design Frameworks, IFIP VLSI (1997), IEEE CS ISVLSI (2007), IFIP/IEEE VLSI-SoC (2009), IFIP Edutech (2009), IEEE LASCAS (2010) for Circuits and Systems Society.

IX. Industrial Setting And Impacts

The commercial microelectronics industrial activity in Brazil started in the 1960s with back-end (packaging) and later with a few bipolar (linear and LSI circuits) wafer factories. Due to the lack of investment by the TNC (transnational corporations) and the higher financial barriers that resulted from the submicron VLSI era started worldwide in the mid-1980s, Brazil never had a wafer fab with NMOS or CMOS capability, not even a 6 inch fab of any type. In the 1990-1995 period, all TNCs ceased to operate factories in Brazil, closing down back-end and wafer fab operations. SID Microeletrônica was the last factory to close down a bipolar wafer fab in the state of Minas Gerais by mid-nineties.

In Brazil the IC design activity experimented a large impulse with the design group at the Telebras group R&D center. Telebras was a large holding of more than 25 telephone companies, all under federal state control. Telebras started an IC design group for telecom (switched/commuted central office equipment) in the year 1981. That group designed over the years more than 50 ICs that went commercial. The privatization of the telecommunication companies in 1998 led to closing of that group altogether. A few other smaller commercial design companies, like Vertice Sistemas Integrados, Itaucom, and Elebra Microelectronics – all controlled by larger Brazilian investment groups – operated under local control and offered commercial design and introduced chips in the market. All three also closed such operation by the mid-90s.

The research and educational activity at the Master's level at Porto Alegre (solely at the Federal University of Rio Grande do Sul) was since the beginning focusing on MOS circuit and system designs, as well as on EDA tools for physical, logic and digital system design. The knowledge and HR (human resources) produced in these fields by UFRGS contributed to provide people and motivation for young engineers to endeavor into the field. However, the closing-down of several of the local start-ups, of the TNCs operations, of the Telebras group, as well as the distinctively sway of the TNCs away from any advanced chip development in the Brazil, altogether led to the narrowing of the job market for any VLSI IC designer or EDA master's engineer that was graduated in the 1990s at the Federal University. Nonetheless, the Microelectronics Group at the Federal University kept researching tutoring undergraduate and graduate students, collaborating with the centers of excellence in Europe as listed in the previous section, as well as initiated, in the year 1989, the registration of the first Ph.D. students at the Graduate Program in Computing at the Federal University. In the early 1990s a new Master Program on Electrical Engineering started at UFRGS under the vision and direction of Altamiro Susin, also a senior member of the Microelectronics Group.

In 1997 Motorola Inc. started a new operation in Brazil: it set up its Brazilian Semiconductor Design Center (BSTC group) near Campinas in the State of Sao Paulo, which grew steadily over the following 10 years to become a 200-strong group of designers in the area of microcontrollers, power management ICs, analog CMOS, automotive IC design, among others. Hence, several designers who had left the previously closed operations (at Telebras, Vertice, Itaucom, and others) in Brazil could find jobs in the Motorola Company. The design group led by Eng. Armando Gomes at Motorola BSTC started to hire the Federal University students as well as other graduates from a dozen of schools which kept a focus on microelectronics education in Brazil. That group had the lowest turnover rate of professionals within the Motorola Company.

The years 2000-2002 saw a repositioning of the Brazilian government with respect to the microelectronics industry. The foreclosure of several companies in the previous 10 years was a bad record to be overcome. In the year 2000 only 5 companies operated microelectronics in Brazil: two back-end packaging, two discrete fabrication and the Motorola design center. Two plans for the Microelectronics industry rebirth in Brazil were drafted by the Ministry of Science and Technology (MCT in Brazil): the National Microelectronics Program (announced in the 3Q 2001) and the version 2 of the same Program, announced in December 2002. In this new strategy the construction of a small volume CMOS fab was part of the plan, as well as the lauching of a support program to enhance the design capability in commercial design houses. Part of the plan was also to offer Master's and Ph.D. level scholarships for top-level schools like UFRGS.

The strong and high level activity of UFRGS in the South of Brazil was one the main reasons for the choosing of Porto Alegre as the location of the first CMOs wafer fab in South and Latin America, the CEITEC center. It leveraged a memorandum of understanding reached between the Government of Rio Grande do Sul State, the local city and Universities, and the Motorola Company in the USA, which agreed to donate a full set of CMOS-capable wafer fab equipment to the state of Rio Grande do Sul. An agreement signed in June 2000, a year before the Federal Government announced the PNM Plan aforementioned. It is fair to say that the local State of Rio Grande do Sul stimulated and asked the federal government to set up an industrial policy towards microelectronics in the year 2000 and 2001. In [1] Wirth, Bampi et al., presented a positional paper to the SBMICRO Society and later to the Government. The CMOS wafer fab in Porto Alegre is not fully operational, and CEITEC was transformed in 2008 in a federal state-owned company. In 2010 a new semiconductor company is being constructed in the Porto Alegre region, HT Micron as a joint venture of Korean Hana Micron and local companies. HT will be dedicated to packaging of integrated circuits, DRAM in particular.

The CEI (IT companies' incubator of the Instituto de Informática at UFRGS) was also the location of the starting of Nangate Brazil, a branch of the EDA Nangate Company, based in Denmark. At the early stages of business development, under 2 years old, there are also Portochip and Trianda, housed at the UFRGS incubator, startups dedicated to the design of chips and electronic systems design. The CEI is also the location of NSCAD, which is an engineering team with very low overhead costs that is responsible for training in IC Design as well management of EDA environments. NSCAD started in March 2005 at UFRGS University, as part of an academic project of the Microelectronics Group of the Federal University, supported by the FINEP agency. NSCAD is nowadays an independent service supported by the Ministry of Science and Technology. NSCAD is also the responsible for an EDA Training Center (CT) that was established at UFRGS with the goal of providing intensive, professional-oriented, one year training in IC Design using professional EDA tools, to enhance the level of specialization and productivity of the junior designer. These designers are educated in 80 to 100 student groups, divided in smaller design teams, to educate on commercial design practices, and hence provide the required HR to spur the activities of design houses or design companies in Brazil. A second CT was established in Campinas.

X. CONCLUSIONS

The Microelectronics Education developed at undergraduate and graduate levels at UFRGS has been a key contributor for the development of the field of Microelectronics in the region. From the early engaging of new undergraduate students in the field (a scientific initiation that is key to entice young students to study complex issues in Microelectronics), to the high level standard of M.Sc. and

Ph.D. level research, the group has contributed to educate several generations of designers. The young engineering and computing students take part on a larger community, that the events and international interactions that we strive for organizing bring closer to Brazil. Hence, the international collaboration that started between academia – in Brazil and Europe most notably – has grown towards a network of initiatives that make it possible now to relaunch a commercial activity in Microelectronics, with more high technology companies interested in the South of Brazil as a source of ideas and talent – not just as the emergent market that Brazil surely is.

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Maxwell meets Kirchhoff: From Circuits towards Fields

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Abstract

With the evolution of technologies towards higher operating frequencies, smaller dimensions and increased system complexity – often in RF and mixed-signal design –, electromagnetic (EM) field effects come into play in what was until not long ago a purely circuit-design world. Not only device, interconnect and substrate parasitics but also, increasingly, 3D components such as embedded passives, bondwires and packages require electromagnetic field simulation for their accurate characterization. 3D electromagnetic simulation is making its way into the design of microelectronic components and both students – the future engineers – and designers need more in-depth knowledge of this domain. This paper discusses the limits of current design approaches, making a 3D electromagnetic simulation necessary. The new course "Technical Electrodynamics" at the TU Darmstadt is shortly presented. Some illustrative examples are also shown.

1 The limits of 2D

The need for electromagnetic field simulation has been recognized for some time now, and the planar (so-called 2D or 2 ½ D) field simulators are an integral part of many design environments. These simulators can efficiently cover many of the current field simulation needs, but they cannot cope with all the 3D effects appearing at high frequencies. Of course, some components, such as IC packages, are by their nature of 3D type and thus impossible to analyze with a planar solver.

Where are the limits of 2D electromagnetic solvers? This question is very difficult to answer in a general manner since there are several factors that need to be taken into account: geometry, dimensions, operating frequency and possible intervening higher harmonics, robustness of the design are the most important ones.

In what concerns the geometry, obviously, components with clear 3D character will probably need a 3D simulation., since in very few cases there are analytical models available for them. It is obvious that complex structures like IC packages, ball grid arrays, multi-chip modules, and Systems in Package (SiP) belong to this category. Even a simple bond wire affects signal performance, especially at high frequencies, and therefore needs to be optimized for reduced parasitic effects. 3D EM simulation allows even a smarter approach by electrically characterizing bond wires and using them as device in circuit design.

During the last years the increasing number of metal layers in IC technology allowed additional devices, like integrated coil inductors and planar multi-layer capacitors. Their three-dimensional geometries and undefined surrounding make analytical modelling difficult and call for 3D simulation to obtain the required design accuracy. This is also valid for vias which are typically insufficiently characterized in IC and PCB design kits. Especially at higher frequencies an accurate characterization of these geometrically simple structures will most probably require a full wave 3D simulation.

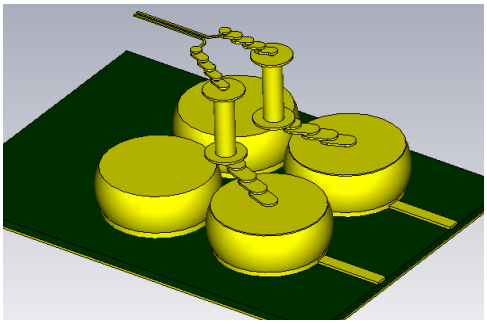
Also geometry-related is the distance between the component of interest and other components or layout elements in the surrounding. While for each component taken separately a classical simulation might have sufficient accuracy, the presence of other components very close by introduces supplementary field effects which may require a 3D simulation. The simple resonator example of section 1.1. nicely illustrates this effect.

The structures' dimensions and the frequency range of interest are two closely related issues. Small structures at low frequencies may not always need a 3D simulation, while at higher frequency even a tiny part might exhibit field effects and require a full-wave 3D simulation.

Last but not least, design quality and reliability are also decisive for the choice of one or another

simulation tool. To give just an example, a fully impedance-controlled design provides the best premises for avoiding disturbance fields which always occur at discontinuity points. However, this is a very difficult, if not impossible task to achieve in a modern design, in which numerous vias, bumps, bondwires are needed. They all induce impedance variations and most probably require sophisticated simulation for their accurate characterization.

a)



b)

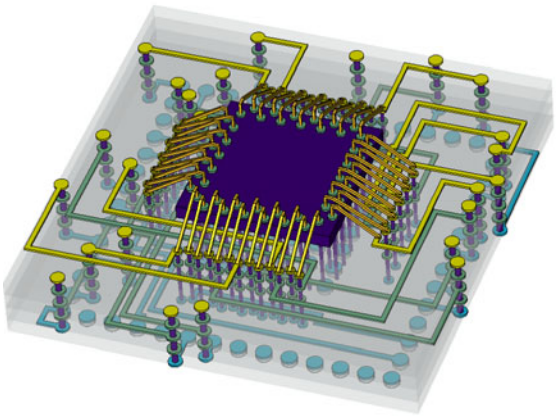


Fig. 1. Typical structures which need 3D EM simulation. a) Vias, bumps and ball grids; b) Full IC packages, bondwires

1.1 An illustrative example

Let us consider a simple structure, an integrated LC resonator, realized in LTCC technology, shown if Fig. 2 [3]. It is representative for passive structures embedded in the RF SiP substrate.

For accurately characterizing the L and C parts of the structure, each of them was simulated separately in the 3D electromagnetic simulator CST STUDIO SUITE [2]. As a result of the simulation, S-parameter models for the two components are obtained, which can then be connected together in a circuit simulation (Fig. 3a). This approach is equivalent to neglecting the field coupling of the two elements.

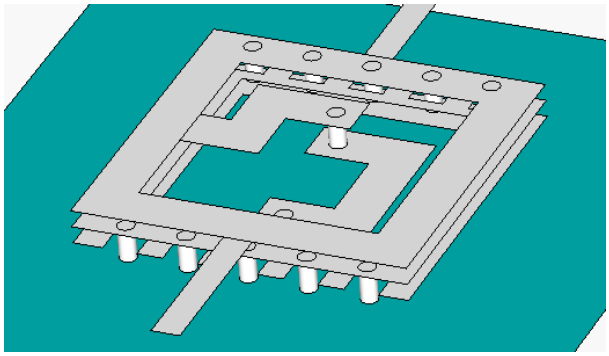
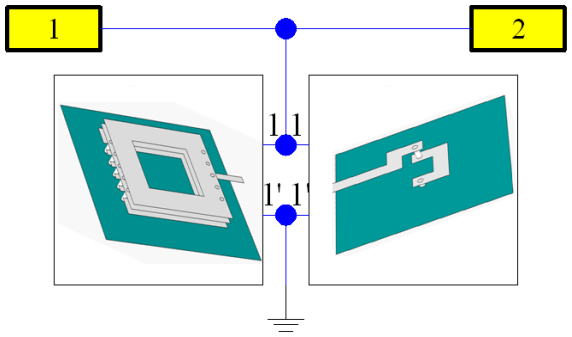


Fig. 2. LC resonator in LTCC technology

To check if these separate models can be used as such with enough accuracy, a second simulation was performed, in which both the L and the C parts were included together in a single 3D model.

a)



b)

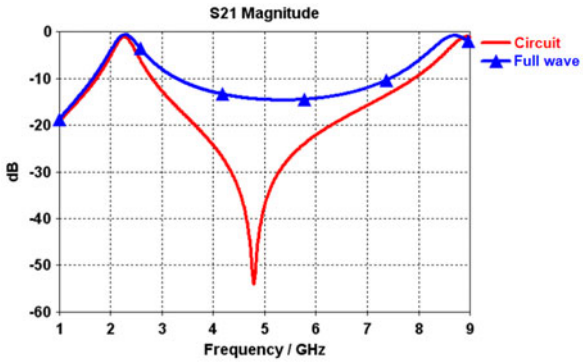


Fig. 3. a) Network model for the LC resonator with the two blocks separately characterized by 3D simulation; b) S-parameters for case a) (denoted “Circuit”) and for the LC resonator simulated as a single 3D structure (denoted “Full wave”)

The corresponding S-parameters are shown in Fig. 3b. Obviously, the capacitor and inductor components of the resonator are placed so close to each other in this configuration that a complete 3D simulation of the whole structure is necessary. However, if the operating frequency is low enough, below 1 GHz, the S-parameters (not shown here) agree quite well in the two setups.

2 Challenges

3D electromagnetic field simulators are still relatively little used in microelectronics. There are several challenges the EM-newcomer is facing.

2.1 Vocabulary

Circuit design specialists know this very well: even analog and RF designers have difficulties in understanding each other. The ones talk about harmonics, saturation and volts, the others about intermodulation, compression and dBm.

It is not much different with field simulation: many things in the circuit and field worlds are similar but just bear different names. What circuit simulation specialists call "edge-to-independent meshes incidence matrix" is named "curl matrix" by field simulation experts. A 3D "discretization mesh" is very similar to a (non-planar) "circuit graph". In some 3D methods, such as the Finite Integration Technique [5] and PEEC [7], a quantity is associated to each edge of this graph which has the dimension of capacitance, resistance or inductivity – all well-known also to circuit designers. Only, field simulation experts call these quantities "elements of the material matrix".

2.2 Simulation complexity

Circuit or analytic models provide an abstraction of the physical behaviour by using device models and therefore allow a quick simulation. They are already well integrated in the design environment and large model libraries are available.

3D field simulations on the other hand require the so-called discretization of the full 3D component (division of space in small elements, such as bricks or tetrahedra, whose number can reach, for just one component, tens to hundreds of thousands). This inevitably makes the simulation of a device with several such components much slower than the simulation based on a circuit model.

Figure 4 shows an example of such high complexity: a full system for biomedical signal acquisition designed in RF SiP technology by the Technical University Hamburg Harburg of Germany [1], that was integrally imported into the 3D simulator.

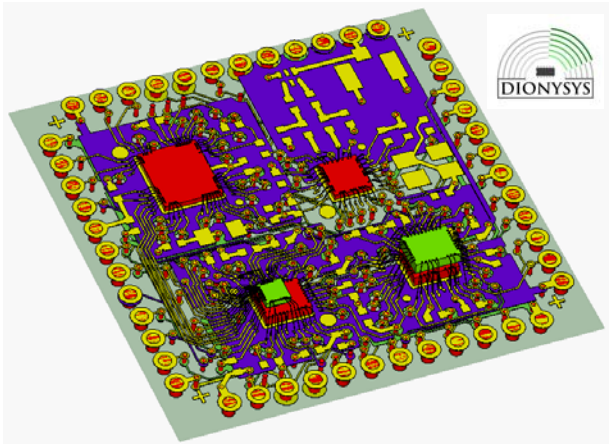


Fig. 4. 3D electromagnetic model of RF SiP for biomedical signal acquisition.

2.3 Expert knowledge in a new domain

Last but not least, in the attempt of mixing circuit and field simulations, two worlds – circuit design and electromagnetic design – come together. We know the circuit world better – many of us had at least one electronic design project in secondary school. Electromagnetic field is taught years later in university and therefore people are not so familiar with it.

Obviously, it is often difficult for someone used to Maxwell's equations to think in circuit terms, or vice-versa. Moreover, the requirements, simulation constraints, and limitations of a circuit simulator are quite different from those characterizing an electromagnetic field simulation. This gives many designers the feeling that they would almost need to „learn" a completely new profession, in order to be able to efficiently include the other kind of simulation in their daily work. Efforts from the side of both the design environment providers and the 3D electromagnetic field simulation companies are under way with the goal to make this (soon absolutely necessary) step as smooth as possible.

So where to start?

The modern designer doesn't in fact need to be an "all-round talent", with a deep knowledge in both circuit design and electromagnetic field simulation.

Mastering the EM-specific **nomenclature** is of course a must – but also a very easy first step. Additionally, some specific knowledge of EM is needed: a basic understanding of **Maxwell's**

equations and of **electric and magnetic fields** can be very useful.

A third ingredient for the future EM-simulation specialist regards the **requirements and possibilities of the simulation** itself. The next section 3 explains these in more detail.

The only part that takes longer is probably to learn how to reach, through clever choices of simulation techniques and parameters, a **trade-off between simulation time and accuracy**. This includes decisions on when a 3D simulation is necessary and when a simpler model obtained with other techniques is sufficient.

3 EM Simulation in a Nutshell

3.1 What an EM simulation is made of

Often, a first clear picture of a scientific domain can be gained by an even short answer to a few simple questions. For EM simulation, the main questions are: What are the input data? What are the important program settings? What types of output data can I expect?

Input data: 3D geometry, material parameters, excitations

The 3D geometry can be either directly constructed by using specialized software or, as most often the case in microelectronics, exported directly from the circuit design tool (the user selects the relevant parts and a transfer of the geometric, material parameter and excitation ports information is performed towards the 3D simulator). This transfer can be automated to a large extent such that a minimum of user interaction is necessary, as shown e.g. in [1]. This step should therefore not represent a problem even for users with little experience in 3D EM simulation. The result of these steps is a three dimensional model of the structure that needs to be characterized and might look like the chip package shown in Fig. 1b.

Main program settings

In 3D simulations, the infinite 3D space needs to be truncated in order to simulate it. The size of the computational domain is one of the settings that influences the solution accuracy. On the boundary of this computational domain, boundary conditions need to be imposed to ensure uniqueness of the solution. One choice would be a boundary condition that simulates the open space. Last but not least, there is the choice of the mesh type, simulation method and whether the simulation should be performed in time or in frequency domain. A short overview of numerical simulations methods is presented in section 3.2.

Output data

There is a variety of results that can be obtained through a 3D simulation. Among them are S- Z- and Y-parameters, an equivalent circuit model that characterizes the port-behaviour of the device, electric currents on traces, grounds and in general on all metallic parts, electric and magnetic fields in any point of the domain, farfield patterns …

In summary:

- **input data**: geometry, material parameters, excitations
- **important program settings**: size of the computational domain, boundary conditions, choice of the solver
- **output data**: S- Z- and Y-parameters, equivalent circuit model, currents on metallic parts, electric and magnetic fields in any point of the domain …

3.2 Methods for full-wave 3D EM simulation

For achieving the EM simulation (so-called full-wave, i.e. without assuming any low-frequency approximations), specialized software packages are used, which implement specific numerical methods.

Among the numerical methods for 3D field analysis, the best-known are the finite element (FEM) method [4], the finite integration technique (FIT) [5], the finite-difference time-domain (FDTD) [6], as well as the PEEC [7]. The FEM and PEEC are typically applied in frequency domain, the FDTD in time domain. The FIT is the only method which can be easily applied in both frequency and time domain.

Each of these methods first discretizes the 3D geometry by using specific discretization meshes. Three representative 3D discretization meshes are shown in Fig. 5.

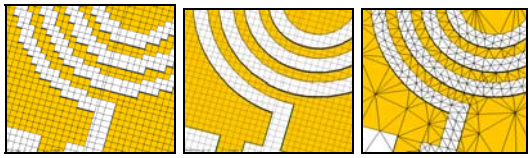


Fig. 5 Detail of a planar coil mesh. From left to right: staircase, confomal hexahedral, tetrahedral.

The electromagnetic field equations – Maxwell's equations – are automatically discretized by the simulation software on the discretization mesh and, depending on the method, solved either in frequency or in time domain. **Transient** (time-domain) simulations are typically performed using an explicit time-marching scheme and have lower memory and computing time requirements than frequency domain simulations. They are ideally suited for broadband simulations of large or very complex structures. Broadband frequency-domain results are obtained from the time-domain signals by means of a Fourier transformation. Frequency domain simulations on the other side require the solution of a system of equations at every frequency point of interest. This requires both a relatively large memory, and a relatively long computing time. For not so large models, they can however be quicker than transient simulations, especially if clever interpolation techniques are used for evaluating the results between the (few) calculated frequency points.

If one starts with EM simulation, he should probably start with FIT, due to the ease of understanding. That is why it is presented in more detail in the next section.

3.2 The Finite Integration Technique

As in any other domain, a user of an electromagnetic field simulation program with a minimum of inside knowledge is likely to achieve optimal results. That is why, in this section, we will try to shortly describe the way in which the electromagnetic field equations are discretized with the Finite Integration Technique (FIT).

Let us demonstrate the derivation of the FIT-discretized form of Faraday's law:

$$\int_{\partial S} \vec{E} \cdot d\vec{r} = -\frac{d}{dt} \int_S \vec{B} \cdot d\vec{S}$$

on the face $S \equiv j$ of a mesh cell, depicted in Fig. 6. The integral on the left hand side (representing the electric voltage along the closed contour of edges which form the face boundary) can be written as an algebraic sum of the edge voltages. The integral on the right hand side is directly one of the FIT unknowns, the magnetic flux through the face j. The discretized equation thus becomes:

$$-e_1 + e_2 - e_3 + e_4 = -\frac{d}{dt} b_j . \qquad (1)$$

Note that we have only used the additive property of the integral, and did not perform any approximation. By writing such relations for all the faces in the mesh, then grouping all the signs plus and minus into a matrix $\mathbf{C}$, Faraday's law has the form given by (2).

In a similar way, the discrete equivalent of all Maxwell's equations, the so-called Maxwell's Grid Equations, can be obtained:

$$\mathbf{C}\hat{\mathbf{e}} = -\frac{d}{dt}\hat{\hat{\mathbf{b}}} \qquad \tilde{\mathbf{C}}\hat{\mathbf{h}} = \frac{d}{dt}\hat{\hat{\mathbf{d}}} + \hat{\hat{\mathbf{j}}} \qquad (2)\ (3)$$

$$\mathbf{S}\hat{\hat{\mathbf{b}}} = \mathbf{0} \qquad \tilde{\mathbf{S}}\hat{\hat{\mathbf{d}}} = \mathbf{q} \qquad (4)\ (5)$$

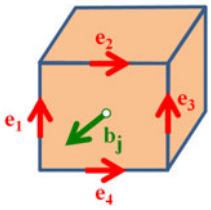


Fig. 6 Allocation of the electric voltage (e) and magnetic flux (b) components in the mesh.

In these equations $\hat{\mathbf{e}}$ and $\hat{\mathbf{h}}$ denote the electric and magnetic voltages along primary and dual edges, respectively.

The symbols $\hat{\hat{\mathbf{d}}}$, $\hat{\hat{\mathbf{b}}}$ and $\hat{\hat{\mathbf{j}}}$ are the electric, magnetic, and current-density fluxes across primary and dual grid faces. The topological matrices $\mathbf{C}$, $\tilde{\mathbf{C}}$, $\mathbf{S}$ and $\tilde{\mathbf{S}}$ represent the discrete equivalents of the curl- and the div-operators, with the tilde indicating the dual grid.

The discrete analogues of material property relations express the coupling between voltages and fluxes, through the material matrices $\mathbf{M}_\varepsilon$, $\mathbf{M}_{\mu^{-1}}$ and $\mathbf{M}_\sigma$:

$$\hat{\hat{\mathbf{d}}} = \mathbf{M}_\varepsilon \hat{\mathbf{e}}; \quad \hat{\mathbf{h}} = \mathbf{M}_{\mu^{-1}} \hat{\hat{\mathbf{b}}}; \quad \hat{\hat{\mathbf{j}}} = \mathbf{M}_\sigma \hat{\mathbf{e}} + \hat{\hat{\mathbf{j}}}_\mathbf{A} \quad (6)$$

These matrices have diagonal form on Cartesian meshes and contain the unavoidable approximations of any numerical procedure.

3.3 Field equations are not that different from circuit equations

That circuit (Kirchhoff's) equations are obtained from the field (Maxwell's) equations is a well-known fact. However, this direct connection is not easily visible in many numerical methods. In the Finite Integration however, the intervening matrices are well-known to the circuit designer:

- The matrix $\mathbf{C}$ has the same meaning as the edges-to-independent-meshes incidence matrix which is used in the loop-current (mesh) analysis; note also that $\tilde{\mathbf{C}} = \mathbf{C}^T$. In field analysis however, the dependent meshes (loops) are not eliminated, for efficiency reasons.
- The matrix $\tilde{\mathbf{s}}$ has the same meaning as the edges-to-nodes incidence matrix, used in nodal analysis.
- The matrices $\mathbf{M}_\varepsilon$, $\mathbf{M}_\mu$ and $\mathbf{M}_\sigma$ have the dimensions of capacitance, inductance and conductance, respectively and can be assimilated with the diagonal matrices containing the edge circuit elements.

For static states, the appropriately combined FIT equations (2-6) lead to exactly the same well-known equations of the Modified Nodal Analysis or Loop-Current Analysis methods.

4 Technical Electrodynamics Course at the TU Darmstadt

At the TU Darmstadt, in recognition of the technological trend, a novel course "Technical Electrodynamics" was included in the Master's Program "Information and Communication Engineering" starting with the winter semester 2010-2011.

The course covers not only fundamental issues of electrodynamics, but also basics of 3D EM simulation and the coupling between the "field" and the "circuit" worlds (cosimulation).

The associated exercise and practical applications class is meant to familiarize the students with the use of a 3D simulator through the simulation "from A to Z" (from geometry definition to result postprocessing) of several typical high-frequency devices. Numerical issues such as convergence for both the linear system of equations and the field solution, accuracy as well as practical knowledge regarding possible sources of error in 3D simulations are also acquired.

Acknowledgment

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Teaching VLSI Design Considering Future Industrial Requirements

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Abstract—**In 1999, the University of Braunschweig introduced a new study program dedicated to embedded systems design called "Computer and Communication System Engineering". It combines traditional educations in computer science and microelectronic engineering. VLSI Design I is one course of this program that works hand in hand with industrial partners. To integrate practical experiences into VLSI education the teaching combines tightly coupled lecture, tutorial and lab to guarantee an ideal learning process. All have the scope on integrated circuits design.**

I. Introduction

Embedded systems increasingly ease our everyday life. Simultaneously their user becomes less aware of them due to their advanced integration. Cell phones, vehicles, medical equipment or entertainment devices unrecognizably rely on digital circuits.

In the past the amount of transistors per area has doubled about every two years [1] leading to a tremendous amount which is no longer manageable by traditional approaches. Thus the development of embedded systems composed of tightly coupled microelectronic devices and multiple software layers has evolved into more platform based design methodologies [2]. This improves the designer's ability of creating more complex systems but does not allow to forget about the transistor's physics as basic element of a circuit. Thus modern education needs to cover a vast range of topics from microelectronic engineering to computer science. Computer and Communication System Engineering is a study program that combines industrial and academic needs of both fields [3].

The philosophy of the VLSI design I course as part of the study program is to tightly couple the contents of lectures, tutorials and labs (Figure 1) supported by industrial partners. This realizes a high level of coherence for the course's contents. Theoretical knowledge is imparted in the lecture. A tutorial supplements it by accentuated exercises. Both events are completed by a lab which includes practical implementations and tool usage. It addresses students from all semesters and thus brings together bachelor as well as master students. The course has been developed in close cooperation with Intel Braunschweig to consider the industrial aspects, technology trends and practical relevant topics. The target is to educate engineers with a sound awareness of technology physics who are able to utilize state-of-the-art design tools.

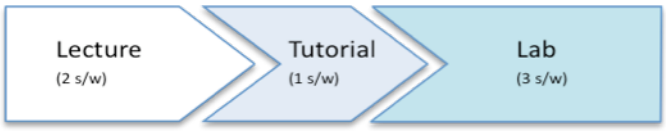

Figure 1: Interlocking of the course's sessions

II. Industrial Interests

Industry partners have dedicated interest in the education of future engineers [4]. Thus they cooperate with universities in creating new study programs, e.g. [5], or in funding professorships. Additionally, they create education programs to support teaching.

Intel believes that students everywhere deserve the skills necessary to succeed in a knowledge-based economy. That is why Intel provides a holistic blend of technologies, programs, and professional development resources for teachers, which can empower countries around the world. With improved teaching and learning environments, students have a superior chance to develop the required skills. Therefore, Intel setup the education initiative [6].

To support education in chip engineering, Intel GmbH Germany sponsored a professorship that takes care of the physical basics for system design. For a close collaboration and exchange, the professorship stands in a direct dialog with Intel GmbH Braunschweig to keep the lectures updated and to orient the lab at actual practices in industries.

III. Course Concept

Future engineers need to have a background in a wide range of topics. It starts from the basic physics of semiconductor materials, continues with the design of circuits including methodologies and ends up in the usage of tools and the handling of operating systems.

Materials and structure of transistors define its capacity, resistance and thus switching behavior. Depending on the technologies complexity different amounts of metal layers can be applied for signal routing. All physical properties of a

manufacturers process technology are represented by tables in a technology file. This file is the target for electronic design automation (EDA) tools that map a register transfer level (RTL) description of a circuit design to gate level. The courses aim is to take student through the whole design process from the physical structure of semiconductors to design methodologies.

Theoretical basics are built up during the lectures. They offer the audience the background they need to have to understand the exercises of tutorials and labs. Tutorials offer guided example exercises to theoretical problems discussed in the lecture. Thus participants get an impression for practical impacts of theoretically discussed lecture content. The Labs communicate hands on skills to connect knowledge from lecture and tutorial with practical tasks with the help of modern EDA tools. As the course program builds up competence from the ground up it demands hardly any prerequisites from its participants. Thus, it allows to address students independently from their study progress. As a consequence, it supports knowledge exchange among the audience.

IV. LECTURES

As the main part of the course the lecture offers the theoretical background of VLSI. It takes two sessions of each 45 minutes a week.

Cost aspects of the chips' manufacturing process introduce to the impact of physical basics to the final product. Namely these are e.g. cost of a die, dies per wafer or die yield. Formulas for the calculation of all of them are deduced stressing the importance of physical devices for the final product. Additionally, the lecture offers a broad overview on the development of the semiconductor market.

This leads to the structure of transistors. Explanations of semiconductor materials treat different devices and their behavior including the meaning of their characteristic plot. Detailed description of internal electrical fields an their influence on electric charges gives a deep insight into the transistor.

Electrical resistance and capacitance have a major impact on signal delays and shapes on a chip. Depending mathematical models are taught as well as interconnect strategies. Furthermore the lecture gives information on how to calculate signal delays.

After explaining structures and behaviors of the chip's elements the audience is introduced to the manufacturing process. Elucidations to oxidation and diffusion techniques lead to standard cell design. This includes design rules and is followed by packaging methods like bonding and flip chip.

Combining transistors to complex gates is introduced by the CMOS inverter as basic element for more complicated functions. The content goes from logical equations over the development of stick diagrams to routing strategies.

Additionally the lecture informs about design methodologies (Figure 2) to show the most efficient way of managing the product development process. This is highly connected to the standard cell design flow from RTL code to synthesis explained on state of the art EDA tools. Implied by this is the introduction to fanout, buffering and critical paths.

Furthermore there is focus on programmable logic arrays showing the potentials of reconfigurable hardware. Especially these devices are connected to the term of intellectual property (IP). Students learn how to differ hard and soft IP going along with the allocation to design hierarchies.

Correct hardware verification becomes increasingly important with growing design size and complexity. Thus finally the lecture gives information of modern test and self-test methods of designs.

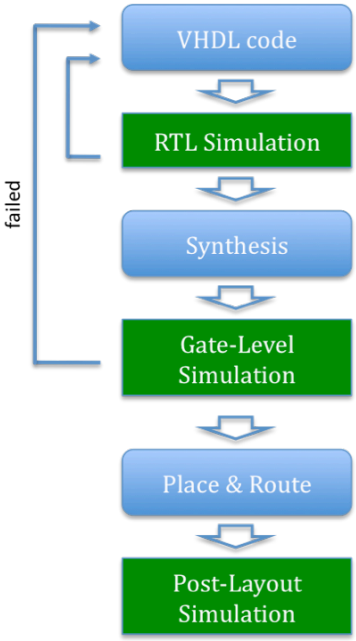

Figure 2: Typical ASIC design flow

This lecture content supports the understanding for designing and optimizing digital integrated circuits with respect to different quality metrics namely cost, speed, power and reliability.

V. TUTORIALS

Supplementary a dedicated tutorial of one session a week offers practical exercises on selected topics from the lecture. It covers essential calculations essential for VLSI system.

Final product cost is an important factor influencing the success of a design in market. Thus Students learn how to practically estimate the package costs for chip development from the theoretically treated formulas of the lecture including e.g. the calculation of yield and process complexity parameters. Along with this goes the understanding of certain design attributes' cost impact e.g. chip size and utilized technology.

Embedded circuit are built up by transistors. As follows an introduction to the transistor plot explains the physical behavior of the basic circuits' element. From given physical parameters and formulas from the lecture characteristic values have to be calculated. These are used to reconstruct the plot for a transistor. Additional exercises practice how to calculate

saturation current or how leakage varies according to temperature.

Employing De Morgan's rule students learn how to derive the logic equations for CMOS circuits design. They are enabled to transform equation into transistor-level schematics and vice versa. Furthermore they are introduced to the creation and comprehension of stick diagrams.

Interconnect modeling is the first step to be done before applying mathematical models on a circuit. Exercises on Elmore delay show how to derive timing from the created models. This clearifies the influence of wires' length on signals.

Additionally logical effort notation is covered by the handling of formulas for path and gate on example circuits. Propagation delays are calculated on the example of a NAND gate. Delay on path level is calculated on a circuit consisting of different NOR and NAND gates.

These exercises offer practical experience to the theoretical contents of the lecture and thus deepen the taught subjects. They build a bridge to the contents treated in the labs.

VI. LABS

The lab closely follows lecture and tutorial. With its three sessions a week it forms a major part of the course. Its aim is to give a deep insight in the practical design process of VLSI systems. Students are guided through the whole system design process starting at RTL and reaching GDSII including place and route.

Operating system for the labs is RedHat Enterprise Linux [7]. All utilized tools are installed on virtual machines (VM). According to this the system for all work stations is only set up once and can be employed on nearly every host operating system. This enables to have a clean system on the start of a lab just by copying the VMs on the computers' hard disks. Furthermore the installation works independent from other installations. Result is a very low maintenance effort especially when working in a computer pool that is used by other work groups either that have own dedicated demands on the system configuration.

As students from all stages of their studies are addressed it can not be presupposed that all of them are familiar with the handling of UNIX systems or hardware description languages (HDL). To bring all participants to the same level the lab starts with the very basics by giving an introduction to all needed LINUX commands and a single session to VHDL.

The whole lab is build up upon a simplified 16 Bit VHDL extensively commented MIPS I microprocessor core. Instruction set and pipeline depth are reduced in comparison to a complete implementation. This core allows an immediate start quickly leading to the emphasis of the course as students do not have to write the whole structure theirselves but are enabled to concentrate on the most relevant elements.

The lab is structured by ten dates:

- The center of modern embedded systems usually is a microprocessor. Correct and efficient utilization is a fundamental to create competitive solutions. That is why system designers need to know about the basic properties of their system's processor. Thus students get to know the MIPS instruction set. From the data sheet they learn the different instruction formats i.e. I-, R- and J-instructions. Afterwards they identify the yet implemented ones in the given HDL code.
- Extending the given core to a 32 bit processor (Figure 3) is the first practical task. Therefore datapath, memory access and register file width have to be adjusted. This inlcudes the exchange of the existing 16 bit memory moduel by a given 32 bit module. As result this exercise deepens the understanding of the microprocessor architecture and the VHDL code from the introductory session. It is the premise to get a feeling for hardware description.

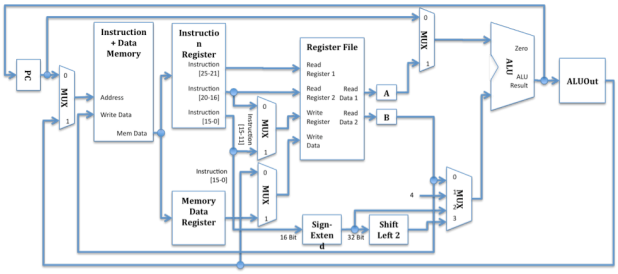

Figure 3: 32 bit MIPS processor [8] for the lab

- Verification of the developed hardware's functionality is a major part of system design to create correctly working products. As follows the students learn to verify the correct behavior of the modified core. They load a given sample binary program into the memory and simulate it. Consequently in the next step the correctness of the implemented changes can be verified by inspecting waveforms created in Mentor Modelsim [8] for the expected results. Detected malfunctions have to be interpreted to be able to make the right corrections in the code.
- Only few instructions are implemented in the given processor strictly limiting its usability. In order to create more complex programs the instruction set is extended by an additional instruction. This helps to get familiar with the structure of VHDL programming language and deepens the understanding of the MIPS processor's instruction handling. In the following the students write their own small binary program strictly sticking to the obliged format from the instruction set documentation. This program to be executed in the MIPS simulation includes the new self created instruction. From the wave forms in connection to the knowledge of the program code it can be concluded when and why certain components of the processor are active.As writing programs in binary is impractical for larger calculations the lab introduces to assembly code. First a multiplication assembly program has to be written that realizes its job by the add instruction. Loop constructs that have to be created for this task can be reused in the following. Afterward a C-code snippet of the Euclidian algorithm has to be translated to assembly code. Cross assembler and linker from open source GNU binutils [10] are used to compile a binary program from it. Both programs are run on the microprocessor. For its verification the results

can be read out from the simulation's wave forms just like for the initial binary program.

- In the following Cadence RTL Compiler [11] is used for gate level synthesis. Cadence tools' behavior is controlled by tool command language (TCL) scripts. After an explanation of the script languages basic elements the exercise is to produce a netlist of the MIPS design for an industrial TSMC 90nm standard cell library. The lab's participants are given a commented script skeleton and may use the tool's built in help to get familiar with necessary commands. They learn how to identify the maximum clock rate of their design and inspect how design size varies with increasing frequency. This allows to get into the usage of TCL scripts to control the tool's behavior, to learn the tool's commands and to get a feeling for the varying design parameters.
- Fundamental for design synthesis is the understanding of the cell library files' content. Included parameters like target temperature or the differences between worst and best case scenarios is extracted from the files and compared to each other. To achieve a better impression of technology libraries' capability the design is synthesized for 60nm and 45nm standard cell libraries as well. Results for maximum clock rate of these models give an impression of the impact of this variance. Maximum achievable frequencies increase with decreasing structure size. These experiments produce standard delay format (SDF) files describing the timing behavior of the components. In contrast to RTL level simulation of the programs in the previous tasks a gate level simulation for the design based on the timing files resulting from synthesis helps to understand how wire delays affect circuit's behavior. Previous timing free simulations worked no matter how high the clock rate had been chosen. Now with increasing frequency malfunctions can be determined.
- Upcoming of mobile devices with their limited access to power supplies make energy concerns an important design goal. According to this the circuit is inspected for its power consumption with the help of Cadence RTL compiler. First Mentor Modelsim is used to create a switching activity file for the design from the program previously created. It contains information of the amount of toggles in the processor from the input program. Afterwards it is fed into power analysis. From the resulting power report students can resolve information about how much different components of the design contribute to total power consumption. Following up the design is equipped with gated clocks and the depending power report shows how this technique reduces designs' power. Results illustrate that the applied mechanisms save up to one third of energy consumption depending on the utilized program.
- As design for test is an essential design goal RTL Compiler is used to insert scanchains. These can be used to test the final hardware after manufacturing. Cadence Encounter Test is used for automatic test pattern generation (ATPG). The resulting test patterns are input for Cadence NC-Sim and could potentially be used for a manufactured chip. A short report gives information about the amount of correct and failed test vector results.
- All previous steps were aiming at bringing the design to a stage where it could be submitted to a manufacturer. Still missing is the final step that maps the design to a GDS II file. For this reason the design eventually undergoes floorplanning, placement, clock tree synthesis and routing in Cadence SoC Encounter (Figure 4).

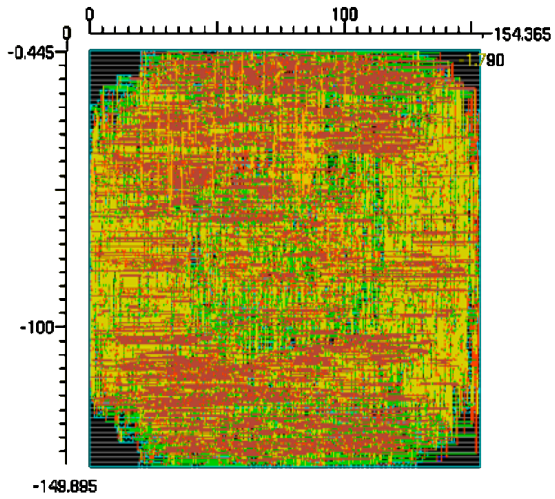

Figure 4: Routed processor from the VLSI lab

VII. Evaluation

Due to the tutorials accompanying the lectures, the supervisors are in direct contact with students solving the given exercises. Problems in the understanding of the lecture's contents can thereby be immediately identified and relieved.

Small homeworks that do not take an effort of more than 15 minutes keep the treated topics in mind and allow to monitor how well the subjects have been learned. In addition the tools' reports give a direct feedback of the participants' advances. Intensive communication during the labs allows to support the students wherever they need help.

After the last sessions an exam evaluates the learned knowledge. It contains the combined topics from lecture, tutorial and lab. Thus a successful examinee has proven knowledge in the whole system development process.

VIII. Conclusion

The tight coupling of lecture, tutorial and lab reaches a high grade of integration concerning theory and practice. Students get involved in the design flow of a complete design from the ground up. They are effectively educated in a wide range of topics. An ample understanding of the underlying principles of embedded system's circuits give the participants of this course a valuable background for their upcoming career as engineer. Efficiency is significantly improved by the tight cooperation with industrial partners.

Acknowledgment

Our thanks go to Intel Braunschweig who are sponsoring our VLSI education program. Cadence and Mentor have provided tools and licenses.

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Industrial Testing Education at Undergraduate Level: A Datasheet and Diagnosis Based Labs Approach

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Abstract—**This paper addresses industrial testing education. This work is done in the context of a French network (CNFM) which provides an access to industrial test equipment to academic people. The actual shared resource is a Verigy V93K System-on-Chip (SoC) tester platform. Undergraduate students often use digital integrated circuits (IC) in their labs and refer to the datasheet without a deep understanding of the device electrical and timing parameters. In our lab-based training, the students are guided to rediscover the role of a component datasheet, through the development of a test program. They become familiar with industrial test environment and mass production testing concepts such as test flow, test limits, parameters margins, and so on, that bonds the design, the manufacturing and the test of an integrated circuit. In addition, labs have been oriented toward the diagnosis of faulty behaviors. To do so, a fault-free circuit is first implemented into an FPGA that emulates the real circuit behavior. The design then allows configuring faulty circuits, including stuck-at faults or timing faults. Diagnosis bases are then addressed this way.**

Index Terms- Test, Testability, ATE programming, Faulty behavior, Diagnosis.

I. INTRODUCTION

This paper describes the French experience in the education of undergraduate students to industrial testing and diagnosis of integrated circuits (IC) using a lab oriented approach.

In the industry, the mass production testing is a specific environment which requires skilled technicians and engineers to handle the test equipments (tester, handler and prober) performing the automatic verification of dies on wafers and the final test of packaged parts. Technicians have key roles as they are in charge of the test equipments setup, the control of the production, the retrieve of test results and the first debug actions in case of sudden yield loss. Due to the lack of know-how and specific hardware resource in the academic environment, industrial testing is not well addressed while in the same time, microelectronic industry offers many opportunities in this field. In order to fill this gap, the National Test Resource Centre of CNFM (so-called CRTC) team has developed dedicated labs at undergraduate level that allows students to get familiar with the main concepts of production testing and equipment usage.

The CRTC has been created to respond to the industrial demand in engineering curriculum with Design & Test competences [1]. CNFM (Comité National pour la Formation en Microélectronique) is a public organization that federates academic and industrial partners for the purpose of education in Micro and Nano-electronics [2]. CNFM focuses on making heavy educational resources such as professional CAD tools, clean rooms, or industrial test equipments available for common use, by all French universities and industrial partners. Considering the huge cost of up-to-date IC testers, the policy of CNFM was to setup a single test center for all the French academic centers. So in 1998, the University of Montpellier was chosen to implement the CRTC. In 2003, after a 2-year long project, students from Europe were able to take control of the tester for remote labs [3]. The technical platform benefits from the competence of more than 25 people (researchers and professors) from a research laboratory (LIRMM, www.lirmm.fr) internationally renowned in the field of design and test of integrated circuits and systems. Research projects include DFT and BIST for digital, analog and mixed-signal circuits and design and test of integrated MEMS. Since 2006, the CRTC team includes a test engineer who manages all the technical support to users and develops training materials [4].

II. LAB ENVIRONMENT

A. Network

As CRTC first duty was to share the tester resource between different universities in France and Europe, a training environment was originally setup which allows a remote access to the test system as presented in fig. 1. In this configuration all test resources (licenses and tester) are installed in Montpellier.

As only one online session can be available at a time because of the unique hardware resource, the students work first on simulator (offline mode) and use the tester when their test program is ready for the debug session.

B. Test resources

The CRTC tester is a V93K from Verigy®. Verigy is one of the four major test equipment manufacturers in the world and is well represented in the European microelectronic industry.

Fig.2 illustrates the basic elements that compose the Automatic Test Equipment (ATE). The main part is the testhead. It can host up to 18 boards (Pin Electronics) for a maximum number of 512 digital pins (or channels) based on existing 32 channels boards. Programming is performed using a regular computer running dedicated software under Linux. The communication between the testhead and the computer is an optical GPIB link.

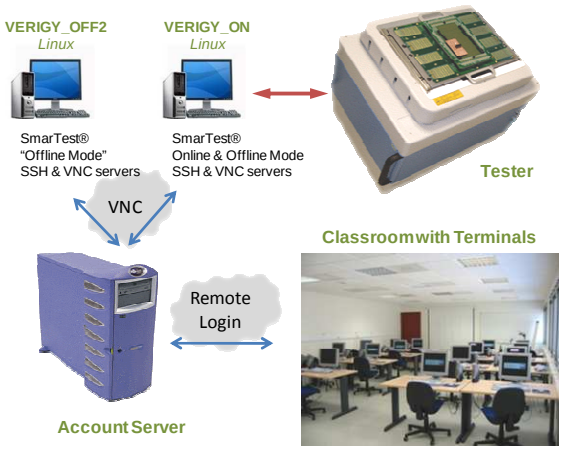

Figure 1. CRTC labs environment

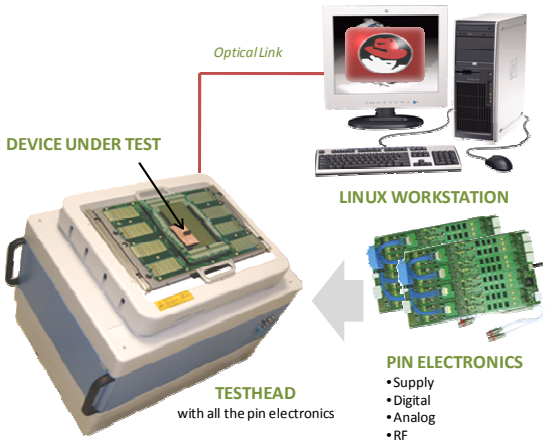

Figure 2. Industrial tester main components

VNC technology offers an easy way for the distant access to the tester. We promote this approach in the context of distant learning as the same desktop can be shared between users. This capability brings a strong interactivity between students and teacher [5]. The testhead is equipped with power pins, digital pins and mixed-signal resources as summarized in table I.

TABLE I. CTRC TESTER CONFIGURATION

Board	Ressource Type	Qty	Channels / board	Specifications
PS3600	Digital	1	32	3.6GSps / 64Mvec memory
PS800	Digital	1	32	800MSps / 64Mvec memory
AV8	Mixed-Signal	1	8	24bits / 200kSps for Audio 14bits / 65MSps for Video
MSDPS	Supply	2	8	-8V to 8V / 2A

III. LAB PROGRAM

At undergraduate level, students are using electronics components daily, and have become familiar with their data sheet without having any idea on how this latter has been constructed. One objective of the lab is to let them rediscover the role of the circuit data sheet and how its behavior and parameters are verified. As the only prerequisites to test an IC are the basics of fundamental electronics, they develop the test program to understand how electrical and timing parameters are measured using an industrial tester.

Most of the time, students are surprised when a device which works in design simulation doesn't operate properly once manufactured. They omit that the manufacturing steps are various and technically complex and can introduce defects in the ICs. So, a second objective is to initiate them to the detection and diagnosis of faulty behaviors.

A. Part 1: Study of the Datasheet

The device under test (DUT) used for the labs is a simple 8-bit shift register (74ACT299) which is in use in professional trainings for years. From the datasheet specifications, the students are guided to understand the information displayed in the different sections (DC Parameters, AC Parameters, …) and how this data relates to the test program. The operating conditions will represent the test conditions in temperatures and voltages. The device pin function and the truth table, respectively available is the datasheet are strategic data to allow the students becoming familiar with the device behavior.

In order to check the device behavior according to its truth table, the students have to create a test pattern (also called test vectors) to stimulate the chip. This test vector consists on applying signals on the inputs and on verifying if the data collected on the outputs are as expected. Doing so, they learn how to translate the information from the truth table to a test vector. Table II, shows an example of a test pattern where a '00000001' byte is first parallel loaded into the register and then 8 shifts right follow to move the '1' through all of the 8 I/Os pins. In this table, '0' and '1' represent the data applied by the tester to the device input pins, while 'H' and 'L' represent the expected device response.

TABLE II. 74ACT299 PARTIAL TEST PATTERN

	Pin	MR	CP	S0	S1	DS0	DS7	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	Q0	Q7
# Cycles	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
	2	1	1	1	0	0	0	L	**H**	L	L	L	L	L	L	L	L
	3	1	1	1	0	0	0	L	L	**H**	L	L	L	L	L	L	L
	4	1	1	1	0	0	0	L	L	L	**H**	L	L	L	L	L	L
	5	1	1	1	0	0	0	L	L	L	L	**H**	L	L	L	L	L
	6	1	1	1	0	0	0	L	L	L	L	L	**H**	L	L	L	L
	7	1	1	1	0	0	0	L	L	L	L	L	L	**H**	L	L	L
	8	1	1	1	0	0	0	L	L	L	L	L	L	L	**H**	L	**H**

In an industrial context, test vectors are automatically generated by CAD tools called ATPG (Automatic Test Pattern Generators), using an approach based on fault simulation. In this training, as the device is simple, students are requested to write a test vector themselves. It is crucial that they understand how the IC behaves before focusing on the electrical and timing parameters. Moreover, it is the logical order to develop

and execute a test program. As a matter of fact in mass production, this order allows detecting gross defaults and rejecting defective parts before performing any measurement.
Most of the time, students do not realize the importance of electrical and timing parameters in the design of circuits, in relation with process technology scatterings and the consequence regarding components compatibly when mounted on printed circuit boards (PCB). On the other hand, the definition and role of the input and output voltages (V_{il}, V_{ih}, V_{ol}, V_{oh}), the leakage currents, dynamic output and quiescent supply currents parameters are usually well understood as they use them regularly during experimentations at school. Verifying them on an industrial tester simply consists in applying the Ohm's law, i.e. forcing a current to measure a voltage and vice-versa; and programming the test equipment accordingly.
A majority of students ignore the importance of timing parameters like operating frequency, set-up time (t_{su}), hold time (t_{hd}) and propagation delay (t_{pd}) in sequential circuits. During labs, they learn the meaning of these specifications and how they can be measured on tester using a reference signal, like the master clock of the device.
Today consumer electronic products are relevant examples to help them understanding the overall relation between circuit design, manufacturing, test and these parameters. Like in mobile phone applications, the measurements of the current consumption in operating stand-by and quiescent modes allow verifying the battery duration in call and idle modes.
Once the students are comfortable with all these concepts, they are requested to extract electrical and timings information from the datasheet and to implement a suitable the test program.

B. Part II: Introduction to Indutrial Testing

The electronic resources available in the testhead are presented first: the driver that applies input signals to the DUT; the comparator that captures output signals and compares the result to the expected values specified in the test vector; and the programmable load to source or sink currents to or from the DUT. A dedicated instrument allows performing precise DC voltages and currents measurements. All these hardware resources are available for each single channel which authorizes parallel or concurrent testing. A good knowledge of the tester hardware helps the students understanding how an electrical signal is created by the combination of a voltage referring to logic state and a timing information (waveform).
Next, the software environment is introduced. The test program is developed into a dedicated tool called SmarTest®. Once, the students have defined the levels (Vil, Vih, Vol, Voh) the timings for all pins and written the test pattern, they are ready to implement a test flow with all the functional and parametric tests to be executed sequentially.
Fig. 3 illustrates the developed test flow. The strategy behind test flow implementation is addressed here.. When the result produced by a single test is "Pass", the next test in the flow is executed. Otherwise, it goes to a virtual waste basket called "bad bin" and then the program execution is stopped. Sometimes, when a test fails, another test is performed. For instance, a microprocessor device failing a 1GHz test which will be tested again and may pass a 500MHz one. The test flow ends on a "good bin" indicating that the device matches its datasheet parameters. A functional test is usually performed first, then the parametric ones (static and dynamic parameters) where the program developer has set as test conditions the values previously extracted from the datasheet.

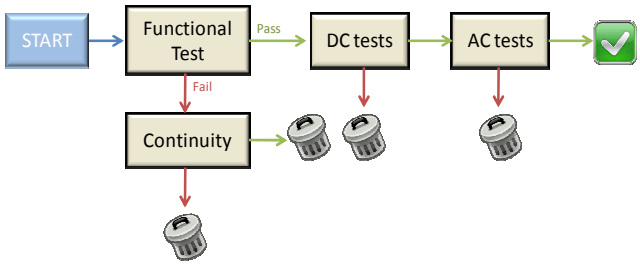

Figure 3. Example of a simple 74ACT299 Testflow

C. Part III: Analysis of Test Results

The functional test is a "go/nogo" test so that the outcome is just a "Pass" or "Fail" result. When focusing on parametric test results, it may not be straight for students to understand the meaning of the measured values. For example, the V_{il}/V_{ih} test of the 74ACT299 requires an initial setting, say 0.8V for V_{il} and 2V for V_{ih} on all inputs. The output of the characterization test provides actual V_{il} and V_{ih} values, say 1.2V and 1.4V. These values show the functional margins of the device and the robustness of the design towards the manufacturing as it means that the device still functions when 1.2V is assigned to a logic state 0 and 1.4V to a logic state 1.

Once the students get familiar with the analysis procedure using electrical parameters and the concept of margins, the timing results are analyzed. If we measure a 9.5ns propagation delay between the clock rising edge and an output of the circuit, while the datasheet specifies a delay of 12.5ns, then we can conclude that the device operates slightly faster than the guaranteed limit.. This margin improves the production yield because it accommodates some level of process shift.

D. Part IV:Initiation to Faults Detection and Diagnosis

As the device used for the training is obviously a good one, it is not possible to confront the students with failing behavior. Our approach was to implement a gate-level copy of the circuit into an FPGA that can be altered to inject either stuck-at faults (node stuck at '0' or '1' logic state, or extra delays) to emulate real failures.
The 74ACT299 device has been coded into a structural VHDL module that represents the very same circuitry as the original integrated circuit. Additional lines and gates have been inserted allowing the configuration of faulty behaviors…

The targeted FPGA is a Xilinx xx available on Digilent Nexys development board. In our setup, the FPGA I/Os are directly connected to the ATE channels, while the Nexys board is

externally supplied (see Fig. 4). The development board features switches, buttons and a 4 digits 7-segments display that have been used to develop a simple user interface that allow the teacher to easily select the operating mode or the emulated circuit (fault-free mode, stuck-at fault mode, or delay fault mode). Due to the limited number of switches, a reduced number of nodes have been selected to insert stuck-at faults and additional propagation delays. Delays are also selectable in a range from 3ns to 40ns. The choice of the node for fault injection has been made allowing various diagnosis difficulty levels.

Figure 4. The Interface board and FPGA board connected to the testhead.

From educational point view, this approach is very efficient as it allows the teacher to introduce various faults in the device at different times without the need of reprogramming the FPGA.

In the last part of the labs, the students face faulty behaviors and they learn how to develop a diagnosis strategy.

The training starts with an easy stuck-at fault case and goes crescendo. The students use the "pattern debugger" tool to visualize the failing vector cycles and failing output pins (fig. 6).Other investigation tools such as the "timing diagram" which provides the chronograms of the signals on all pins are also used. The type of fault may be assumed based on simple observations available in the pattern debugger… For instance, if only high states (H) or low states (L) fail, the failure is probably a stuck-at fault. If both high and low states fail, the failure may be a delay one. Next, we focus on identifying the failing pin. Here, we need to make assumptions and check if the combination of the defect and selected pin produced all the failures displayed in the test vector. The students are not used to this exercise but the outcome is an overall understanding of a product life cycle (design, manufacturing and test).

This exercise may be organized as a game: one student introduces a defect in the circuit from the FPGA board and the others have to apply the diagnosis procedure to identify the pin and the fault. If they are unsuccessful, the student may help them by providing some clues.

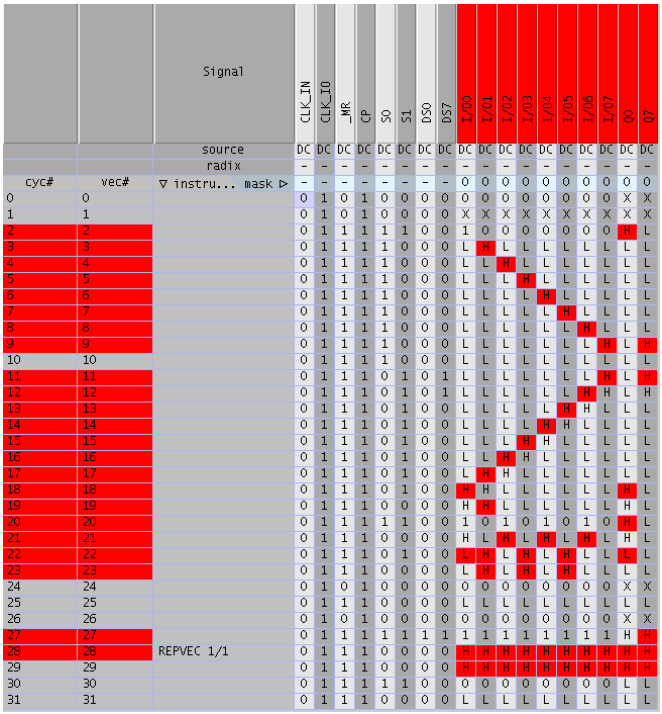

Figure 5. Example test vector failures

IV. CONCLUSION

This paper details an experience in the field of industrial testing education for undergraduate students. During 8 hours lab, the students acquire a global knowledge and know-how regarding the verification of integrated circuits and then better understand the interactions between design, manufacturing and test. An approach to insert faulty behavior in an FPGA-emulated device has been developed to support training on diagnosis strategies.

ACKNOWLEDGMENT

The authors wish to thank the Région Languedoc Roussillon for its continuous support to CRTC projects. Since CRTC creation in 1998, Verigy (formerly Hewlett-Packard and Agilent) has always been a strong partner. This work is also supported by CNFM and University Montpellier II.

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SAME goes back to school

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Abstract— This project, carried out by the SAME association [1], is the result of several observations. Indeed, the PACA region is a business and research cluster in the field of communicating secured solutions where microelectronics is at the heart of these solutions. Nevertheless, we do not build a world-class centre of excellence without strong local support of the population. Unlike other areas such as the Silicon Valley, the French Riviera has not gotten a high-tech culture. The majority of engineers recruited in the companies member of SAME come from other regions or other countries. It is thus imperative that we take action at the origin and encourage our children and high school students to become engineers. In a general manner, young people give up too often on the scientific academic fields which are supposed to be difficult.

I. INTRODUCTION

Facing this reality, a promotional kit (presentation of engineering careers in general and microelectronics engineers in particular) was developed in 2007 by two students from the electronics department at Polytech'Nice-Sophia, as part of their internships, supervised by SAME engineers and a university professor. The idea of this kit is to break away from the stereotypes of the engineering career that is often unknown. Young people have an image of an austere person in a white blouse at the back of the laboratory. The courses, in particular the preparatory classes to «Grandes Ecoles», are intimidating. This kit presentation, in a « PowerPoint » document (see Figure 1), lasts about one hour. It is carried out, in theory, jointly by a professor and an engineer from Sophia, which will demystify the engineering career and show the different aspects as well as the different possible ways to achieve them.

Figure 1. Kit « Same goes back to school »

II. ENGINEERING CAREER

This presentation is fairly interactive and its aim is to make high school students react as much as possible. It begins by showing the different roles which an engineer can perform in the course of his career and of the different technical fields covered (see Figure 2).

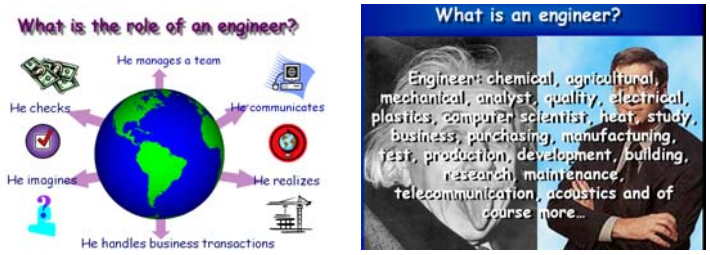

Figure 2. Engineering roles and careers

We will indeed show that an engineer's work is not limited only to the scientific field and most of all; it can be constantly changing, in the same way as his salary (see Figure 3)! All questions are welcome.

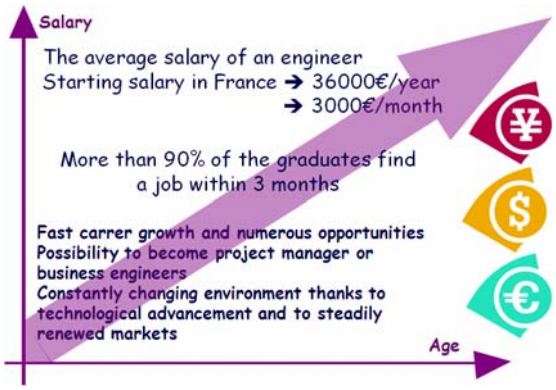

Figure 3. Career opportunities and salaries

III. MICROELECTRONICS ENGINEER

When the high school students have run out of questions, we continue the presentation more specifically on the microelectronics engineering career. Wafers, dies, packaged dies and above all "open" iPods, passed around in the classrooms show us just how far electronics have invaded our daily life. It is important to show that Europe remains a significant international cluster, particularly in the field of

design (see Figure 4). In general, high school students are not aware of the system of business and research clusters which have been put into place in France. We now give a brief description of the concept by presenting the local industries.

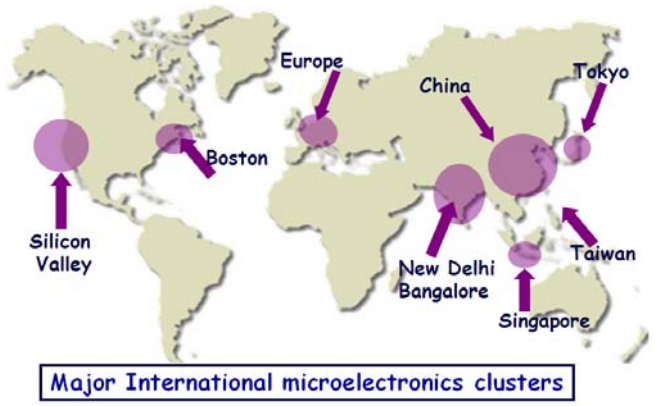

Figure 4. International clusters

A trip into the heart of the iPod (see Figure 5), which is a familiar object to high school students, illustrates the constant and fast-growing evolution of the microelectronics industry. We then show how several teams of engineers (sound, acoustics, computer, telecommunications, physics, electronics) have enabled a user to legally download his favourite piece of music from the studio recording of a rock group, rap or R & B so that he can listen to it on his iPod. Next, we convey the evolution of microelectronics technology through the different iPod (and iPhone) versions as shown in figure 6.

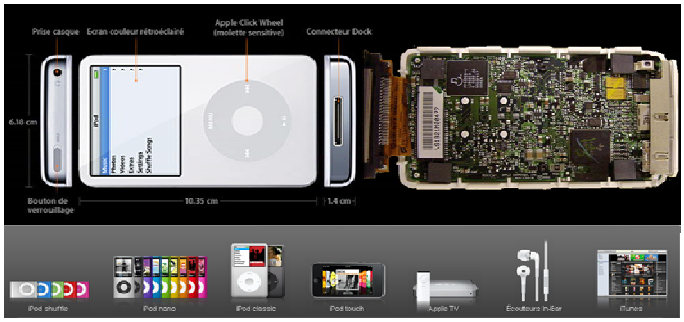

Figure 5. A trip into the heart of the iPod

Figure 6. Evolution of the iPod – The different generations

Scaling is made possible thanks to the invention of transistors which is the fundamental basis of the microchip. A microchip includes millions of transistors and can perform many more or less complex functions. If we apply the same miniaturization-performance rates to an automobile, a car today would measure 3 cm and would be able to go up to a maximum speed of 3000 km/h.

As compared to the Pyramids which total about 2.3 million stones each one, a microchip contains more than 100 million (or a few billions) transistors. To design a modern microchip, a team of dozens even hundreds of engineers is required. Unlike the thousands of slaves who built the Pyramids, engineers receive quite a high salary in exchange for their work. To reach such a density of integration, the size of the transistor over the course of the years has diminished, being divided by 1.4 every 18 months. The size today is inferior to that of a virus (see Figure 7).

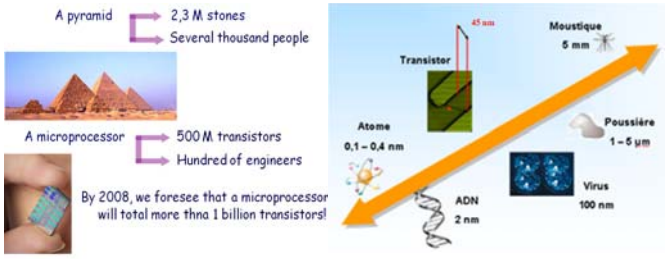

Figure 7. Microchip complexity and Comparison of a transistor size

Let us simplify by showing how a transistor can operate as a control switch and how it also constitutes the fundamental basis of digital electronics (see Figure 8). To be more precise without discouraging the high school students, we also show two videos (see Figure 9): one - an extract from the French TV show ”C’est pas sorcier” [2] and the other - a DVD directed by EDA Centrum about EDA tools and on networking problems [3].

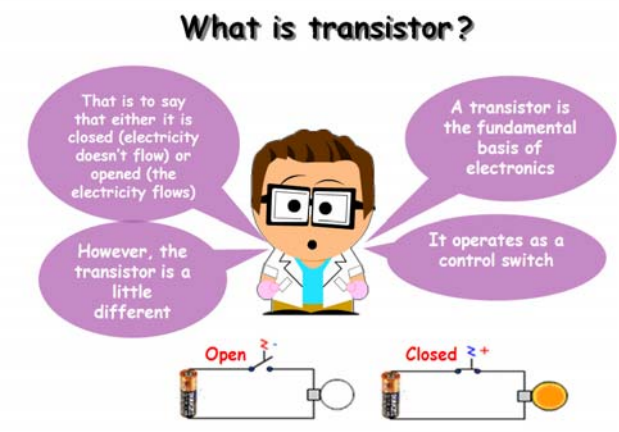

Figure 8. The transistor is the fundamental basis of digital electronics

Figure 9. Extracts from the videos shown to the high school students

IV. TRAINING ENGINEER

To conclude our presentation, we show the different possibilities available to students who wish to obtain an Engineering or a Master's degree: preparatory classes to the «Grandes Ecoles», integrated preparatory classes, universities and Institutes of Technology (see Figure 10).

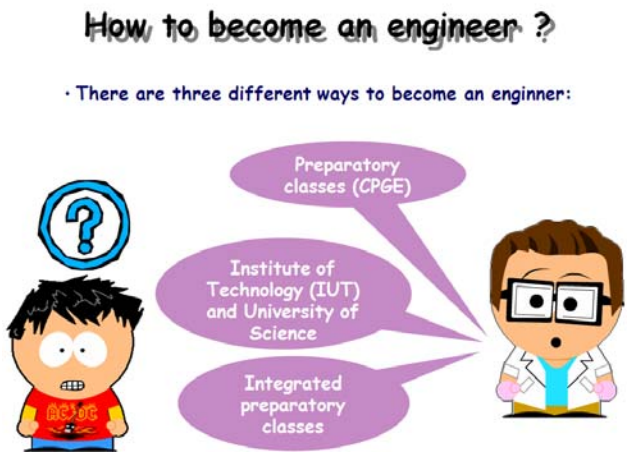

Figure 10. Three different ways to become an engineer

As high school students are not so familiar with networks such as Polytech, they usually ask a lot of information about "undergraduate programs". Questions on the practical details of admission, graduating to the next year and on the work load are asked quite often! The specifics of one type of training in comparison to another, particularly in the Social Sciences, as well as foreign languages are often questions which come up during the final discussion.

Young people today are truly interested in international experiences and the possibility to do part of their studies abroad. It is necessary to recognize that we should likewise put them at ease about the hypothetical difficulty in our academic courses.

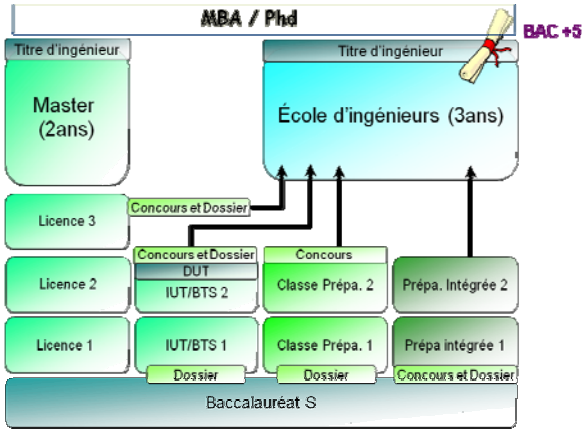

Figure 11. Different options of training to obtain an Engineering or Master's degree

The targeted public is high school students in their senior year or those preparing a French "Baccalaurat Terminale S" as well as those preparing a degree in Science, Technology and Industry. Throughout the school year 2007-2008, several presentations were done in high schools in the Alpes Maritimes Region, generally given by a team of engineer-professor (see Figure 10). The presentation is shown to students in their senior year at the beginning of the first term just before they need to make their final choice of studies for university.

At the end of the presentation, we hand out a questionnaire to each student about the presentation, their perception of engineering careers and their interest in the scientific fields. The first feedback received is encouraging because a significant ratio of high school students indicates that this presentation has changed their view on engineering careers:

- all of them found it interesting, but too short
- a lot of them asked for more information «integrated preparatory classes» schools

At the end of the presentation, a quiz to win an iPod is also given. A winner is drawn each year (second time in 2008) and his prize is given at the closing ceremony at the SAME forum.

VI. CONCLUSION

This is a long-term process. The impact on the culture of the French Riviera and on the ratio of natives from the French Riviera in engineering schools is measured on long-term. The next step would be to extend this project to other regions as part of economy awareness. All documents can be turned in free of charge to all colleagues in the CNFM network. We would simply expect that they hand in all modifications, a summary of their use and presentations in front of high school students.

This project is a trial balloon. SAME has not gotten the financial means or the manpower to reach out to all the high schools or the high school students of France. Our goal is to work with other associations which will relay our project in their technical and geographical fields. It is possible for us to organize training sessions of « trainers ». In the future, we would like to reach out to 15-year-olds (French school system- «3ème»), combining the presentation with mandatory internships in companies. We would also like to produce a film focusing on the main points of the presentation with a concentration on the regional employment pool.

This project will become a « success story » when we succeed in having a crowd of students, who have been partly persuaded by our presentation, enrolling in our engineering schools. Henceforth, we would like it to be known that this project was awarded, on a European level, second prize in the category « Investment in Education » which was sponsored by the journal « Electronics KTN » (see Figure 12).

Figure 12. Second prize (European finalist)

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Teaching Analog Design Concepts in Deep Submicrometric Technologies.

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Abstract—**In order to perform hand calculations in an analog design, the technological parameters involved in the square law equations of the MOSFET must be known for different widths and lengths, for both *n* and *p* transistors. Extracting this information from an advanced model such as BSIM4 is not a simple matter for the novel designer or under graduated student. This paper proposes the use of electric simulation combined with MATLAB functions to extract the required parameters for a first cut design.**

Keywords.- Education; Analog Design; Parameter Extraction; MOSFET Models.

I. INTRODUCTION

The electronic design is an iterative process. This task starts with a set of specifications, which are mapped into an electronic system aimed to meet the initial requirements. Simulation is used to verify the validity of the proposed design concerning the given needs. Analog circuit design uses a set of equations mainly based in the so called "square law model" to accomplish the mentioned mapping. Those equations proposed by Sah in 1962 [1] are simply and easy to use. These equations are also known as Level 1 model within SPICE. They give a first estimation of the transistor sizes in developing a basic building block such as a voltage comparator or an operational amplifier. However this model functions well for transistors with long channel length (*L*) and wide width (*W*) [2]. As technology improves and smaller transistors are being fabricated, advanced models for simulation in SPICE-like programs have been developed, for instance, the BSIM4 model is very popular for simulation of nano-metric devices [3]. This model includes, among others, the effects of velocity saturation present in deep sub-micrometric devices, which are neglected by the Sah model. This fact brings a consequent mismatch of more than 100%, if the size of a transistor is calculated to meet certain transconductance or output resistance requirement using the Level 1 model and simulating using the BSIM4 model [4]. This situation is quite confusing for students or novel designers when being introduced into the world of analog design with current technologies having an *L* under one micron, since the student does not feel, that she or he has "control" over the design. This circumstance brings besides confusion, frustration and a tendency to use the simulator as a "magic box" to obtain aspect ratios of transistors by means of parametric analysis changing *W* and *L* arbitrarily until the needs are found. This method does not give any feeling nor insight of the circuit under design and in many cases the students end the course with the wrong believe, that analog circuit design does not have an accurate approach more than trial and error. In this paper, a method to extract the parameters needed by the Level 1 model from electric simulations performed in SPICE is presented. Here, while in an electric simulator the BSIM4 model for nano-metric devices is used, functions of MATLAB are handled to find out the values of the square law model parameters. Sah model parameters are important because, although the majority of the literature concerned with CMOS analog circuit design includes a chapter regarding sub-micrometric devices [4,5,6] uses the simple model to derive the behavior equations of both the transistors and basic building blocks typical of analog systems. Therefore, Level 1-based equations are the starting point to perform hand calculations in analog circuit design. The presented approach has been used with success, last year in analog circuit design courses in two universities in Mexico. The paper is organized as follows: Next section presents an overview of the courses organization, after that, the proposed approach is presented in detail. Section 4 shows a basic building block designed by students who attended the course, using the information found in section 3. Finally some conclusions are given.

II. COURSES OVERVIEW.

The courses in both universities were organized in 12 weeks, six hours per week. They comprised the typical themes of a basic Analog CMOS Circuit Design course, namely, MOS transistors, Single Stage Amplifiers and Differential Amplifiers, two topics were included: Short Channel Effects and Technology Characterization, The course structure was the following:

- Introduction
- MOS transistors and Models
- Short Channel Effects
- Technology Characterization
- Single Stage Amplifiers
- Differential Amplifiers

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They only comprised electric design, no layout aspects were covered, since they are left for a second course.

III. Extracting Sah's Model parameters in Matlab from Electric Simulations

A. The Square Law Model

The well known simple model relating the drain current and the applied voltage between gate and source in a MOSFET, when operating in its linear region, is given by:

$$i_D = \frac{K'_{LIN} W}{L}\left[\left(v_{GS} - V_T\right) - \frac{v_{DS}}{2}\right] v_{DS}\left(1 + \lambda v_{DS}\right) \quad (1)$$

The parameters involved in this equation are defined as follows:

K'_{LIN}.- Intrinsic transconductance parameter in the linear region.

V_T.- Threshold voltage of the device.

λ.- Channel length modulation parameter.

The quantities v_{GS} and v_{DS} are the voltages applied between gate and source and drain to source respectively. This region of operation finds limited application in CMOS analog circuit design as for example in a voltage controlled resistor. Of more interest is the saturation region, in which eq. (1) becomes:

$$i_D = \frac{K'_{SAT} W}{2L}\left(v_{GS} - V_T\right)^2\left(1 + \lambda v_{DS}\right) \quad (2)$$

Here, K'_{SAT} is the intrinsic transconductance parameter in saturation, which is usually smaller than K'_{LIN}. Since a bulk to source voltage (v_{SB}) usually appears in stacked devices, in the simple model V_T is defined as follows:

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right] \quad (3)$$

Where, γ is the bulk threshold parameter and ϕ_F the strong inversion surface potential. As it will be shown γ is easily found and can be used to estimate V_T in a cascode-connected device. From eq. (2), the small signal transconductance and output resistance are derived as:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{K'_{SAT} W}{L}\left(v_{GS} - V_T\right) \quad (4)$$

$$r_O = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1} = \frac{1}{\lambda i_D} \quad (5)$$

These last equations reflect the importance of having values of K'_{SAT}, V_T, λ and γ to calculate the aspect ratio of a transistor which has to meet certain g_m or r_O. However, due to short and narrow channel effects present in deep submicrometirc devices, the value of the mentioned parameters is dimension dependent. For this reason it is necessary to do several simulations for the different channel dimensions prospective to be used thorough the designs.

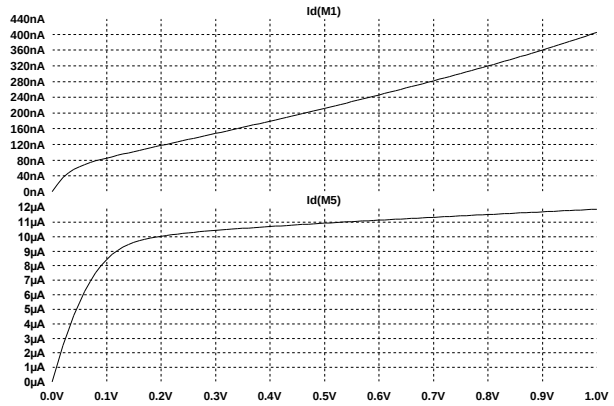

Figure 1. I_D-V_{DS} Curves of MOS transistors with aspect ratio of 3 and L=100nm (up) and L=2μm (down).

B. Electric Simulations

Figure 1 shows the simulated response of the drain current of two MOS transistors, both having a W/L=3 but one with L=100nm and the other with L=2μm. In these simulations, the BSIM4 model of the IBM 9RF technology with feature size of 90nm available through MOSIS were used [7]. From this curve K'_{LIN} and λ can be determined once the (v_{GS}- V_T) quantity, also known as over drive voltage (V_{OV}) has been chosen [2]. Figure 2 shows the so called transconductance characteristic of the MOSFET for different values of v_{SB}, from them, K'_{SAT}, V_T and γ will be obtained. Again, the response of large and short channel devices is plotted.

C. Parameter Extraction through MATLAB

Now, enough data to be used for the estimation of the above mentioned parameters has been collected. If the *i-v* data got in the simulations are exported in a text file, they can be used to apply numerical techniques such as linear regression in order to compute, with in certain error margin, the value of the searched quantities.

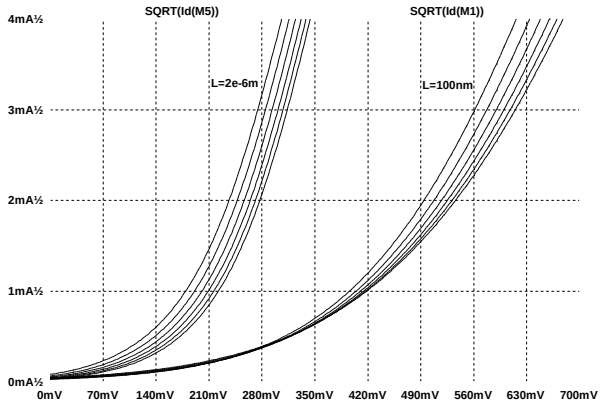

Figure 2. Transconductance characteristic for short and long channel devices.

At this point, any programming language such as "*C*" could be used, but for simplicity, the *MATLAB* program was chosen, since an easy and quick way to determine the information in question was seek, besides, the objective was to have values of the parameters suited to start hand calculations in a required design, not to exercise programming techniques or numeric methods. As known, *MATLAB* has an extended library of functions to perform linear regression and curve fit. The function `polyfit` [8] acts over a data set and returns the coefficients of a polynomial of order *n* which best fits the given function. For instance, the following code lines take the data stored in the vectors `id` and `vds` and approximate their relation with a polynomial function of order one (a straight line) the resulting coefficients are stored in the vector `coef`:

```
coef=polyfit(id, vds, 1)
m=coef(1,1) % slope
b=coef(1,2) % y-intercept
```

If the vector `id` contains the drain current data in the saturation region, the value of the parameter λ is obtained by dividing `m` by `b` as indicated in the chapter 4 of [2]. This approach was used taken as input vectors the *i-v* pairs obtained in electric simulations. A simple program in *MATLAB* was written by the students in order to organize the information into the regions of interest, i. e.: drain current in linear region, drain current in saturation and so on, for the different chosen transistors. The mentioned function was applied to the input vectors and the resulting coefficients were used to obtain the desired values. Finally the information was organized into tables. Figure 3 shows some of the results for K'_{SAT}, and V_T of a short channel device.

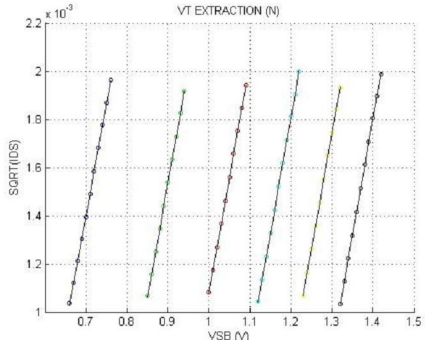

Figure 3. Simulation Data and Fit Line obtained in MATLAB for NMOS Transistors.

IV. Case Study of a Design: The Flipped Voltage Follower

As a case study, the electric design of a voltage follower using the topology proposed in [9] was carried out by the students at the end of the course. The schematic diagram of this circuit is depicted in figure 4.

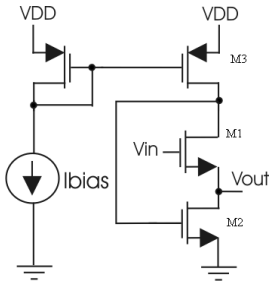

Figure 4. A Flipped Voltage Follower.

This circuit acts as a non inverting voltage follower well suited for low voltage applications. It has almost unitary voltage gain and an output resistance given by

$$r_{OUT} = \frac{2}{g_{m1} g_{m2} r_{O1}} \tag{6}$$

With the parameter values found and collected in table 1 for NMOS transistors, a flipped voltage follower was designed to have a voltage gain of one and to drive a capacitive load (C_L) of 0.5pF at 100MHz. This load capacitance requirement was chosen in order to preserve stability of the circuit following the condition:

$$\frac{C_L}{C_{DM3}} < \frac{g_{m1}}{4 g_{m2}} \tag{7}$$

Where, C_{DM3} is the capacitance seen from the drain of M3 to ground. Figures 5 and 6 are showing the simulated results of the DC transfer curve of the circuit and its transient response respectively. Recall that electric simulations were done using the BSIM4 model of the IBM 9RF technology and 1V of power supply. A similar characterization work for PMOS transistors was done, although it is not reported here.

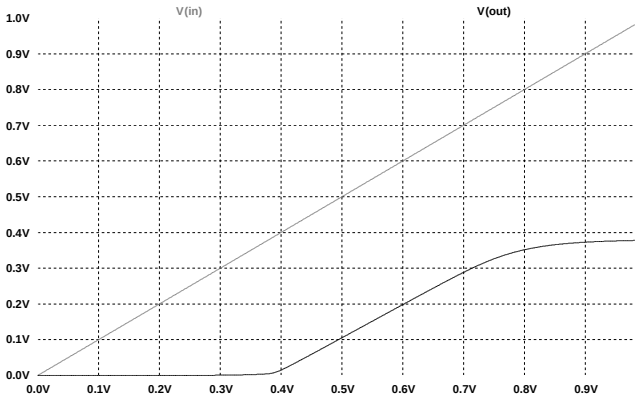

Figure 5. DC transfer response of the designed flipped voltage follower.

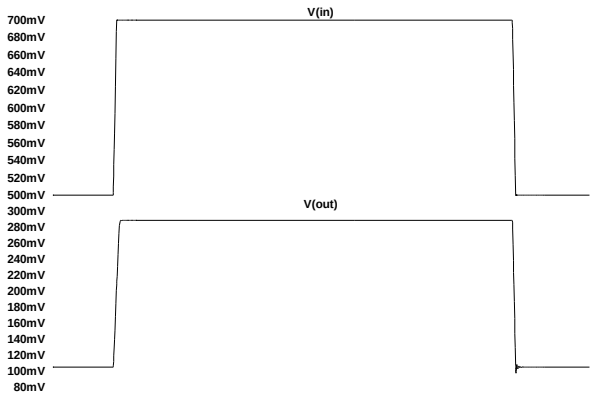

Figure 6. Transient response of the designed flipped voltage follower at 80MHz with a C_L=0.5pF.

TABLE I. ESTIMATED PARAMETER VALUES FOR NMOS TRANSISTORS

W/L	K_{LIN} (A/V^2)	K_{SAT} (A/V^2)	V_T (V)	λ (V^{-1})	γ ($V^{1/2}$)
10μm/1μm	$3.96x10^{-4}$	$766x10^{-6}$	$205x10^{-3}$	0.1	0.41
200nm/2μm	$9.63x10^{-3}$	$535x10^{-6}$	$330x10^{-3}$	1.12	0.42

V. CONCLUSIONS

An easy and comprehensive method to extract the technological parameters in a deep submicrometric technologic process was presented. The so obtained results are useful in order to have a starting point when a basic building block is going to be designed and the equations describing the circuit characteristics were derived using the MOS simple model. The student or novel designer should always first characterize the technology in use in a similar way before starting to carry out any design, otherwise, large errors in the hand calculations will be obtained and any insight in the designed circuit will be gained. The proposed methodology has been used to teach analog circuit design concepts in post-graduate courses, using advanced MOS models for the electric simulation of deep submicrometric devices. Obtaining in such a way the values of the quantities involved in the square law MOSFET model is a very constructive experience and gives to students a good comprehension of the operation of MOS transistors.

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Teaching Cognitive-Inspired Design of Sequential Circuits

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***Abstract*— The paper deals with a cognitive-inspired design of digital systems. Specifically we discuses a new approach for teaching of sequential circuits (SC) design. The approach is based on using Split Algorithmic State Machines (ASM) for initial specification of SC. We analyze both the complexity of the Split ASMs and the quality the corresponding hardware solutions. The proposed approach was implemented and studied in an undergraduate Computer Engineering class. The results of our study demonstrate that the proposed approach improves both the students' success in solving design tasks and the debagability and testability of resulting schemes.**

Keywords- sequential circuit, algorithmic state machine, cognitive template.

I. INTRODUCTION

The present paper belongs to the field of digital design education. Specifically we deal with teaching sequential circuits (SC) design. A process of design/synthesis of SCs comprises a sequence of initial specification transformations for obtaining an optimized circuit according to design constraints (speed, area, power dissipation etc.). In the paper we demonstrate on the deep interrelations between the initial specification of the SC and its hardware implementation. Our approach is based on two hypotheses:

1) an initial specification of any SC is strongly affected by the cognitive style of the designer;

2) a logic circuit inheriting a structure of its initial specification is more understandable and debugable than a regular circuit that doesn't inherit the initial structure.

Various representations of SCs, as well as various hardware description languages are well studied. Usually, a SC is implemented in optimized form that is quite far from the initial specification. This gap between the initial specification and implementation is well grounded if the main design concern is the implementation cost. When debugability and understandability factors become dominant, the gap becomes questionable. Moreover, the human-machine interaction on the system level of design becomes more "user-oriented", while the implementation level of the design becomes more distinct from the system level, and thus, complex to be managed. In general, this gap characterizes the technology progress in the modern society. However, the common sense and the basic technological orientation being successful in the every-day life, is not always applicable for developing digital systems and, especially, for teaching logic design.

From our teaching experience, we came to conclusion that standard automation tools are not suitable for teaching logic design due to their user-orientation and not the implementation orientation.

The majority of SC initial specifications is developed by humans and, as a result, inherits some humans' thinking templates. Actually, the thinking templates usually have a tree-like structure and, fortunately, may be formalized. We consider a specific cognitive style − dichotomic networks − as a class of representations, that correspond to a particular specification of SCs. Dichotomic networks comprise so-called dichotomic fragments [2]. We refer to dichotomic fragments as binary trees; dichotomic networks are referred to as systems of interconnected fragments. An important example of a dichotomic representation of SC is an Algorithmic State Machine (ASM) chart. Development of the ASM chart requires thinking in terms of ASM paths, each corresponding to a specific Boolean cube. The entire ASM chart forms a single dichotomic fragment. The ASM specification is natural, logical, and testable, but it requires bearing in mind all possible logical paths (situations) and referring to them within the system. This strict requirement renders the ASM specification logical and testable, however, it puts designers in a position where they have to define very sophisticated and even artificial/unexpected states of the system.

When the number of variables grows, the process of defining an ASM specification becomes difficult and even unnatural. Whereas Hardware Description Languages (HDLs) allow a system specification in a natural way (split representations), the majority of the existing VLSI CAD synthesis tools are still based on the conventional SC representation. As a result, the solutions tend to be non-understandable and non-debugable. The main subject of our study is a newly introduced Split ASM having all the advantages of a conventional ASM but free of the above drawbacks. A SC can be defined both as a single ASM and by a network of ASMs of low complexity. The trade-off between these two extreme cases is of a special interest. This trade-off as well as the size of the ASM fragments and the structure of

their interconnection within the Split ASM is subjects of our study. It is known that when people are given a problem for which there exists a correct solution and an initial estimate of that solution, they tend to provide a final estimate close to the initial one. This is termed anchoring. Anchoring heuristics help humans simplify problem solving in complex situations without conscious effort. In our work, we apply the anchoring heuristic principle to teaching SC design. We consider the initial specification of SC as an initial estimate of the design solution. Since the entire design process is a sequence of equivalent transformations between various representations of the same SC, each of the representations may consider a certain implementation of the system. Thus, the initial specification is also a kind of implementation. If the initial specification is considered an anchor, then the design problem can be solved by using the anchoring and adjustment heuristics algorithm. In contrast to conventional teaching methods, we synthesize a SC directly from its initial specification. Circuits produced by the anchoring synthesis may have an additional overhead in comparison to circuits produced by the conventional optimization method. Nevertheless, we consider this a reasonable price for such an important property as debug-ability and readability of the SC. Moreover, we show that a relatively small overhead is required for the proposed approach.

The present work presents:

- A study of dichotomic networks as cognitive basis for specification of SCs.
- A study of the efficiency of teaching SCs defined in Split ASM form.

We show that use of Split ASM notation and dichotomic cognitive templates allows design of SCs in a very efficient way. Circuits designed by students according to the proposed approach are understandable and debugable. The proposed approach allows increasing a size and complexity of SCs that can be handled by students.

II. SPLIT ASM

A design process transforms a set of specifications into an implementation of the specifications. Both the specification and the implementation are forms of description of the system functionality, but they have different levels of abstraction. Given the behavioral description of the system's (observed or desired) functionality, from the formal model stage onwards, we distinguish between two main paradigms: the procedural (algorithmic) paradigm and the declarative paradigm [1,3].

According to the declarative paradigm, the person (e.g., student, user, designer) defines the structure of the system by focusing on the logical scheme of the SC. In contrast, according to the procedural paradigm the user focuses on the behavior of the system.

In our study, we deal with the most popular paradigm - the procedural paradigm. The main formal construct for the procedural paradigm is the ASM chart. The ASM chart is a directed connected graph comprising an initial vertex, a final vertex, a finite set of operator vertices, and conditional vertices [4]. Each conditional vertex contains a single logical condition from a set of input variables (x's) of the SC. Each operator vertex contains a specific output vector (Y) from the set of output signals of the SC.

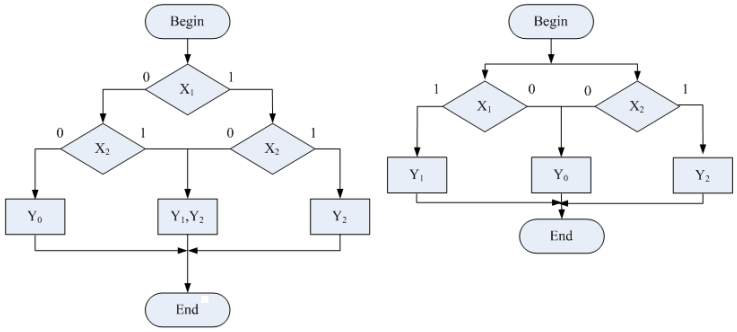
We define the Split ASM by connecting a number of conventional ASMs (component ASMs) as follows:

1) Parallel connection: connecting roots of two or more components ASMs.

2) Sequential connection: replacing one terminal node of an ASM with another ASM.

These component ASMs (sub-graphs in to Split ASM) correspond to dichotomic fragments. The output vectors of each of the fragments are logically summed.

Fig. 1 illustrates the ASM and Split-ASM descriptions of the same SC that controls two-axis manipulator having two inputs and two outputs variables, which form 3 types of output patterns.



a) b)

Figure 1. Example of a SC representation by ASM (a) and Split ASM (b).

Clearly, an ASM is very suitable form of the initial specification [2]. Nevertheless, it has a significant cognitive contradiction. On one hand, the ASM corresponds to a classical von Neumann's architecture that is based on the sequential, step-by-step execution of the algorithm. On the other hand, on the hardware level, the behavior of the ASM is concurrent. Furthermore, the ASM description includes a significant redundancy, associated with its tree-like nature. One of the main requirements for a modern systems' specification is its ability to support the concurrency.

The proposed paradigm allows combining advantages of both considered paradigms: the declarative and the procedural. Each sub-graph of Split ASM is the usual ASM, allowing the use of the existing design methodology. At the same time, communication sub-graphs allow to trace the structure of the described system. Our assumption of necessity of the initial specification and the final description conformity, finds the acknowledgement in the proposed paradigm. In additional, the Split ASM specification is therefore much more natural. It

corresponds to human cognitive patterns to present a complex entity as an assembly of simpler components.

Our study combines methods both from cognitive science and from computer science. Namely, we reveal the mental representations people have for a given domain and the visual devices they use to convey it, and at the same time, we create effective hardware, which inherits the cognitive style of the designer.

The cognitive theory presented in [6] formulates a number of principles and understandings about human learning. Human memory has two channels for processing information: visual and auditory.

- Human memory has a limited capacity for processing information.
- Learning occurs by active processing in the memory system.

The proposed Split ASM fulfils the above principles; it has a graphical representation, each separated component ASM includes a smaller number of variables (i.e. reduction of complexity). Moreover, since the working memory has a limited capacity [5], the task of designing a SC becomes more difficult and complicated as the number of input-variables increase. The Split ASM allows to reduce the number of variables and hence to use efficiently the short-term memory.

III. EXPERIMENTS

The experiments included eight SC design tasks (Berger counter design, 1-hot code controller and standards benchmarks designs [7]). A group of 43 undergraduate Computer Engineering students were asked to define appropriate ASMs, both in the conventional and in the split form. The resulting designs were compared in terms of their quality and the design time. Additionally, in order to compare the understandability of the two schemes, the students were asked to perform reverse engineering and to find out the functionality that a given ASM represents.

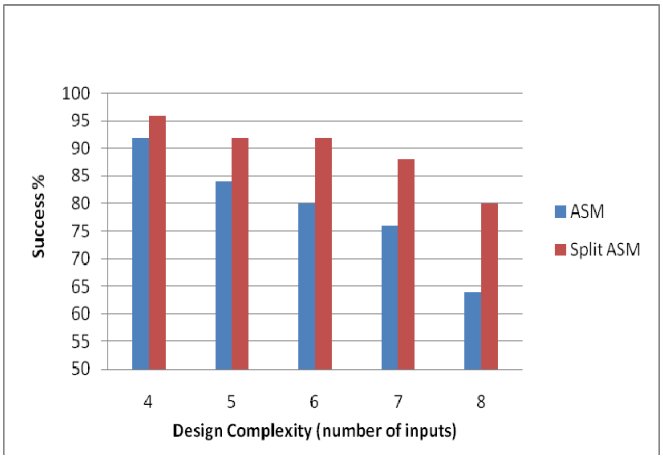


Figure 2. Average success in completion of design tasks.

The comparison between the two representations indicates that:

1) the Split ASM has a shorter average path length than the corresponding conventional ASM and a smaller number of vertices;

2) the Split-ASM is preferable from of the point of the hardware overhead – the Split ASM provides about 20% reduction in the number of gates.

Let a success in solving a given task be the completion of the design in a given time. Fig. 2 shows the relation between the success and the number of input variables for both ASM forms.

A review of the designs and interviews of the students indicate that the majority of students preferred to work with a Split ASM due to its simplicity and efficiency when the number of input variables has increased. Fig. 3 demonstrates this observation.

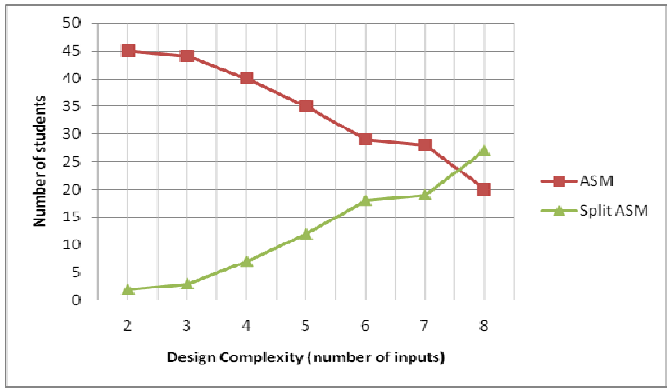


Figure 3. The distribution of the design paradigms as a function of the number of input variables.

As can be seen from Fig. 3, the number of input variables - 7, is the threshold, after which the migration from ASM to Split ASM is inescapable. Our result is well correlated with the known fact that the depth of short-term memory is 7±2 items input (variables input variables in our case) [9].

Fig. 4 shows the relationship between the number of components in Split ASM and the number of input variables.

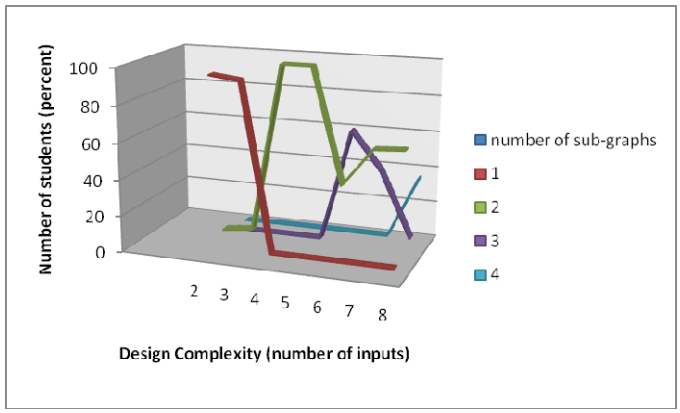


Figure 4. Number of components versus design complexity.

For evaluation of design mental complexity [10] and comparison between ASM and Split ASM, we introduce a

new complexity criterion so called a rectangle of complexity: a product of the Split ASM components number and the average path length. Experiments show that for each initial specification this new criterion in most cases remains constant and does not depend on number of components.

To demonstrate the understandability property of the Split-ASM, we performed an additional experiment in a group of 14 students. The students were asked to find the proper specification of a given implementation, i.e., to perform a reverse engineering. The success rate in performing a correct reverse engineering of a Split-ASM was 70%, while for conventional ASM the success rate was 50%.

IV. CONCLUSIONS

We presented a new approach for teaching SC design. The approach is based on the cognitive-inspired Split-ASM notation. Circuits designed by students according to this approach were found to be more understandable and debugable than the conventional designs. Moreover, the proposed approach allows increasing a size and complexity of SCs that can be handled by students. The effectiveness of the approach was examined on a number of design tasks. The new approach gives a more adequate idea about the digital system's behavior. We believe that the Split ASM approach has good future perspectives in digital design teaching.

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Microelectronics education at MIEM: from materials to system on chip/board.

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ABSTRACT

A continuous microelectronics education system has been developed at MIEM. The approach provides all microelectronic products design stages learning and is based on close software/hardware relations and wide collaboration with industry enterprises during education process. The microelectronic products design stages studied inside the microelectronics educational program are considered.

1. INTRODUCTION

The Moscow State Institute of Electronics and Mathematics (technical university) (MIEM) is one of the leading Russian universities in preparing engineers and researchers for electronic and especially for microelectronic industries.

According to industry requirements and in collaboration with the industry enterprises the special microelectronics educational program for students and industry engineers has been developed at MIEM.

This microelectronics program has more than twenty years history and it is regularly corrected and gets additional elements and materials according to microelectronics trends.

The experience of microelectronic industry showed that to provide qualified educations in this area it is necessary to give students deep understanding and experience in all aspects of microelectronic products design: from semiconductor materials, throughout devices and circuits to VLSI, SoC, FPGA, PCB design.

It is known that the most effective way of preparing for an engineering career in the microelectronics industry is to combine deep theoretical knowledge with practice on real devices and circuits and CAD tool experience.

2. KEY FEATURES OF MICROELECTRONIC EDUCATION AT MIEM

In this paper the microelectronic educational system with close software/hardware relations developed at MIEM is discussed. The education approach is similar to the VLSI design curricula initially developed by the University of Michigan and later supported by Intel [1]. (It is well known that Intel spends much energy to improve VLSI education world-wide).

From the beginning of electronics and later microelectronics education at MIEM, the educational program gave students a deep knowledge in the fundamentals, combined with practical lab works and project-oriented works using CAD tools.

To provide high quality of education all necessary microelectronic products design stages (levels) are studied inside our microelectronics educational program:

-Semiconductor materials,
-IC manufacturing technology,
-Semiconductor devices and IC elements,
-Digital and analog circuits,
-Large systems level (ICs, SoCs, PCBs).

The key features of our microelectronics educational program are the following:

1. All design stages studied at the educational process provide high quality and universal character of microelectronic education for future engineers and researchers.

2. The system is based on close software/hardware relations during education process. Theoretical knowledges are supported by practical works with hardware and software. We consider such relations to be very important for high quality of microelectronics education

3. Practical works of devices and circuits contain two main tasks:
   - first, to study real device characteristics (hardware part),
   - second, to simulate the device with modern CAD tool (software part) and to compare with the measured data.

5. Students work with real CAD tools used at microelectronic industry for VLSI design.

6. Education-research centers (by Mentor Graphics, Synopsys, Motorola, Xilinx, Renesas, etc.) provide CAD training and microelectronic equipment experience.

7. Close collaboration with microelectronics industry enterprises takes an important part at education system.

Different aspects of the MIEM educational program were presented and discussed at international conferences and exhibitions [1-3].

Microelectronic equipment design stages and software/hardware elements studied at the educational process are described below.

3. EDUCATION-RESEARCH CENTERS – IMPORTANT PART OF EDUCATIONAL STRUCTURE

The world leading software and hardware companies understood the importance of MIEM in microelectronics education and opened education-research centers at MIEM.

Motorola and Renesas Centers provide training for students and industry engineers to the principles of operation and characteristics of modern electronic components, microcontrollers, microprocessors, telecommunication and network equipment.

ZyXEL Center provides training to get and/or improve the experience in the field of the network technologies, information security and network equipment.

Xilinx Center provides education for MIEM students and reeducation for industry engineers in the field of modern digital FPGA systems design with VHDL. The Center has special development boards (with the last versions of FPGA) for projects implementing and debugging.

Cypress Center provides training to get the experience in the field of programmable systems on chip design.

Mentor Graphics training Center is equipped with the modern versions of MG software running on PC computers. The goal of the Center is to teach students the basic techniques for analysis and design of perspective analog and digital systems based on IC chips and PCBs.

In Synopsys Center students get experience in technology/device simulation with TCAD software.

In cooperation with the leading Russian semiconductor companies the students participate in SOI/SOS CMOS, SiGe HBT, BiCMOS devices design projects.

4. COLLABORATION WITH MICROELECTRONIC INDUSTRY ENTERPRISES

As has been mentioned the microelectronic educational process at MIEM is carried out in collaboration with the leading microelectronic industry enterprises:

- Institute for Design Problems in Microelectronics of Russian Academy of Sciences;
- Federal State Unitary Enterprise "Measuring Systems Research Institute named after Yu. Ye. Sedakov" (N. Novgorod);
- Federal State Unitary Enterprise "Scientific and Production Association " Pulsar";
- Federal State Unitary Enterprise "Scientific and Production Association "Orion".

The leading specialists from these enterprises give lectures and provide real industry training for students. The student study design stages and real microelectronic production equipment. They take part at real industry projects, defense their theses and take an engineer's or master degree. The ongoing relationship with microelectronic industry provides relevance and real-world orientation of our teaching and research.

5. MICROELECTRONIC MATERIALS LEVEL

This level is the first at microelectronic education and includes the next main courses:

- Crystal physics and crystallography, with contains topics:

  crystal lattice, crystalline forms, methods for lattice description, physical properties of crystals, electric and magnetic crystal permittivity, piezoelectric effect, elastic properties of crystals, electro-optical properties of crystals,

  total of 116 hours, including
  34h lectures,
  17h labs.

- Theory of strength and plasticity. The purpose of the course - the deep understanding of atomic mechanisms of strength and deformation processes in materials. It contains topics:

  mechanisms of plasticity, materials strengthening, basic mechanical properties of materials and methods of its definition, elastic and non elastic properties of materials, fluidity, hardness, rupture of materials, high temperature strength, material fatigue, wear-resisting properties of materials.

  total of 182 hours, including
  68h lectures,
  17h labs, term project.

- Materials and elements of electron technology. The course contains topics:

  materials classifications, physical nature of conductivity, superconducting materials, conductive and resistive materials for microelectronics, characteristics and main properties of semiconductor materials, semiconductor structures in microelectronic devices, main physical processes in insulators, magnetic materials, methods of microelectronic materials and devices investigation.

  total of 250 hours, including
  85h lectures,
  35h labs,
  17h term project/

- Methods of material structure and composition investigation contains topics:

  principles and methods of X-ray spectral analysis, emission spectral analysis, methods and applications of electron spectroscope, secondary ion mass spectrometry, diffraction methods for studying the material structure (theoretical bases), X-ray methods for investigating the material structure, methods of determination of lattice parameters, X-ray spectrometer application, methods of electron diffraction analysis, electron microscopy, neutron diffraction analysis,

  total of 220 hours, including
  51h lectures,
  34h labs, term project.

The main specialized department providing education for this level is Electronic Engineering Science of Materials. The department has the laboratories:

- laboratory of metallographic analysis,
- laboratory of physic-mechanical properties of materials studying ,
- laboratory of structural analysis.

The hardware equipment for this level include:

- scanning electron microscope,
- X-ray structure analyzer ,
- X-ray diffraction meter,
- mass-spectrometer,
- spectrophotometer.

The software tool used in educational process is Synopsys TCAD.

6. IC MANUFACTURING (TECHNOLOGY) LEVEL

The departments responsible for this level are: Physical Basis of Electronic Engineering, Technological Systems of Electronics, Metrology and Sertification.

The level includes the main courses:

- Technology of materials and electronic devices. It contains topics:

  crystal growing methods, epitaxial film growning methods, glass and ceramic formation methods, methods of quality control, photolithography processes, p-n-junction formation methods, soldering and welding methods, environment influence protection, technology equipment usage.

  total of 170 hours, including
  34h lectures,
  17h labs, term project.

- Micro- and nanotechnology processes. The

course contains topics:

physical-chemical methods of surface cleaning, equipment and methods of electron beam deposition, vapor-phase epitaxy , liquid-phase epitaxy, vapor-phase, liquid-phase and ion-plasma etching, oxidation processes, diffusion, doping, ion-implant doping, annealing, lithographic processes.

total of 170 hours, including
34h lectures,
17h labs, term project.

- Physical bases of electron-bombardment technology. The course contains topics:

electron scattering theory, electrons stopping and scattering, models of electron scattering, electron-beam vaporization, electro-plasma interaction.

total of 141 hours, including
17h lectures,
17h labs, term project.

- Physical bases of ion-plasma technology. It contains topics:

ion-material interaction, including ion stopping, nuclear stopping, electron stopping, ion range, ion doping, secondary ion emission.

total of 209 hours, including
85h lectures,
17h labs, term project.

The hardware equipment for this level include:

- scanning electron microscope,
- vacuum evaporation equipment,
- laser equipment,
- equipment for metrological assurance.

It should be pointed that MIEM specialists not only use standard hardware equipment but also design some new one. For example in Figure 1 you can see student working with hardware equipment for nano film formation and investigation.

Figure 1. The last year student works with hardware for nano film formation and investigation.

To provide real industry orientation the modern IC manufacturing processes:

- conventional CMOS process,
- SOI/SOS CMOS process,
- GaAs process etc.

are practically studied at semiconductor enterprises (our partners).

For better understanding of technology features and getting experience in technology simulation, the students use Synopsys TCAD tools in their work.

They simulate real (and near future) semiconductor technology process steps and analyze characteristics of structure layers: doping distribution, depths, resistivity, etc. After they compare simulated parameters with measured ones or with ones known from theoretical course.

7. SEMICONDUCTOR DEVICES AND VLSI ELEMENTS LEVEL

MIEM provides deep studding of microelectronic device physics. The following specialized departments are responsible for education at this level: Physical Basis of Electronic Engineering, Electronics and Electrical Engineering, Radioelectronics.

The following courses are used at this level to provide deep studding of VLSI element physics:

- Solid-State physics. The course contains topics:

solid states classification, crystal lattice vibration, electron conductivity of metals, isolators properties, optical properties of crystals, magnetic properties of crystals, super conduction, electron emission, contact effects.

total of 236 hours, including
68h lectures,
17h labs, term project.

- Semiconductor physics. The course contains topics:

band theory of solids, electron and holes statistics, nonequilibrium charge carriers, charge carriers scattering mechanism, kinetic phenomena at semiconductors, generation and recombination of nonequilibrium charge carriers, diffusion and drift of nonequilibrium charge carriers, surface effects at semiconductor devices.

total of 170 hours, including
51h lectures,
34h labs.

- Solid-State electronics. The course contains topics:

metal-semiconductor contact, p-n-junction theory, rectifier theory, Zener diode physics, bipolar junction transistor theory, p-n-junction FET, MOSFET structures, Schottky transistor.

total of 130 hours, including
34h lectures,
17h labs, term project.

- Quantum and optical electronics. The course contains topics:

the interaction of electromagnetic radiation with atoms, generation and amplification of electromagnetic radiation, linear crystal optics, nonlinear optics, optical effects at semiconductors and heterostructures, solid-state and liquid lasers, gas lasers, light emitting diodes, semiconductor lasers, optoelectronic sensor, optical radiation driving, optical methods of information transfer and processing.

total of 150 hours, including

34h lectures,
17h labs, term project.

- Physical basics of semiconductor device reliability. The course contains topics:

the problem of reliability of electron devices, reliability control, reliability improvement practices, foundations of the theory of probability and mathematical statistics, probability distribution functions and coefficients, foundations of the theory of reliability, failures in electron devices: classification and mechanisms, external influence on electron devices, effects of electrical and thermal exposure and their influence on reliability of electron devices, reliability assurance tests, prediction of reliability of electron devices, mechanisms of degradation processes in materials and devices.

total of 116 hours, including
34h lectures,
17h labs.

TCAD simulation is necessary element in modern technology development. So we use TCAD (Synopsys) tool at educational process to simulate semiconductor devices characteristics. Students study the influence of device structure parameters (doping distribution, layer thickness, etc) on device characteristics (threshold voltage, current gain, transit time, etc.).

- Microelectronics course contains topics:

MOSFET characteristics, equivalent circuit, parameters, thyristors, thermistor, voltage-depended resistor, hall-effect sensor, magnetic sensitive transistor, resistance strain gauge, pressure-sensitive diode, SPICE models for different types of transistors, integrated circuit classification, digital and analog circuits, integrated bipolar transistor, NPN and PNP integrated transistors, multiemitter transistor structure, integrated injection structures, integrated rectifiers, complementary MOS FET structures, passive elements of integrated circuits, HEMT transistors, FLASH memory, GaAs transistors, Gunn effect,

total of 130 hours, including
34h lectures,
17h labs, term project.

SPICE models for semiconductor devices and parameter extraction technique are necessary and important part of our educational process.

Practical labs are performed at electronics and microelectronics laboratories and usually contain two parts:

- Experimental (hardware) part – measurements and study of real semiconductor device characteristics,
- Software part - SPICE model parameter extraction from measured data and device simulation with SPICE program.

Advanced and postgraduate students work at research laboratories and study real elements of VLSI ICs (SOI CMOS, SiGe…), measure their characteristics using probe station (see for example Figure 2), Keithley 2602 source-meter, extract SPICE model parameters using ICCAP tool and simulate with Mentor Graphics Eldo and Cadence Spectre tools.

Figure 2. The post graduate student performs his research work of SOI CMOS MOSFETS using probe station.

The specific work performed by Electronics and Electrical Department in collaboration with microelectronic enterprises are [4]:

- radiation hardness analysis and modeling ,
- electro-thermal modeling of power elements and blocks of integrated circuits.

Graduate and postgraduate students take part in these works with interest.

8. DIGITAL AND ANALOG CIRCUIT LEVEL

- Micro circuit technique course provides basic knowledge of digital and analog circuits and contains topics:

For digital electronics - BJT and MOSFET switches, simple logic gates, R-S-flip-flip, static and dynamic memory cells.

For analog electronics - BJT amplifier stage, voltage regulators, current generators, OA stages, OA applications.

The course is provided by Electronics and Electrical Engineering Department together with Radioelectronics Department.

Students get a deeper understanding of digital electronics taking the course:

Computer hardware components and its simulation. The course contains topics:

Different logic gates, different kinds of flip-flops, registers, counters, memory ICs, SPICE simulation of logic circuits.

total of 116 hours, including
34h lectures,
17h labs.

At practical (hardware) work students study characteristics of real logic gates; flip-flops; different types of registers and counters.

In analog electronics students study the real analog circuits: transistor amplifiers, OpAmps, oscillators, voltage regulators and so on.

The software tools for this level are:

- Electronics Workbench, SPICE (different versions),
- Mentor Graphics Eldo,
- Cadence Spectre.

Students simulate analog and digital circuits from single gates to large circuits, compare results with measured ones and with theoretical data (see Figure 3).

Figure 3. The student discusses his IC design project with lecturer.

9. LARGE SYSTEM LEVEL (VLSI, SOCS, PCBS)

The courses are provided by the departments: Electronics and Electrical Engineering, Computer Science, Computer Systems and Networks. The following main courses are used at this level.

- VHDL language . The course contains topics:
  Hardware description languages, VHDL operators and data types, VHDL basic constructs, objects description, VHDL additional constructs, functional verification of VHDL descriptions, circuit description with VHDL, VHDL basic libraries.
  total of 105 hours, including
  34h lectures,
  51h labs.

  Labs help to learn the usage of VHDL operators and other constructions, to get experience in project implementation with real FPGA/CPLD devices.

  Development boards (from Digilent) with XILINX Spartan-2, 3 FPGA are widely used at education process. Using development boards for education is one of the most efficient ways to learn FPGA design and their practical application.
- CAD systems. The course contains topics:
  Computed aided design stages and principles, placement and routing algorithms, PCB design methodology, IC design methodology, design libraries.
  total of 86 hours, including
  34h lectures,
  34h labs with CAD systems, term project.

Students perform analog/digital IC design with TANNER and Mentor design systems. To perform the project successively it is required to use CAD tools extensively: for circuit simulation and for layout design.

- Microprocessor systems. The course contains topics:
  Intel processor: architecture, command system, memory organization, interrupts, protected mode. RISC microprocessors and microcontrollers. Modern microcontrollers: architecture, memory, ports, interrupts, bus types, USB-bus, bult-in DAC and ADC converter, power consume control, digital signal processors.
  total of 140 hours, including
  68h lectures,
  51h labs, term project.

Microprocessors and microcontrollers are studied using professionally packed evaluation Motorola's, modern Renesas and Cypress modules and corresponding software tools . The students learn how to write simple programs in assembly and C languages, how to download them to the microcontroller and how to debug the program. Our experience shows that application boards are very interesting for students and motivate them to more deep theoretical knowledge. In Figure 4 you can see the student performing his term work with CYPRESS development board with CY8C29466-24PVXI microcontroller.

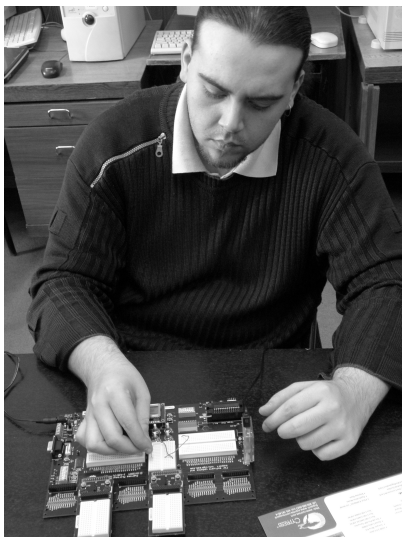

Figure 4. The student performs his term work using CYPRESS development board with CY8C29466-24PVXI microcontroller.

- Computer networks. The course contains topics:
  Principles of computer network organization, transfer protocols, local network organization and access, global networks, networks design, telecommunication hardware, network security, network administration.
  total of 116 hours, including
  34h lectures,
  17h labs.

As mentioned earlier ZyXEL Center provides practical training for students and engineers to get and/or improve the experience in the field of the ZyXEL network technologies.

It should be pointed that MIEM provides high quality microelectronic education not only for students, but also for industry engineers in the form of additional education. Xilinx Center provides additional VHDL courses and ZyXEL Center is responsible for additional education in the fields of network programming and hardware.

10. CONCLUSIONS

The microelectronics education system at MIEM based on:

- wide hardware/software products application of leading microelectronic companies,
- continues and throughout learning process: from semiconductor material to system on chip/board,

is described.

Specially created authorized educational-research Centers (Mentor Graphics, Synopsys, Motorola, Xilinx, Renesas, Cypress) provide CAD training and microelectronic equipment experience.

Collaboration with industry enterprises provide high quality education for students, post graduate students, reeducation for industry engineers, joint research projects, practical training.

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A new joint research and teaching project on micro- and power electronics

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***Abstract*— This paper describes the motivation and approach for setting up joint study and research programs in the field of Power Electronics and Micro-Electronics at Reutlingen University and University of Stuttgart initiated by and focused at the need of the Robert Bosch Automotive Electronics division.**

Keywords- industry-university cooperation; joint research, joint teaching

I. INTRODUCTION

The increasing importance of micro- and power electronics in the automotive world as well as in the energy sector sets a special focus on an excellent education in engineering.

To strengthen this education the Robert Bosch GmbH, the University of Stuttgart and Reutlingen University signed an agreement in November 2009 to cooperate in this field. Therefore the Robert Bosch Centre for Power Electronics (RBZ) has been established. Bosch funds the education and research with about 15 million EUR in a period of 10 years. The federal state government adds 12 million EUR in the same timeframe to form an excellence cluster for power and microelectronics in the heart of Baden-Württemberg.

II. KEY ASPECTS

- Technical motivation: electro-mobility will play a key role in the future automotive and supplier market. Energy generation by solar systems as well as wind power plants require electronic power conversion based on similar technologies.
- Increasing demand for highly skilled graduates in all fields of Power Electronics as well as in certain specialized fields in Micro-electronics, currently only rarely available on the HR market.
- Economic motivation: The area of Stuttgart-Reutlingen is one of the most intense industrial areas in Europe, dominated by car manufacturers and automotive suppliers. The Bosch Automotive Electronics division is currently investing a total of about 600 Mio € in a new semiconductor fab at the Bosch plant of Reutlingen, which has been inaugurated by the president of Germany, Horst Köhler, on March 18th 2010. Reutlingen University is located very close to the Bosch plant; distance to the University of Stuttgart is only 30 km. By combining high-tech semiconductor production and lab equipment of Bosch with the excellence of 2 close-range universities as well as additional financial support by Bosch this offers a great opportunity to set-up a unique centre of excellence in the above mentioned fields.
- A new 4-semester Master of Science program in Micro- and Power Electronics is currently established at Reutlingen University, existing Master programs at University of Stuttgart are extended by specialisation areas in Power Electronics. Both Master programs will start in October 2010 for the first time and students may enter these programs every term.
- At both universities existing or emerging Bachelor programs are extended with respect to form a basis for the postgraduate programs. However, holding a degree from Reutlingen University or University of Stuttgart is not mandatory at all to apply for the Master programs. Those are also open to alumni from other, even international, universities.
- Both University of Stuttgart as well as Reutlingen University of applied sciences will run a joint doctorate program, which is unique in the German academic community.

- The joint research and study centre will consist of a total of 7 chairs located at both Universities, one of the professors being employed in mutual consent between the Universities. 2 existing chairs at the University of Stuttgart, which are members of the RBZ, will be joined by 5 new professors at both universities. The structure of the RBZ with the consisting chairs can be found in fig. 1.

III. DETAILS

The Robert Bosch Centre for Power Electronics (www.RBZentrum.de) is set up as a joint research and teaching centre, where the partners focus on complementary topics. Reutlingen University has its main focus on microelectronic and power electronic modules as well as on integrated circuits whereas the University of Stuttgart with its cleanroom facilities focuses on technological aspects supplemented by the research on system aspects.

Aspects of reliability and robustness, which are important for both modules and systems, are covered by the jointly appointed professor; therefore he is the link between the universities not only in a formal manner but also in questions of research.

With the set up described before, the RBZ covers all aspects in the development of micro- and power electronics, starting from technology up to systems.

Concerning teaching, the Curricila of both universities are closely coordinated between all three partners and therefore fit very well the industry's need for education in the field of micro- and power-electronics. Whereas the University of Stuttgart extends its existing Master in Electronics towards special topics in power electronics, Reutlingen University sets up a completely new Master program. Both Master programs can be attended by all students with a relevant bachelor degree in Electrical Engineering, Electronics or a comparable bachelor degree with appropriate focus.

Besides the funding of the professors and of a part of the labs and facilities in Reutlingen, Bosch enables multichip wafer runs within its new 200mm fab. Students may design their own chips within a corresponding lesson for integrated circuit design and run these designs afterwards at Bosch. Finally, the devices will be characterized by the students either in university labs or in Bosch labs.

Very worth mentioning is the joint doctorate program of the RBZ funded by the German state of Baden-Württemberg, which may be entered by all students with a relevant Master degree. A professor of Reutlingen University and a professor of the University of Stuttgart always form a corporate pair of reviewers, independently from the PhD student working in Stuttgart or Reutlingen.

The close cooperation on the one hand enables the students to acquire the know-how of up to date technology and tools and on the other hand makes sure that they are well prepared for the work in an industrial environment.

The RBZ provides the possibility of excellent education in the field of micro- and power electronics starting from a Bachelor, complemented by a Master and finally completed by a doctorate program.

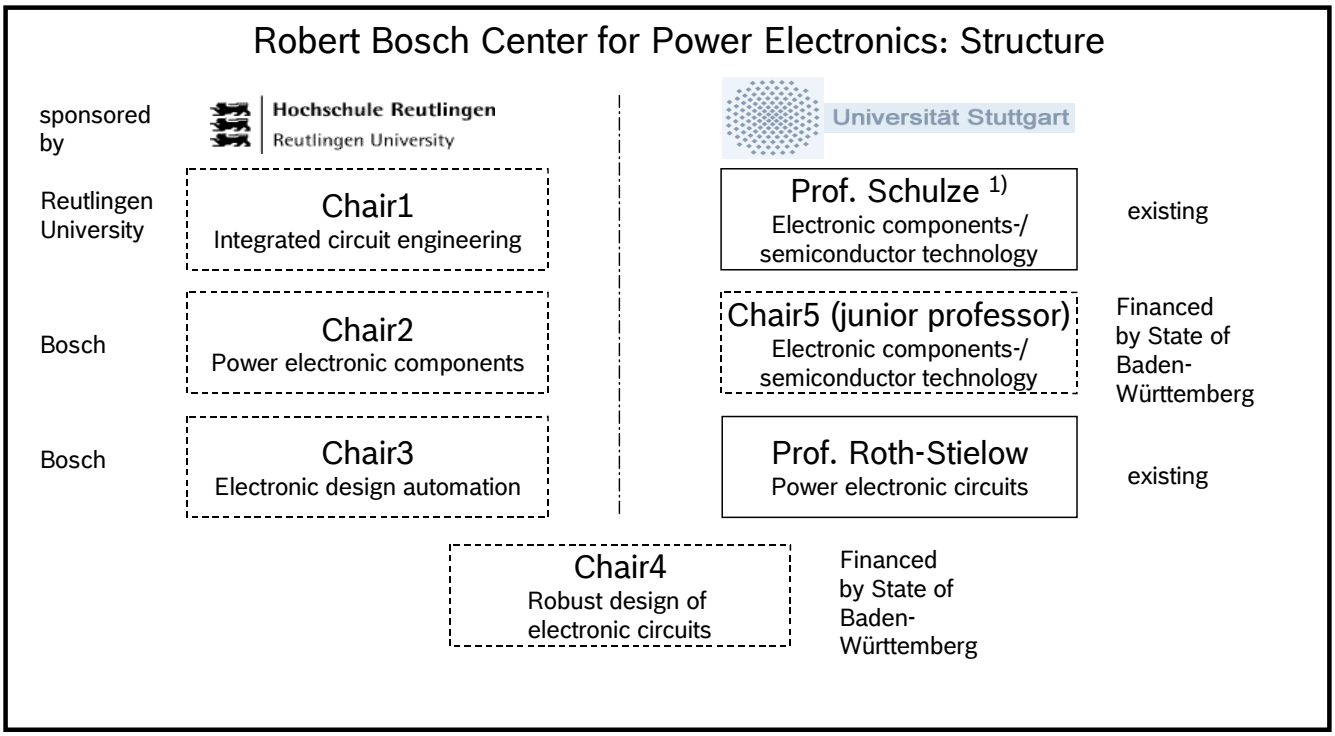

Fig.1: Structural Chart of the RBZ

E-Learning Environment for WEB-Based Study of Testing

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Abstract— **An environment targeted to e-learning of test issues in microelectronics is presented. The environment consists of a set of Java applets, desktop applications and of a web based access to the HW equipment which can be used in the classroom, for learning at home, in laboratory research and training, or for carrying out testing of students during exams. The tools support university courses on digital electronics, computer hardware, VLSI design and architectures, testing and design for testability to learn by hands-on exercises how to design digital systems, how to make them testable, how to build self-testing systems, how to generate test patterns, how to analyze the quality of tests, and how to localize faults in hardware.**

Keywords - e-learning, defects, fault models, test generation, fault simulation, built-in self test, boundary scan, fault diagnosis.

I. INTRODUCTION

Digital hardware (HW) has exhibited high reliability in the past; however, future nanometer-scale HW devices will become a source of problems. The more complex electronics systems are getting, the more important the problems of test and design for testability are becoming. These topics are often underestimated in educating electronics and system engineers. This is because in the today's university curricula test issues are usually neglected: students learn how to design electronic systems but not how to test them. The next generation of engineers involved with SoC and NoC technologies should be made better aware of the importance of test, and trained much more in test technology to enable them to develop, design and produce high quality and defect-free products.

The main goal of the conducted work was the creation of a homogeneous e-learning environment for studying the test and diagnostics of digital systems. In the paper a conception and means are presented to improve the skills of students educated for HW and SoC design in test related topics. The method presented here deals with the goal to put interactive teaching modules ("living pictures") to the Internet that can be used as tools in a lecture as well as for individual self-studies. The modules can be accessed independent of time and place. On one hand, teachers can demonstrate simulations of different examples and procedures of test related topics using living pictures during the lessons. On the other hand, students can use the same simulation modules on their home computer, if the living pictures are available on the Internet. Finally, the same modules can be used during examination.

In the following we present a set of well linked tools for learning test issues like test generation and fault simulation at different levels of abstraction. Three levels are represented: gate level, macro- or sub-circuit level where macros represent Fanout Free Regions (FFR), and Register Transfer Level (RTL). Dedicated tool sets are developed for learning Built-in Self-Test (BIST) and fault diagnosis problems. For investigating realistic physical defects in microelectronic circuits a novel web based HW/SW environment based on a special education chip ("DefSim") has been developed. It allows carrying out remote experiments via Internet with different realistic defects selected remotely in the DefSim. To learn and investigate interconnect testing issues at the printed circuit board (PCB) level, a multi-functional system, which provides a simulation, learning, research, and CAD environment for IEEE 1149.1 Boundary Scan (BS) standard has been developed.

The presented environment consists of the following tools: (1) logic level applets (LLA), (2) register transfer level applets (RTLA), (3) tool for investigation of physical defects (DefSim), (4) BIST analyzer (BISTA), (5) tools for fault diagnosis (DIAGNOZER), (6) tool for Boundary Scan research (BScan), and (7) tool set for logic level test generation and fault simulation (Turbo Tester - TT). The test related topics covered by the presented tool set are illustrated in Table 1.

Table 1. HW testing topics covered by the e-learning environment

Tools	Fault models	Test generation	Fault simulation	Chip level BIST	Board level test	Fault diagnosis
LLA		+	+	+		+
RTLA		+	+	+		
DefSim	+	+	+			
BISTA			+	+		
DIAGNOZER			+			+
BScan	+				+	
TT		+	+	+		

While the Java applets are platform-independent by their nature, all the desktop applications are available for Windows, Linux and UNIX platforms.

II. DESCRIPTION OF THE ENVIRONMENT

A. *Logic Level Test*

The engine of the concept of teaching logic level test consists of PC-based tools [1] installed locally and Java-applets invoked remotely via Internet [2]. By using the interaction possibilities of the Java-applets the students can have the first acquaintance with how to produce input test stimuli for testing logic level circuits, how to simulate faults, and how to locate the faulty gates or faulty connections (Figure 1). Different learning tasks and exercises are described in Section III, which make use of the applets.

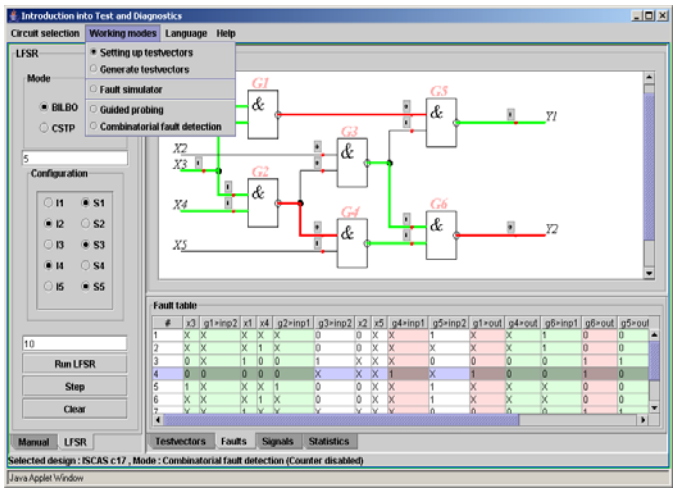

Figure 1. LLA interface

The PC-based tool set, which supports learning test at a more advanced level, is called Turbo Tester (TT). TT includes a rich set of tools for test generation implemented for different algorithms like deterministic, genetic, random, and allows in such a way to compare different approaches and methods of test generation. The circuits can be represented at different levels (gate and FFR-levels) which allow investigating the scalability of different test generation algorithms, and how the efficiency of the algorithms depends on the complexities of circuits.

Figure 2. Login page for WebTT

The set of TT tools provides good possibilities for laboratory training and experimental research. Among other convenient features this toolset has a web access to the tools installed on a server. This interface is called WebTT (Figure 2).

B. *Register Transfer Level Test*

Two types of applets are used in the environment: applets for investigating and learning test problems in simple gate level circuits, and applets for practicing design and test problems in more complex digital systems represented on RTL level, consisting of control and data paths [3] (Figure 3).

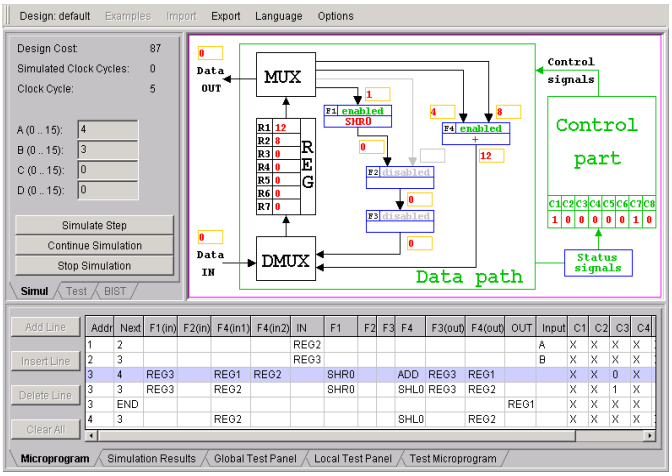

Figure 3. RTLA interface

Students can exercise RTL implementations of processors represented by data flow graphs or micro-programs (like multiplication, division, signal processing algorithms etc.). Such topics as design of data-flows and microprograms of computing algorithms, investigation of tradeoffs between speed and hardware cost in digital design, RTL simulation, design for testability, functional level test generation, built-in self-test (BIST), diagnostic analysis and other related problems are covered by these applets. By gate-level fault simulation it is possible to evaluate the fault coverage of functional tests. The applet fully reflects the "easy action and reaction" concept which was taken as the major target for its creation. Each field in the microprogram, each functional unit in the circuit map, and other modules are clickable. Their functions can be changed or further adjusted. The reaction on each action is instantly reflected by highlighting of selected modules.

C. *Defect Level Test*

The central element of the DefSim environment (Figure 4) is the IC with a large variety of shorts and opens physically inserted into a set of digital standard cells and small circuits [4,5]. The IC is attached to a dedicated measurement box serving as an interface to the computer. It is possible to select any defect of interest by addressing it in the circuit. Then the user can apply an arbitrary input test sequence and measure the circuit's response to it in terms of both the binary logic values and current levels (IDDQ). It is also possible to compare its behavior over the correct copy of the same circuit. From the didactical point of view, the DefSim environment targets (but it is not limited to) two main areas of expertise: defect modeling and defect observability. The students will learn in practice that

some simple defects represent a real challenge especially from the diagnostics (defect localization) point of view. The environment allows carrying out remote experiments via Internet.

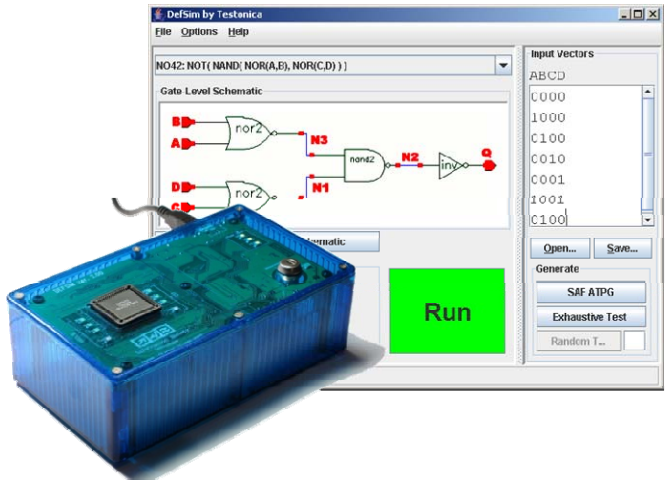

Figure 4. DefSim environment and its IC

D. Boundary Scan

The BS standard is a very important state-of-the-art testing technique of modern complex integrated systems. The main goal of the BScan tool (Figure 5) is to introduce the basic concepts of the standard [6,7].

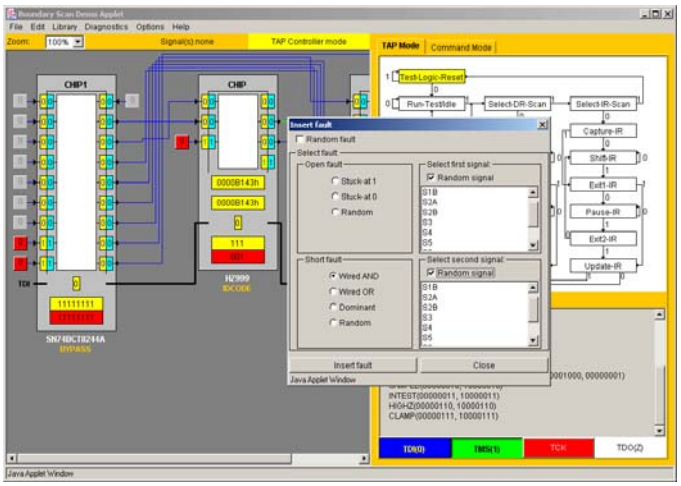

Figure 5. BScan tool

The students should learn the BS instructions and working modes and see from inside how the BS structures are operating. According to the standard, all the chips on the board are connected into a scan chain via TDI (Test Data In) and TDO (Test Data Out) pins. Hence, all the instructions and test data can be inserted via the single TDI input only. Therefore, the task of controlling the system of several BS chips is not a trivial one. First of all, students should study the Test Access Port (TAP) Controller, which is the key device in the whole BS conception. They learn to move from state to state on the state diagram and insert different BS instructions via TDI. The next step is the study of data registers and their proper usage. When the main principles of BS operation are understood, the students face the task of interconnect diagnosis. They should learn how to properly select test vectors in order to find interconnect defects of a given type. The final and the most advanced task is to write a description of an own chip according to given parameters using BSDL format.

E. Built-in Self Test

Linear Feedback Shift Registers (LFSR) and other Pseudo-Random Pattern Generators (PRPG) have become one of the central elements used in test and self test of contemporary complex electronic systems like processors, controllers, and high-performance integrated circuits. We have developed a training and research tool BIST Analyzer (BISTA) (Figure 6) for learning basic and advanced issues related to PRPG-based test pattern generation [8,9].

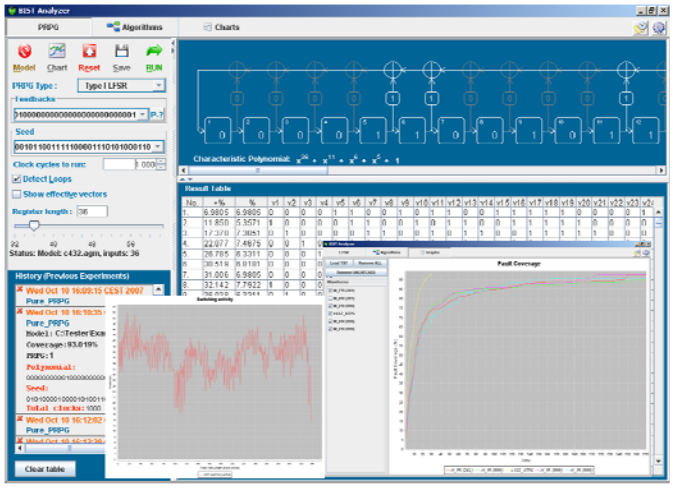

Figure 6. BISTA tool

Unlike other similar systems, this tool facilitates study of various test optimization problems, allows fault coverage analysis for different circuits and with different LFSR parameters. The main didactic aim of the tool is presenting complicated concepts in a comprehensive graphical and analytical way. The multi-platform JAVA runtime environment allows for easy access and usage of the tool both in a classroom and at home. The BISTA represents an integrated simulation, training, and research environment that supports both analytic and synthetic way of learning.

F. Fault Diagnosis

The tool set DIAGNOZER (Figure 7) represents a multifunctional remote e-learning environment for teaching research by learning and investigating the problems of fault diagnosis in electronic systems [9,10]. It is a collection of software tools which allow simulating a system under diagnosis, emulating a pool of different methods and algorithms of fault location and analyzing the efficiency of different embedded self-diagnosing architectures, and investigating the effect of real physical defects in electronic circuits. Both, fault model based and fault model free approaches to fault diagnosis as well as cause-effect and effect-cause techniques of fault location are supported in the presented environment. Also different embedded BIST and self diagnosis architectures are emulated to evaluate the efficiency of diagnosis. The emerging novel fault model free approach is

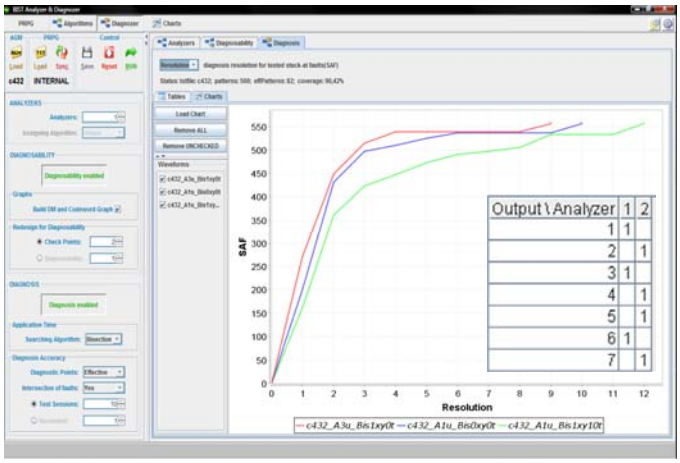

Figure 7. DIAGNOZER tool

supported by the tool DefSim which allows to investigate real physical transistor-level defects in electronic circuits and to map them on the higher logic level for interpreting the fault model free diagnostic results.

III. TEACHING SCENARIOS

Based on the presented teaching tools the following hands-on laboratory scenarios have been developed and are currently used in teaching and self-learning of test related topics.

A. Introductory Topics of Digital Test

Scenario 1: Logic level testing of digital circuits

Learning logic level test involves the following exercises with using the applets LLA:

- manual test generation for a given gate-level circuit,
- analyzing the quality of tests by fault simulation,
- generating fault tables and fault locating procedures,
- creating procedures for fault diagnosis and locating faults in a circuit.

The task of test generation consists of finding a set of test patterns which is able to detect all the possible faults in the circuit. The students can try to minimize such sets of test patterns. Another exercise is to generate a set of diagnostic test patterns which can be used to locate any possible fault.

Some of the tasks can be organized in a gaming style or as a competition between students. For example, a fault can be inserted into a circuit by the teacher, and a competition between students will be thereafter carried out in a manner who is the first who can localize the fault i.e. who will be able to use the minimum search steps. This way of working with applets makes learning very exciting.

B. High-Level and Hierarchical Test

Scenario 2: RTL level testing of digital systems

Learning higher RTL level test involves the following scenarios with using the applets RTLA:

- design of a data and control paths (microprograms) on RT level with investigation of the tradeoffs between speed and HW cost,
- RT-level simulation and validation of the created microprograms,
- functional high-level test generation and low level test quality (stuck-at fault coverage) measuring.

In the functional test mode first, the cheapest test technique is investigated, which does not require designing special test programs and embedding of special test structures into the system. The required level of fault coverage must be achieved by a smart selection of input data. The sole checkpoint allowed for catching the fault is the data path primary output.

Scenario 3: Hierarchical testing of digital systems

Hierarchical test mode for digital systems is investigated according to the following scenario:

- for each selected functional unit (FU) in the system, gate-level local tests are generated, and the fault coverage of these tests is calculated,
- for each FU, a dedicated high-level (RTL) symbolic test microprogram is generated,
- for each FU, a hierarchical test by embedding its local tests into the RTL symbolic test is generated,
- the hierarchical fault simulation in order to evaluate the global fault coverage of the whole test program is executed.

C. Defect Level Test

Scenario 4: Introduction to physical defects

Learning defect level testing is supported by the DefSim environment. All the exercises can be divided into two groups: less advanced and more advanced ones. The first group of tasks is targeted on students whose main specialization is general microelectronics:

- getting a truth table of good (without defects) CMOS simple and complex standard gates,
- getting a truth table of good (without defects) small combinational circuits,
- repeating the steps above but with a given defect of a certain type in order to observe how the circuit's function is modified by the defect,
- getting basic knowledge of voltage and current testing principles.

The second group is for students in more specialized courses and described in scenario 5.

Scenario 5: Test generation for defects

In the DefSim environment, the user gets a chance to compare the efficiency of different logic level fault models in the way they are capable of covering all shorts and opens in a CMOS circuit. The students will learn in practice that some simple defects represent a real challenge especially from the diagnostic point of view. Since DefSim supports voltage and IDDQ testing, the user can compare the efficiency of both

methods in terms of fault detection. In most cases their performance is noticeably different. The following DefSim-based exercises are targeting defect level test generation:

- test generation for opens in a small circuit using a transistor-level schematic and in a bigger circuit using a logic-level schematic,
- finding all possible test vectors for a given short and calculation of its truth table,
- checking the efficiency of stuck-at fault (SAF) test in detection of shorts and opens,
- detection and localization of an unknown defect,
- study of shorts that form memory elements inside combinational circuits.

D. Built-In Self-Test

Exercises on the BIST are based on the tool BISTA, and the following problems are targeted: PRPG solutions and their mathematical models, test pattern generation (TPG) configurations, test quality issues, fault coverage improvement, and TPG optimization.

Scenario 6: Introduction to PRPG

The scenario is devoted to investigation of the basic concepts of PRPG and ensures that the students understand the subject and that they are ready to proceed with the rest of the work. The scenario consists of:

- checking of the primitivity of polynomials for the following PRPG types: LFSR, modular LFSR and cellular automaton,
- generation of pseudorandom test patterns with 100% fault coverage for a given small circuit with as short test length as possible.

Scenario 7: PRPG Optimization

In this scenario the students study and compare efficiency of pure PRPG with reseeding technique and hybrid BIST methods. The scenario consists of the following tasks:

- generation of pseudorandom test patterns for a given large circuit with as high fault coverage as possible by using all available PRPG types,
- comparison of different PRPG types,
- investigation of the BIST with reseeding,
- investigation of the hybrid BIST.

E. Fault Diagnosis

Exercises are based on the tool DIAGNOZER, and target the following topics: methods and strategies of diagnosis, improving diagnostic resolution, optimization of procedures, and investigation of the diagnosibility of systems.

Scenario 8: Diagnostic response analysis

In this scenario, students investigate the properties of the response analyzer based on designing different architectures of the analyzer block. The scenario involves the following tasks:

- investigation of the dependency of the diagnostic resolution on the numbers and lengths of signature analyzers in the response analysis block,
- investigation of the dependency of the diagnostic resolution on the length of the diagnostic procedure.

Scenario 9: Diagnostic algorithms

Students study the properties of different methods and strategies of fault diagnosis: binary bisection of patterns, binary bisection of faults, jumping and doubling. They study also the cause-effect and effect-cause diagnostic approaches and analyze the efficiency of the fault model free diagnosis by comparing it with classical SAF model diagnosis. The scenario involves the following research exercises:

- evaluation of the diagnosibility of circuits for different approaches like cause-effect, effect-cause and fault model free diagnosis,
- comparison of the diagnostic resolution and test lengths for different fault diagnosis methods,
- redesign circuits for better diagnosibility.

The presented scenarios are adapted for both analytic and synthetic study, where the students first learn the subject by observation (using prepared examples) and then generate and/or solve their own specific exercises. The scenarios cover various strategies and methods of organizing and optimizing test generation and fault diagnosis.

IV. EVALUATION

The described teaching scenarios had been successfully practiced at many European universities such as Linkoping in Sweden, Darmstadt and Ilmenau in Germany and of course at the Tallinn University of Technology.

At the Ilmenau University of Technology the course was evaluated by the students with very positive results: On a scale from 1(best) to 5 (worst) the overall rating of the lecture was 1,3. The use of the interactive tools was rated with 1,1. The students stated out that they have learned much by own experiments with the interactive tools. It was also positive mentioned that the relation between learning outcome and necessary learning time was very efficient.

V. CONCLUSIONS

The presented environment for carrying out different laboratory research scenarios to get hands-on experience in the field of testing and fault diagnosis of complex digital systems allows students to inspect the taught subjects by individual research experiments. The proposed environment supports distance learning as well as a web-based computer-aided teaching. The interactive modules are focused on easy action and reaction, are attractive and encourage students for critical thinking. The tasks chosen for hands-on training represent simultaneously research problems, which allow fostering in students problem solving skills and creativity.

The described environment is introduced into teaching process at the Tallinn University of Technology in Estonia and is suited for using at all levels – bachelor, master and doctoral study. It has been used also in teaching at several universities in Sweden, Germany and Portugal, and has got a positive feedback from students.

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Introduction to Fault analysis at Logic Level – An Educational Approach based on DSCH

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Abstract—This paper presents an educational approach to practice fault analysis at the gate level of digital circuits by means of a specially designed fault injection block. The technique allows injection of single stuck-at fault at the nodes of the circuit. This tool is integrated to DSCH3, and allows the logic simulation of basic blocs in the presence of faults, as well as determining the fault coverage of a set of test vectors.
This cooperative work consists in introducing DFT tools and fault analysis capabilities, in order to improve the skills of students in the field of integrated circuit testing.

***Index Terms* — Integrated circuit design, Testing, Design for Testability, logical stuck-at fault model, DFT CAD educational tools.**

I. INTRODUCTION

The development of the teaching of microelectronics in Tunisia follows the international curricula. At the beginning the course was based on the characterization of materials, the technological processes like on the design of the devices and basic cells for ASICs and design flow. Currently it touches the various nano and micro aspects and new electronic devices. It relates to the preceding fundamental aspects in addition to the modern flow of design for reconfigurable supports or not. In this flood of design, the most used tools for description are them: VHDL, VHDL-AMS, SystemC. Initially the didactic tools were based on tools of CAD in version of demonstration of software or on university versions, as published in [1-3].

However, new helps with education programs or agreements of companies like Mentor, AMS… or association protocols with CMP [4] and Europractice [5] open to our university new opportunity with tools accessibility. At our days, in the University of Monastir and Sousse (ISSAT and ENISO), the graduates in master of microelectronics are more than 200. Majority of these students continued in doctorate and already supported there PhD.

On the other hand, the increasing complexity of VLSI circuits, Systems on-Chip (SOC) or even Networks-on-Chip (NOC) has made test generation one of the most complicated and time-consuming problems in digital design. The more complex are getting electronics systems, the more important will be the problems of test and design for testability because of the very high cost of testing electronic products. At present, most system designers and electronics engineers know little about testing, so that companies frequently hire test experts to advise their designers on test problems, and they even pay a higher salary to the test experts than to their VLSI designers. This reflects also today's university education: IC design is widely introduced, but only truly dedicated students learn test. The next generation of engineers involved with System-on-Chip (SoC) technology should be made better aware of the importance of test, and trained in test technology to enable them to produce high quality and defect-free products.

This paper introduces the context of microelectronics education in Tunisia (section 2), gives the theoretical backgrounds of the tool (section 3), and proposes a tool overview as well as an illustration on simple case studies (section 4), followed by a conclusion.

II. MICROELECTRONICS EDUCATION IN TUNISIA

On April 2008, the CNFM (French Center of Training in Microelectronics) [6] signed a framework agreement for collaboration with the Universities of Sousse and Monastir and the Technology pole of Sousse, Tunisia. The agreement was signed in Tunis in the Mediterranean Forum Business Development-MAD-ALLIA. This framework agreement expresses the intention to develop training, research and technological innovation in the field of microelectronics in Tunisia, as well as increase mobility between the various agencies involved in the two countries.

Specifically, it plans to establish in Tunisia, various measures based on the experience of CNFM network in France: pooling resources and expertise, provision of software, training of trainers, education days, welcoming students and trainers in the central technology of open CNFM, etc.. The partners are also committed to working together to obtain financing including through tender or programs promoting international relations.

This collaboration is one aspect among others who express the desire for Tunisia to take forward in the field of microelectronics. This dynamics of teaching and the formation by research allowed the attraction of foreign industrial activity in engineering in Microelectronics like ST Microelectronics (300 engineers in 2007), ALCATEL, SAGEM (3200 people)… or national industry like TELNET...

This industrial activity was consolidated by the creation of a new technological poles specialized in Microelectronics in Sousse (third city in Tunisia) after that of the technological pole El Ghazala in Tunis although specialized in telecommunication.

On the other hand, DSCH3 and Microwind3 [7] tools have been used from several years in Monastir, Gabes and Sfax (since 1998) in their free version, and, more recently, in ISSAT of Sousse which, actively use DSCH3 and Microwind3 (in their complete version) as a “tester user”. Labs based on DSCH3 and Microwind3 are introduced and taught in a course entitled "Advanced Design" [8][9] in the department of electronic engineering as an option. All students chose this option, find the content very interesting and their feed-back is very positive.

III. THEORETICAL BACKGROUND FOR THE TOOL

Design of logic integrated circuits in CMOS technology is becoming more and more complex since VLSI is the interest of many electronic IC users and manufacturers. A common problem to be solved by designers, manufacturers and users is the testing of these ICs.

A. Testing an IC

Testing an integrated circuit can be expressed by checking if its outputs correspond to the inputs applied to it. If the test is positive, then the system is good for use. If the outputs are different than expected, the IC is rejected (Go/No Go test). A diagnosis may be applied to it, in order to point out and identify the problem's causes.

Testing is applied to detect faults after several operations: design, manufacturing, packaging, as illustrated in figure 1. If a test strategy is considered at IC level, the fault can be detected at early system design stages, located and eliminated at a very low cost. When the faulty chip is soldered on a printed circuit board, the cost of fault remedy would be multiplied by ten. And this cost factors continues to apply until the system has been assembled and packaged and sent to final users, as illustrated in Figure 2.

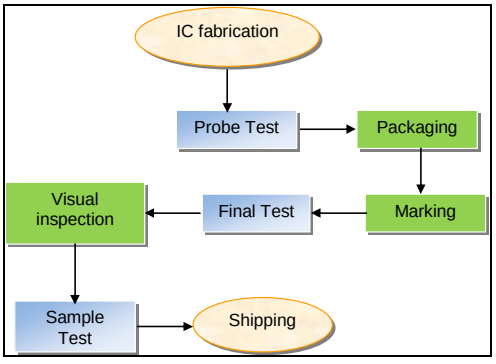

Figure 1: typical IC production flow

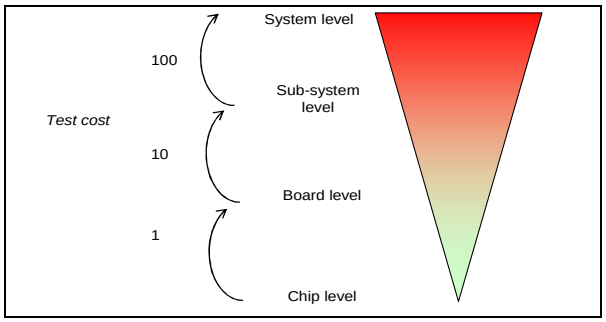

Figure 2: Test cost (The rule of ten)

The first idea to test an N input circuit would be to apply an N-bit counter to the inputs (controllability), then generate all the 2N combinations, and observe the outputs for checking (observability). This is called "exhaustive testing" (Fig. 3), and it is very efficient, but only for few- input circuits. However, this technique becomes very time consuming when the input number increases. Given a set of faults in the circuit under test (CUT), our goal is to obtain the smallest possible number of test patterns which guarantees the highest fault coverage. Test compaction refers to the process of reducing the number of test patterns in a test set without reducing its fault coverage.

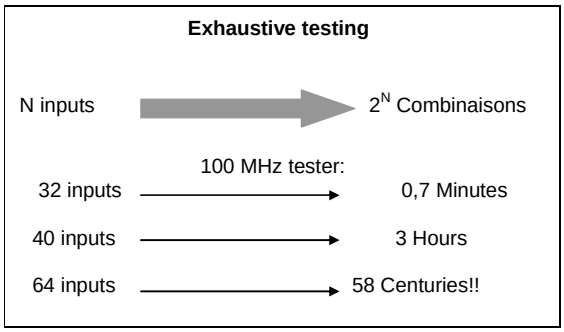

Figure 3: The exhaustive testing time becomes prohibitive with a large number of IC inputs.

A test pattern (or test vector) for a fault *f* in a circuit *C* is an input combination for which the output(s) of *C* is different when *f* is present than when it is not (Fig. 4). A test vector *x* detects fault *f* if:

$$C(x) \oplus C_f(x) = 1$$

Where: $C(x)$ is the response of the fault free circuit, and $C_f(x)$ is the response of the faulty circuit.

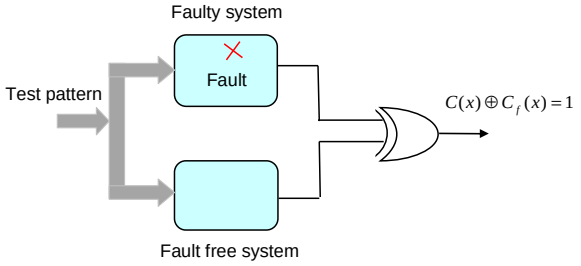

Figure 4: A test pattern detects a fault if the fault free response is different from the faulty response.

B. Fault Testing

1) Fault model

Failure modes are manifested on the logical level as incorrect signal values. A fault is a model that represents the effect of a failure by means of the change that is produced in the system signal. Several defects are usually mapped to one fault model, and it is called a many-to-one mapping. However, some defects may also be represented by more than one fault model. Fault models have the advantage of being a more tractable representation than physical failure modes. It is possible to mark most commonly used fault models (Table 1).

Fault Model	Description
Single stuck-at faults (SSF)	One line takes the value 0 or 1.
Multiple stuck-at faults (MSF)	One, two or more lines have fixed values, not necessarily the same.
Bridging faults	Two or more lines that are normally independent become electrically connected.
Delay faults	A fault is caused by delays in one or more paths in the circuit.
Intermittent faults	Caused by internal parameter degradation. Incorrect signal values occur for some but not all states of the circuit. Degradation is progressive until permanent failure occurs.
Transient faults	Incorrect signal values caused by coupled disturbances. Coupling may be via power bus capacitive or inductive coupling. Includes internal and external sources as well as particle irradiation.

Table 1: Most commonly used fault models

As a model, the fault does not have to be an exact representation of the defects, but rather, to be useful in detecting the defects. For example, the most common fault model assumes single stuck-at (SSF) lines even though it is clear that this model does not accurately represent all actual physical failures. The rational for continuing to use stuck-at fault model is the fact that it has been satisfactory in the past. In addition, test sets that have been generated for this fault type have been effective in detecting other types of faults. However, as with any model, a fault cannot represent all failures. Further will be discussed a bit closer the fault models that have been brought in Table 1.

2) Stuck-at-faults

As it was mentioned earlier, a single stuck-at fault (SSF) represents a line in the circuit that is fixed to logic value 0 or 1. We consider here permanent faults that are faults that are continuous and stable, whose nature do not change before, during, and after testing. These faults are affecting the functional behavior of the system permanently. These faults are usually localized and can be modeled. Other faults such as temporary faults or intermittent faults are not considered in this application note.

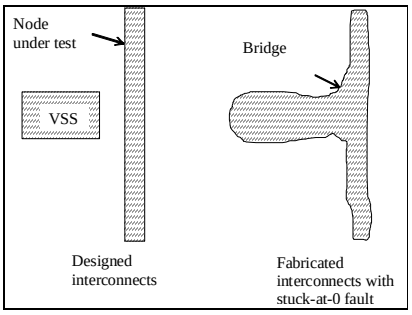

Figure 5: Physical origin of a node fault stuck at 0.

Fig. 5 illustrates a possible origin for a node stuck at 0 voltage: the implementation is close to a VSS node (here situated close, same layer), and a faulty metal bridge makes a robust connection to the ground.

3) Other faults

The manufacturing of interconnects may result in interruptions or short-cuts, which may have catastrophic consequences on the behavior of the integrated circuit. Fig. 6 illustrates the case of “Open” and “Short” faults, not considered in DSCH for fault simulation.

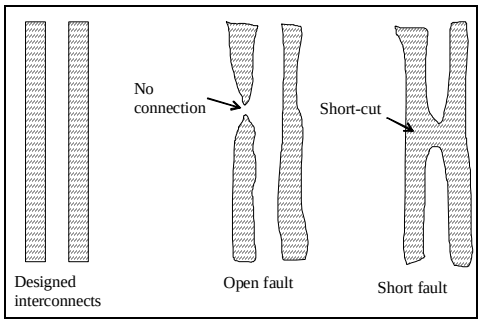

Figure 6: Physical origin of the “Open” and “Short” fault.

Many other faults are also considered in the literature: transistor stuck-on and stuck-open faults interconnect transition and delay faults, etc... These faults are not considered in this work. Independent of how accurately the stuck-at fault represents the physical defect, we next continue investigating how to generate patterns that detect these faults.

4) Testing and fault coverage

Testing is the process of determining whether a device functions correctly or not. The question is: How much testing of an IC is enough? The Yield (Y) is defined as the ratio of the number of good dies per wafer to the number of dies per wafer. Fault coverage (FC) is the measure of the ability of a test set T to detect a given set of faults that may occur on the DUT (Device Under Test). We shall try to achieve FC=1, that is a fault coverage of 100%.

FC= (#detected faults)/(#possible faults)

Defect level (DL) is the fraction of bad parts among the parts that pass all tests.

$$DL = 1 - Y^{(1-FC)}$$

Where FC refers to the real defect coverage (probability that T detects any possible fault in F or not) and DL is the DPM (defects per million). Typical values claimed are less than 200 DPM, or 0.02%.

IV. Tool Overview and Case Study

DSCH3 is software [8-9] for logic design, companion of Microwind, an educational tool for CMOS IC design [7]. Based on primitives, a hierarchical circuit is built and simulated. Interactive symbols are used to friendly simulation, which includes delay and power consumption evaluation.

In this work, we introduce the concept of fault, consider the Single Stuck-at Fault model (SSF), and show how these faults may be injected and simulated. Then, using DSCH, we show how to build a reference truth table, and how to simulate these faults applied to input and output nodes of the circuit under test. We investigate how test patterns detect these faults. The ultimate goal is to classify the efficiency of test patterns, in order to select the most efficient test vectors, and therefore reduce the number of test patterns.

A. Fault simulation concepts

1) Introduction to fault simulation

Fault simulation is performed during the design cycle to achieve the following goals:

- Testing specific faulty conditions
- Guiding the test pattern generator program
- Measuring the effectiveness of the test patterns

To perform its task, the fault simulation program requires, in addition to the circuit model, the stimuli, and the responses of a good circuit to the stimuli, a fault model and a fault list. As was mentioned earlier, there are different fault models, and the most widely used is the stuck-at model. Test patterns generated for this model have proven to be useful for other types of models, such as multiply stuck-at, bridging, and delay faults. The responses deduced by the fault simulator are used to determine the fault coverage.

In the fault simulation process, a fault is considered from the list and a pattern is applied to the circuit. If the fault is detected, it is dropped from the fault list and the next fault is considered. Otherwise, another pattern is applied, and if the fault is not detected when all patterns are applied, the fault is then considered undetectable by the test and is removed from the fault list. The process is continued until the fault list is empty.

Another way to perform fault simulation is to consider first, the fault free circuit, simulate it and extract a reference truth table. After that, simulate faulty circuit by injecting faults one by one, and for each fault extract a faulty truth table that should be compared with the reference table in order to find out test vectors for the considered fault. This is done until the fault set is empty.

2) Fault simulation result

The output of a fault simulator separates faults into several fault categories. If we can detect a fault at a location, it is a testable fault. A testable fault must be placed on a controllable net, so that we can change the logic level at that location from 0 to 1 and from 1 to 0. A testable fault must also be on an observable net, so that we can see the effect of the fault at a primary output (PO). This means that uncontrollable nets and unobservable nets result in faults we cannot detect. We call these faults untested faults, untestable faults, or impossible faults. In this section we investigate the testing of two circuits, a Nand-Or combination and a full-adder.

B. Case study1: Fault injection in Nand-Or Circuit

1) Manual fault injection

The Nand-Or circuit is a simple combination of a 2-input NAND gate and a OR gate. The concept of manual fault injection is presented in fig. 7. The fault injection at a node N consists in opening the connection and inserting a multiplexor circuit. An example of s@0 and s@1 injection circuit is proposed, based on two multiplexors, one for the function mode (normal function/fault injection mode), the second for the injected fault type (s@0/s@1). A manual implementation in DSCH is reported in Fig. 8 and the corresponding simulation in Fig. 9, with both normal and fault injection.

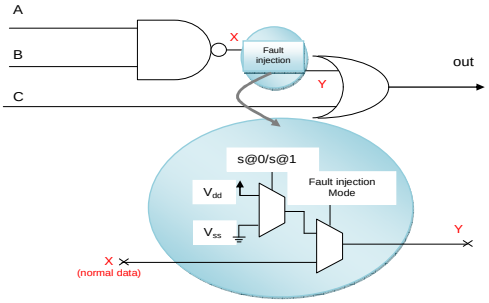

Figure 7: Fault injection principles

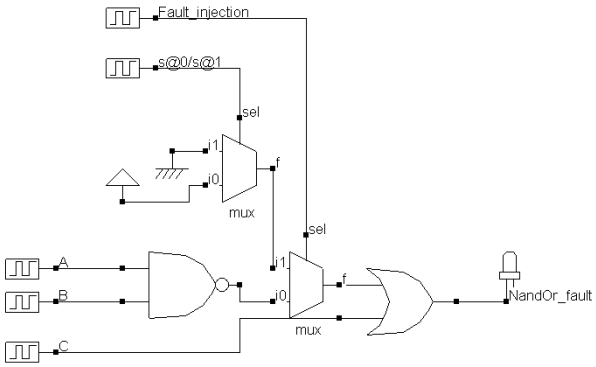

Figure 8: Manual fault injection in a NAND-OR circuit

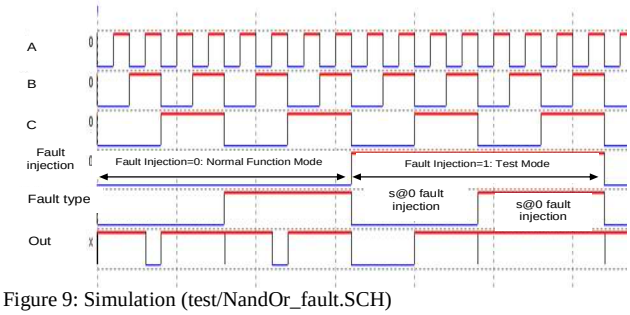

Figure 9: Simulation (test/NandOr_fault.SCH)

2) *Automatic fault injection*

The NandOr circuit has five nodes, therefore 10 possible stuck-at faults, if we also consider the internal node linking the NAND2 output to the OR input. The automatic Fault Analysis Tool is executed by following the next steps. First, the student launches the logic simulation which feeds the table with the values obtained in the chronograms of the circuit logic simulation. Second, the student specifies the type of fault and injection nodes: the student selects the type of fault "s@0 & s@1", and applies it to "All nodes" (Fig. 10).

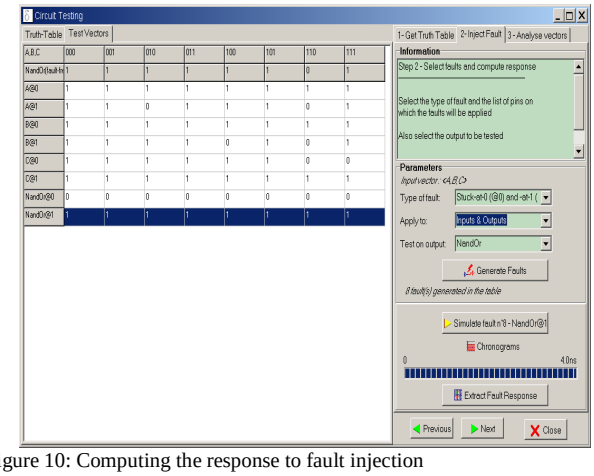

Figure 10: Computing the response to fault injection

The student generates the fault list and pilots the simulation which evaluates the consequence of all faults one by one. The logic values are transferred to the corresponding line. The student repeats the last two steps until the table is completed (Fig. 10). By a click on "Highlight Detection Vectors", the result is shown in Fig. 11.

From Fig. 11, it can be seen that the vector 110 detects A@0, B@0, C@1 and NandOr@1 (4/8 faults). The vector 100 detects B@1 and NandOr@0 (2/8 faults). The vector 010 detects the fault A@1. The vector 111detects the remaining fault C@0. Therefore 4 test vectors (010, 100, 110, 111) detect all stuck-at faults (test time will be the half of an exhaustive test).

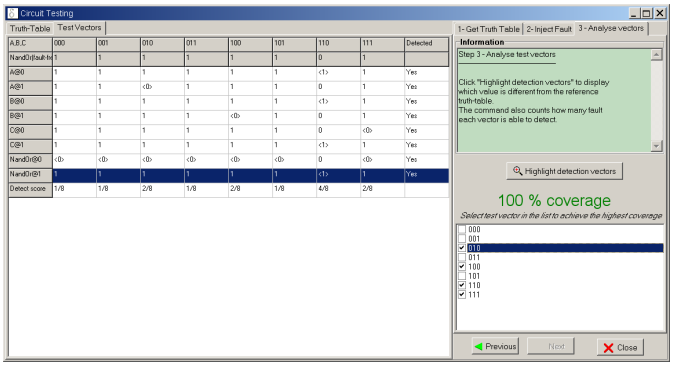

Figure 11: Vector detection efficiency evaluation, showing a 100% fault coverage

V. Conclusion

This paper has described an educational feature added to DSCH linked with fault injection and simulation at logic level. The mechanisms for logic fault injection, simulation and optimum test vector extraction have been described and illustrated on case-studies. The tool will be introduced in Sept. 2010 in Tunisia and France for conducting practical trainings related to IC test and illustrated theoretical courses about logic gate and logic circuit testing. Future developments will concern a module for fault injection at the layout level using Microwind3. The idea is to model the failure with a spot interfering with lithography at a given process step, and then move it on the layout, simulate with SPICE and observe its effect on the electrical behavior of the circuit in comparison with the defect free circuit.

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Interactive eLearning courses

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***Abstract*—This article shows the authors' motivation and experience in designing, realization and implementation of interactive www course "Electronic devices and circuits" in both Slovak and English language. These eLearning projects are accessible on the educational portal „eLearn central" for the students. The essential part of the course is a library of interactive flash animations. The course "Electronic devices and circuits" in Slovak language is free and has been successfully exploited as support of face to face education in Dpt. of Microelectronics since 2005.**

Keywords-interactive web course; eLearning; electronic devices and circuits; flash animations; SCORM

I. INTRODUCTION

The Internet, as an information source, has now a dominant position in our lives. Especially young people like this way of obtaining information much more than other ones. An ordinary student prefers automatic search of information through the Internet to personal visit of a library, information centre or another institution. These students expect to have an access to the same technology for education as they have now for other purposes - computers, cell phones, pagers, and PDAs. Simply they like to be connected. In this point when Internet is set on top, we can say that interaction beats the passivity. Modern Information Technology has opened up many new possibilities in learning [1, 2].

By combining the Internet, interactivity and learning we get one of the most popular and progressive forms of education at the present time, well-known as eLearning. Multimedia elements, time and place independence, wide information sources belong to other advantages which cannot be found in classical education.

Universities are the repository and the transmitters of the nation's scientific knowledge, so they must keep pace with the rapid expansion of knowledge. Otherwise, their students would receive an outdated education. This trend concerns of course students attending Faculty of Electrical Engineering and Information Technology, Slovak University of Technology in Bratislava, as well.

Our students engage the subject "Electronic devices and circuits" in the second year of their bachelor study [3]. The subject "Electronic devices and circuits" deals with basic knowledge of physical principles, electrical properties, technology and constructional principles of passive and active electronic devices, the basic knowledge about electronic systems, circuit properties of passive and active devices, application of diodes, transistors, operational amplifiers, digital circuits and another semiconductor devices in different applications.

It is well known that it is very difficult to understand basic principles of electronic devices and systems without understanding inner processes in semiconductors. One of the ways how we can help students to reduce knowledge differences, to motivate them and to raise education efficiency of subject Electronic devices and circuits was to create an eLearning source of information - interactive www course "Electronic devices and circuits" to enhance the quality of traditional teaching methods.

II. THE COURSE "ELECTRONIC DEVICES AND CIRCUITS"

The course "Electronic devices and circuits" in Slovak language is the standard self contained eLearning course and includes 10 lessons converted into SCORM packages (Shareable Content Object Reference Model) [4], more than 30 interactive animations, glossary with more than 300 terms and number of hypertext references. The lessons have been supplemented by one/two types of interactive self testing modules. Creating of such type of course is very difficult and time consuming.

The course is accessible for students on the educational portal „eLearn central" (http://ec.elf.stuba.sk). The „eLearn central" portal is located on the server of the Department of Microelectronics FEI STU. The current version of this portal uses a course management system Moodle 1.9. (Modular Object-Oriented Dynamic Learning Environment), which is an open source software package designed to help educators create effective internet-based courses and web learning sites [5]. These courses are successfully implemented in education process on Dept. of Microelectronics since 2005 [6].

A. The course lessons

A single course lesson gives the basic principle definitions and terms connected with electronic devices and circuits to FEI students in the second year of their Bachelor study.

Lesson titles are the following:

- Electronic systems, devices and passive circuits
- Semiconductors and pn junction of semiconductors

- Semiconductor diodes and diode circuits
- Bipolar junction transistor
- Bipolar junction transistor dynamical parameters
- Unipolar transistor
- The bipolar junction transistor as an amplifier - the common-emitter
- Further basic scheme with bipolar junction transistors
- Operational amplifier
- Digital circuits (Fig. 1)

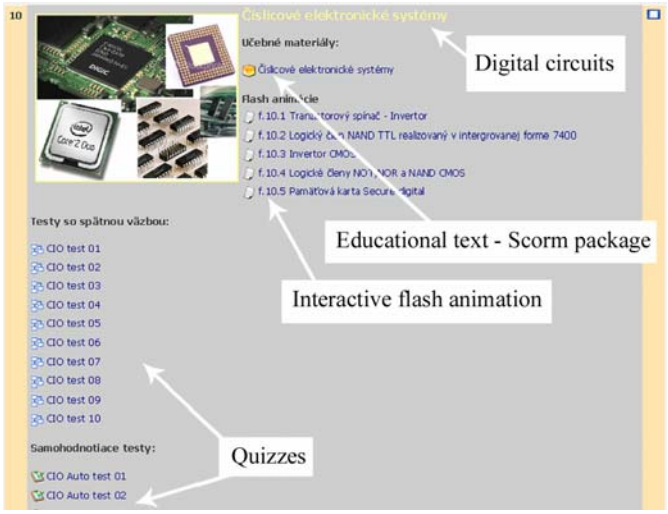

Figure 1. Visitor´s view of the Student menu "Electronic devices and circuits" - lesson "Digital circuits".

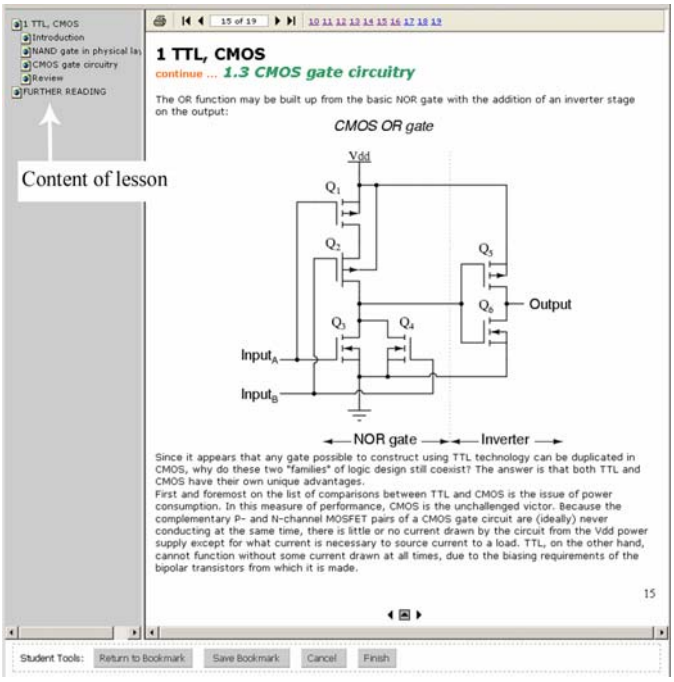

Figure 2. The lesson "Digital circuits", CMOS gate circuitry – SCORM.

Figure 3. The lesson "Diode", Diode types – SCORM package.

All the course lessons are converted into a SCORM package (Fig. 2 and Fig. 3), as SCORM is a widely approved eLearning standard, which describes a specific way to deliver some eLearning content. It is a part of a strategy called the Advanced Distributed Learning (ADL) initiative [4]. SCORM is a collection of standards and specifications adapted from multiple sources to provide a comprehensive suite of eLearning capabilities that enable interoperability, accessibility and reusability of web-based learning content.

SCORM packages are created by software THESIS Professional [7]. The THESIS product family comprises a set of SCORM compliant eLearning tools that make it possible for educators to use popular Microsoft Office programs, such as Word, PowerPoint, Excel, Visio, and MS Producer to create learning objects for eLearning.

B. The interactive animations

The students imagination of inner processes in semiconductors and electronic circuits is not supported enough only by static pictures and characteristics. Our goal was to help the students to understand these processes through various interactive animations. The animations have been designed in such a way that they would show animated details of a given object and so help obtaining the knowledge much easier and faster.

The animations have been created by using Adobe flash tool [8] or by using both Adobe Flash software and SPICE (Simulation Program with Integrated Circuits Emphasis) (Fig. 4). Some animations work as a format converter of SPICE output files into graphic Internet browser show format [9]. We have created the output files for variety of input parameters using simulation in the SPICE application. Thanks to this we are able to provide a high level of interactivity in our animations.

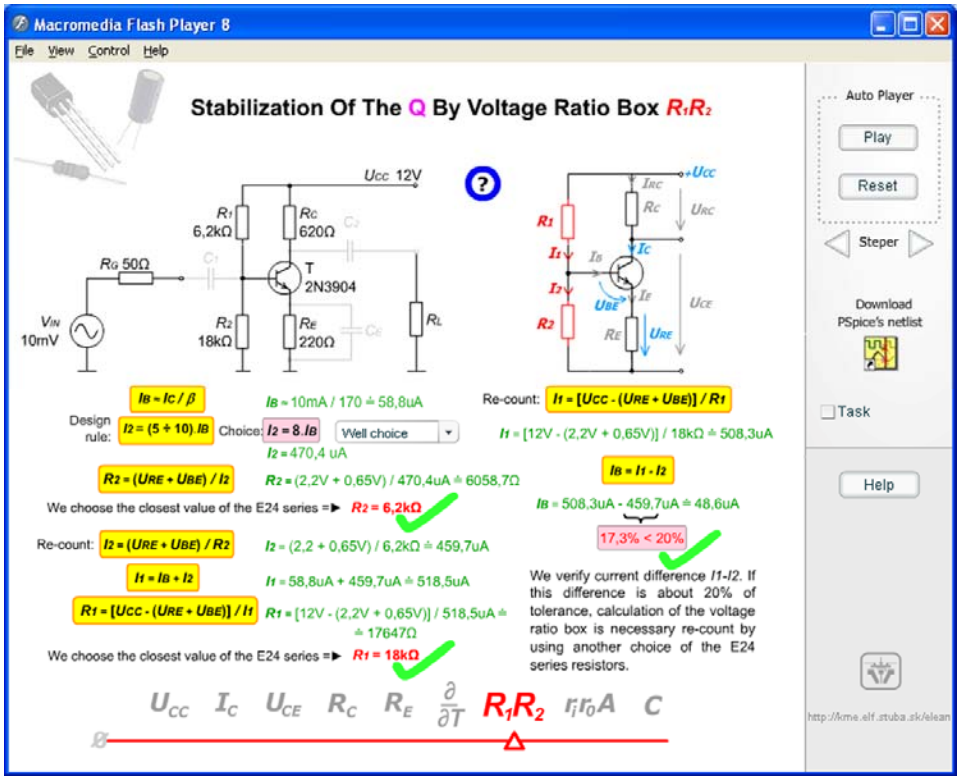

Figure 4. Interactive Flash animation "Low frequency Amplifier design" - Step by Step

We decided to use these authors´ tools for interactive animation creation because of its potentiality to authentically capture the important interaction in electronic devices and the possibility to work with scalable vector graphics. Flash also fulfilled the requirement for the smallest size of animations, vector graphic with the view of non-decreasing quality at higher resolution. An output format of finished animation could be then published on web pages very easily.

More than 30 interactive animations were initially developed for a course „Electronics devices and circuits": among them animations of passive devices, passive filters, diodes and their usage in electronic circuits, LCD, LED, LD (Fig. 5), OLED, photodiode, laser diode, e-paper, as well as BT, HBT, FET transistors, amplifiers, real and ideal MOS structures, examples of planar technology produced diodes, bipolar junction transistor and CMOS gate, optical storage media, digital circuits and gates (Fig. 6).

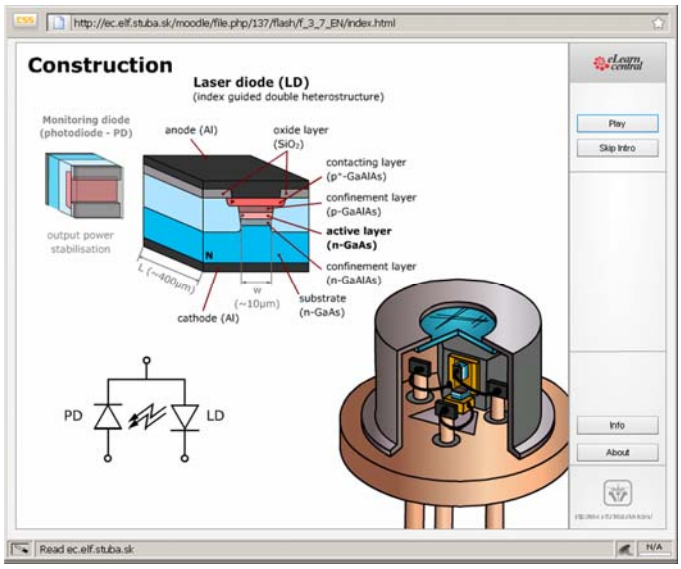

Figure 5. Interactive Flash animation Laser diode: "Intro" part construction with laser diode and monitoring diode [10]

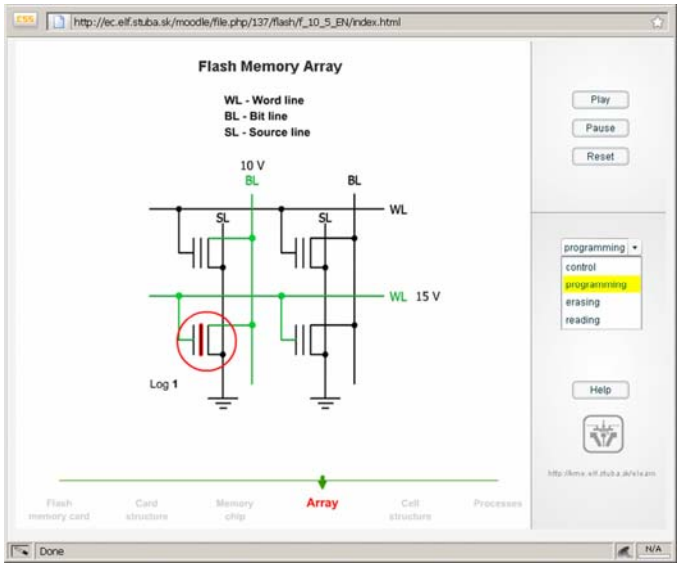

Figure 6. Interactive Flash animation Secure Digital Memory Card: "Flash Memory Array" – Programming

Figure 7. Visitor´s view of the Student menu "Electronic devices and circuits" interactive site map of the course content.

These original animations are uniqueness of our portal. All interactive animations are free available for everyone interested [11].

C. *The quizzes*

All quizzes were created in Moodle XML format with our "questions and answers editor" This editor allows various question types to be mixed in a single text file and this format supports even popular Multiple-Choice option, line comments, question names, feedback and percentage-weighted grades etc. Results are listed in %. The best results are stored in users' accounts. The user is informed about these results in the case he repeats the test. The lessons have been supplemented by one/two of two types of interactive self testing modules „Quizzes for Fast revision of knowledge" and „Quizzes with a feedback possibility". By the quiz for fast revision, students can see not only their results in %, but after finishing the test also expected correct answers.

By the quiz with a feedback possibility, if the student does not answer correctly, the quiz automatically redirects him straight to the text related to actual question. The student has an opportunity to read through the educational text again and repeat the answer after that. He/she may proceed in carrying out the quiz only if his/her answer is correct.

There are available at least 5 various quizzes with 10 multiple-choice questions supporting single or multiple answers in both types of modules.

D. The glossary

One important and very useful option in Moodle is the possibility to create a glossary of terms, which can be maintained by the instructor or collaboratively by students. All terms edited in a course are auto-linked with the glossary so they can be stored and reused in other courses on the whole portal.

We decided to use this ability of Moodle to create our own glossary to help students to better understand the specific technical terms. Now the glossary has more than 300 explanations and our goal is to prepare all terms used in our education texts to this form.

E. Two versions of the course

The course "Electronic devices and circuits" was prepared in two language versions Slovak and English. The ambition to create the English version of this course (Fig. 7) originated from the fact, that our faculty annually provides the study process also for foreign students. The second but not less important objective was to present our study programs and activities in wider scope. There are several differences between Slovak and English version of the course. The content and education form of English version is slightly adjusted for needs of foreign mainly self studying students [12].

This English version is also extended with interactive navigation map of the course content (Fig. 7). The map is dividing all course chapters into the tree structure. After mouse click on each block, the desired theme is displayed, which means that you don´t have to browse between single course weeks in Moodle environment.

The final modifications and customizations of English course version are still performed.

F. The offline e-coursebook

According to the fact, that the interactive www course "Electronic devices and circuits" is successfully used as an active support in educating the same named subject for five years now, we decided also to create the offline e-coursebook. So in 2009 we have published the offline version of the course "Electronic devices and circuits" in a form of electronic publication on cd with its own ISBN. We hope that this kind of study material will be helpful for those, who have no instant access to internet and appreciate all the interactivity of our courses.

III. SUMMARY

We have created an extensive eLearning source of information - interactive www course "Electronic devices and circuits" to enhance the quality of traditional teaching methods. The initiative to start such a project dates back to 2004 when also the "eLearn central" team was found, as a group composed of teachers and students. The members of our team have worked together and consulted all arose technical and software difficulties. The first version of eLearning course "Electronic devices and circuits" was created in 2006 and tested among students. Since this time the course has undergo various changes according to needs of our students and other visitors of the educational portal.

The complete course "Electronic devices and circuits" in Slovak language today includes 10 compact lessons, more than 30 interactive animations, glossary with more than 300 terms, several interactive self testing modules and number of hypertext references. The content of this course is regularly updated in order to follow the newest trends and research in the field of electronics.

Our experience with implementing the course to the educational process is very positive and we can observe the interest of students to use the interactive study material every school year not only to prepare for their exams, but also to find some additional information.

All the interactive Flash animations were created as a result of permanent two-way effort of "eLearn central" team. New members of the team were able to integrate and make complicated animations quite quickly thanks to our prepared templates, multimedia schoolbook [13, 14] and a library of our symbols. Most of the interactive animations in our courses are processed in very popular form and this is one of the ways how we are able to draw also the attention of younger people and motivate them to study electronics.

If we want to come close to wider range of so called customers of our work, speaking of potential students, students, partners or enthusiast, we need to meet actual demands. According to them we have prepared the offline e-coursebook of our educational material and also English version of the course "Electronic devices and circuits".

ACKNOWLEDGMENT

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eLearning as a support in education of young experimenters

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Abstract—**The paper presents the authors' motivation, experience in a design, development and a realization of the interactive course "Semiconductor materials and devices electrical characterization". This course is oriented on the preparation and start of young experimenters research activities in the SemiTest Laboratories. These laboratories on the Department of Microelectronics at Faculty of Electrical Engineering and Information Technology, Slovak University of Technology in Bratislava are responsible for investigation of the semiconductor materials quality and device reliability by capacitance-voltage measurements, current-voltage measurements and deep-level transient spectroscopy technique. The course "Semiconductor materials and devices electrical characterization" is assigned mainly for students working on individual projects in these laboratories. This eLearning project is accessible on the educational portal „eLearn central".**

Keywords- interactive web course; eLearning; semiconductor materials and devices; flash animations; SemiTest laboratories

I. INTRODUCTION

At the present time the information technology is important part of human life. The increasing volume of information requires the implementation of the most effective education processes in practice. These progressive technologies including eLearning, offer a wide range of applications and are characterized by creativity and interactivity.

The greatest advantages of eLearning: e.g. multimedia elements, time and place independence, wide information sources inspired authors to use this form of education as support by teaching the students – young experimenters – who are participating in the research activities in the SemiTest Laboratories as a part of their study individual projects.

A. Individual projects on Department of Microelectronics

Students' individual projects are very important part of Bachelor Study Programme Electronics and Master Degree Programme Microelectronics at Faculty of Electrical Engineering and Information Technology, Slovak University of Technology in Bratislava.

Bachelor projects engage students of third year Bachelor Study Programme Electronics. The main aim of these projects is to absorb the knowledge related to methods and techniques of handling relatively large projects. They should be able to show the ability to solve complex problems quite individually and creatively and according to modern methods and instructions used in sphere of Electronics. The students firstly have to master the problematic by finding and processing the corresponding references, than analyze the issues and as a result they must submit their final thesis in writing and also present it orally.

Diploma projects and Diploma thesis involve the students in first and second year of Master Degree Programme Microelectronics. As a part of these projects, students have to master the methods and techniques of solving difficult tasks involved in Microelectronics field. They must learn how to individually and creatively handle complex problems within experimental projects according to modern methods and instructions used in this sphere. Essential part of their work is to gain the ability to analyze all possible solutions leading to suitable result and create models if it is needed.

These projects are focused on educating students so they can easily integrate into working process. During the projects on Dept. of Microelectronics, students get the opportunity to become co-workers of researchers in research activities. It is very important to ensure the high quality conditions for realization of these projects as we need them to be completed successfully.

B. SemiTest Laboratories on the Dpt. of Microelectronics

SemiTest laboratories as a part of the Department of Microelectronics at Faculty of Electrical Engineering and Information Technology serve for research and analyzing of semiconductor materials and structures. These laboratories exploit techniques like current-voltage measurements, capacitance-voltage measurements and deep-level transient spectroscopy.

There are three basic automation measuring workplaces in this laboratory:

Capacitance – Voltage measurements workplace deals with a high frequency capacitance-voltage (C-V) method [1 - 3], non-equilibrium C-t method [4], a time-domain constant capacitance (cC-t) technique [5] and their limitations. C-V, C-t and cC-t measurements are being performed using the 4280 1 MHz C Meter/C-V Plotter Hewlett-Packard, Agilent

4284A 20Hz-1MHz Precision LCR Meter. The output data are stored e.g. with programs HERMES, IRIS...

Current – Voltage measurements workplace exploits the Keithley measurements set up (Keithley 238 High Current Source Measure Unit and 237 High current source measure units, Keithley 478 High Voltage Source Measure Unit - picoampermeter/ voltage source, Keithley 617 Programmable Electrometer, all with computer control system) [2] and also Agilent Technologies N5767A System DC Power Supply, Tektronix TDS3054B eScope Four Channel Digital Phosphor Oscilloscope. This workplace is controlled by program DCAT, etc.

Workplace for measuring Deep Level Transient Spectroscopy (DLTS) serves for identification of parameters of deep traps in semiconductors. DLTS workplace has two complex equipments: new Digital DLTS system DL8000 Accent (Fourier DLTS) and a Polaron Bio-Rad DLTS spectrometer measurement equipment with a boxcar detection system for acquiring the DLTS output signal [6, 7]. Both equipments use liquid nitrogen cryostats.

These methods are used to determine the semiconductor material quality and device reliability [8, 9]. Semiconductor materials and devices have a pre-eminent technological position because of their importance in integrated electronic systems building for wide range of applications. A key ingredient of this technological dominance has been the rapid advance in the quality and processing of materials and devices.

The researchers, teachers and students working (operative) in SemiTest laboratories need sufficient information about the measurement equipments and software; knowledge about physical processes in measured structures and also the set-up possibilities of real automatized measuring stations is needed. Student participating in the research activities of SemiTest laboratories in individual and team projects have only very short time for learning basic knowledge mentioned above. And often we also meet with the basic knowledge gap. This knowledge is very specific; therefore assistance of teachers and research workers is indispensable.

One of the ways how to create a database of educational material and research papers concerning study topic; to make study process more effective, more attractive, easier; is to design web interactive course "Semiconductor materials and devices electrical characterization" [10].

II. THE COURSE "SEMICONDUCTOR MATERIALS AND DEVICES ELECTRICAL CHARACTERIZATION"

This eLearning project is a standard interactive course in a course category "Electronics" accessible on the educational portal „eLearn central" (http://ec.elf.stuba.sk). The current version of „eLearn central" uses a course management system Moodle 1.9 [11]. Moodle (Modular Object-Oriented Dynamic Learning Environment) is a software package for internet-based courses and web sites producing. It is an open source software.

The course "Semiconductor materials and devices electrical characterization" deals with electrical measurement techniques: current-voltage measurements, capacitance-voltage measurements, a deep-level transient spectroscopy and barrier structures - Schottky structure, PN junction, MOS structure and transistor investigated by these measurements.

The focus is set on the basic principle of these methods and the set-up possibilities of real automatized measuring stations in our SemiTest laboratories [1 - 6].

The course was made as a modular system (Fig. 1), which was divided to the three different levels

- The first level is representing diagnostic methods. This level is oriented on automation measuring workplaces in the SemiTest Laboratories and basic principles of measuring barrier structures (Fig. 2 - 4).
- The second level defines barrier structures which are measurable by diagnostic methods – Schottky barrier structure, PN-junction, MOS structure and transistor. This level can be used as a support for face to face education of subjects dealing with these topics (Fig. 5).
- The third level is concerning with single measurements applied on ideal and real structures and examination of their behavior (Fig. 6).

Graphic design of the course is processed so that the user can see how the structures are related to measurement methods (Fig. 1). The users have displayed the entire scheme of the course and thus have access to all methods of measuring the individual structures. After passing the mouse cursor over each button, the related topic is highlighted. The individual buttons serve as links to information prepared for easy intuitive learning.

A. The format of course lessons

If a student enters the course, he can see three basic parts (Fig. 1). The main part is in the middle – Topic outline. After the first information: News forum, The aim of course, How to study in this course and Course authors follows an Interactive site map of the course (Fig. 1) and seven topics with educational materials.

On the left side there are blocks: People/Participants; Activities/Forums, Resources, SCORMs; Administrations; Random term in glossary.

On the right side there are blocks: Latest news, Virtual tours in SemiTest laboratory, Upcoming News and Recent activity.

The course "Semiconductor materials and devices electrical characterization" includes seven lessons, sixteen interactive flash animations and a number of hypertext references. The basis of an educational text in this course is composed by Diploma Thesis, Dissertations and papers presented on domestic and international scientific conferences and in journals produced during research activities in the SemiTest Laboratories.

The course lessons were created by an adaptation and conversion of the education text according to the requirements of Internet studies – eLearning. The lessons were converted into SCORM packages (Fig. 2 - 5).

Figure 1. Visitor´s view of the Student menu "Semiconductor materials and devices electrical characterization"; interactive site map of the course content

The specification SCORM (Shareable Content Object Reference Model) was developed by ADL - Advanced Distributed Learning [12]. It is a model defining relations among course components, data models and protocols with the aim to permit interchange of these courses among individual learning systems satisfying the SCORM specification.

SCORM helps define the technical foundations of a Web-based learning environment. At its simplest, it is a model that references to a set of interrelated technical specifications and guidelines designed to meet high-level requirements for learning content and systems.

SCORM currently provides an Application Programming Interface (API) for communicating information about a learner's interaction with content objects, a defined data model for representing of this information, a content packaging specification that enables interoperability of the learning content, a standard set of meta-data elements that can be used to describe learning content and a set of standard sequence rules which can be applied to the organization of the learning content. SCORM packages were developed using a software THESIS Professional.

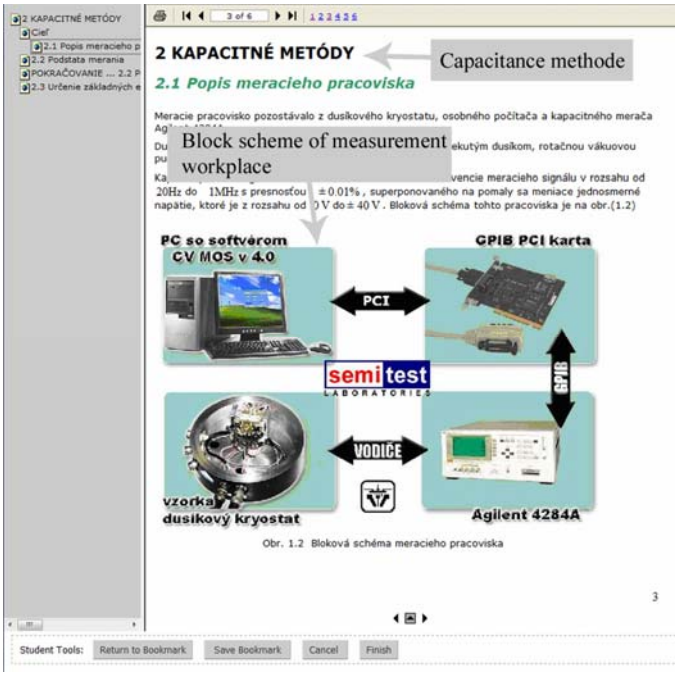

Figure 2. SCORM lesson – "Capacitance methods" – Description of measurement workplace

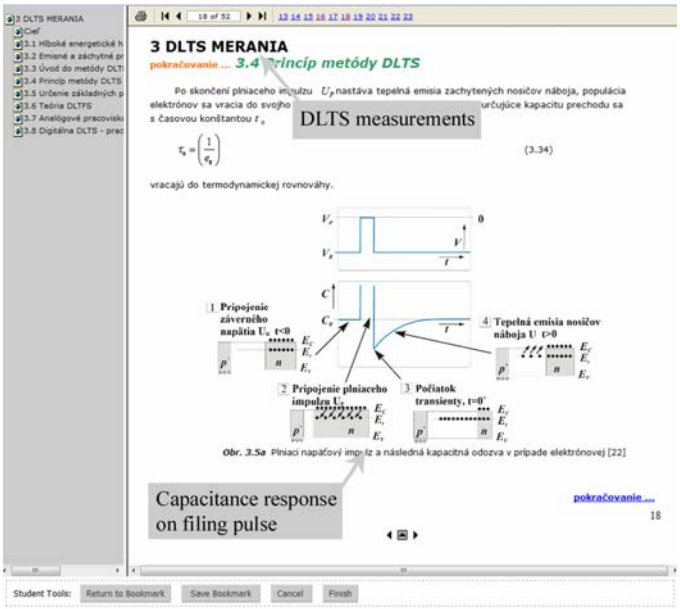

Figure 3. SCORM lesson – "DLTS measurements" - The principle of DLTS method

Each lesson is introduced with a definition of study objectives. The lesson texts had to be divided into short well-defined units enriched by content-related schemes, illustration photos and images. Each lesson has also prepared a printable version of the educational material in pdf format. The texts were complemented by numerous navigation elements (Fig. 2 - 5), such as the active navigation menu bar on the left side of the screen. It provides a full lesson content overview, so that the student just selects the topic and the matching study section

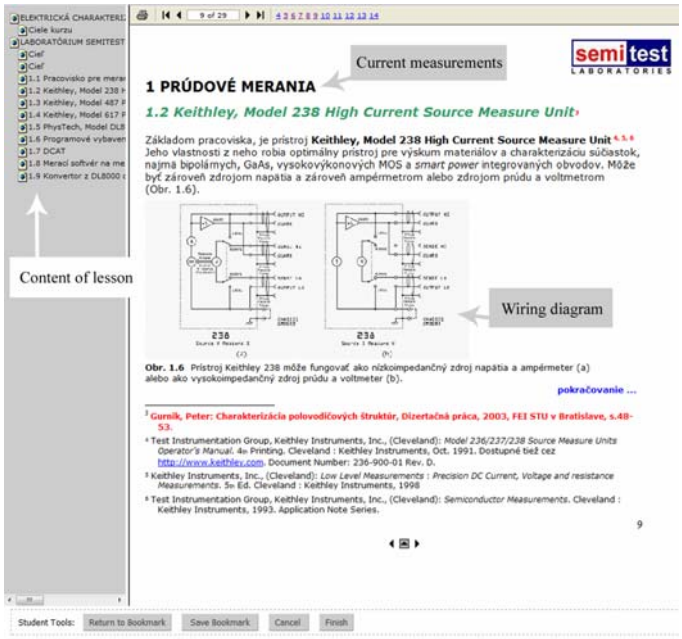

Figure 4. Student's view of the SCORM lesson –"Current measurements" – Kethley, Model 238 High Current Measure Unit

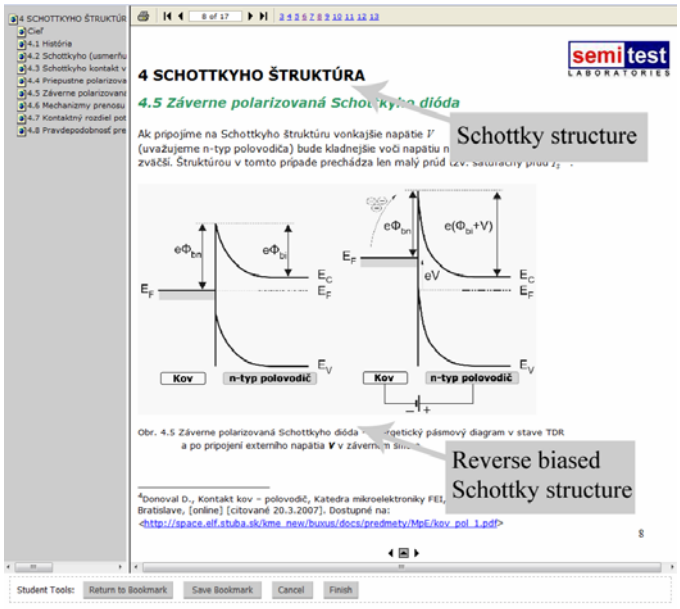

Figure 5. SCORM lesson – "Schottky structure" - Energy diagram of Schottky structure at reverse bias.

immediately appears on the screen. Further navigation elements include the arrows in the page heading and footing. In the case a text exceeds the page scope, the active continuation link enables to jump to the next page.

The new part of course is also hyperlink on databases of research articles about Gallium nitride – very perspective semiconductors wide bandgap materials. This database has been creating by students – young experimentations in diagnostic laboratories at Dept. of Microelectronics [13].

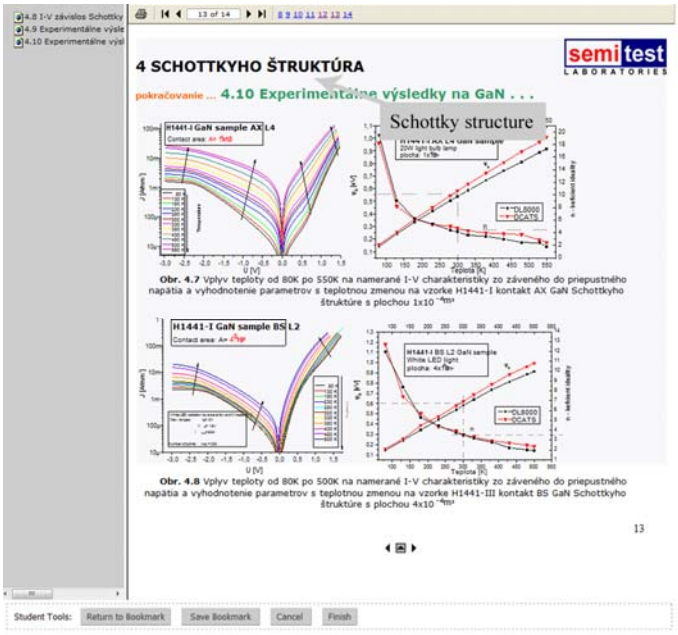

Figure 6. SCORM lesson – "Schottky structure" -
The experimental results on Schottky structure on GaN.

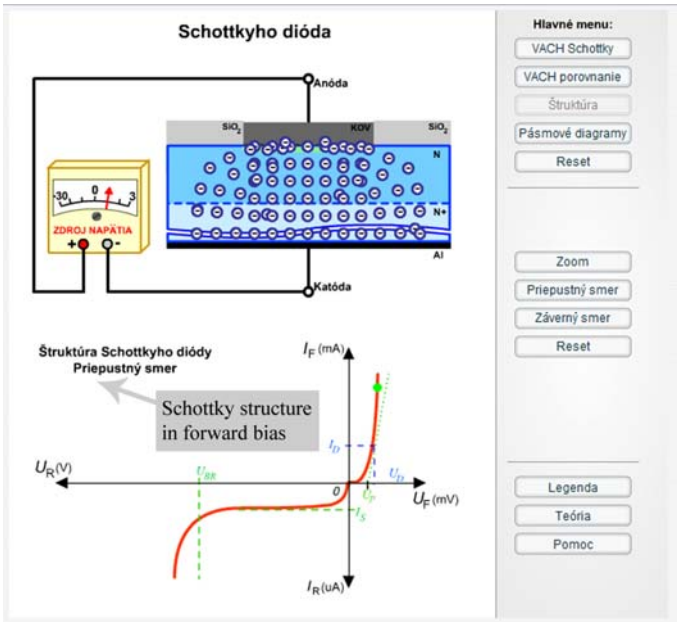

Figure 7. Interactive flash animation – "Schottky structure" -
The inner processe in Schottky structures in forward bias

B. *The interactive flash animations*

Sixteen interactive animations developed in Adobe Flash are added in this course. These animations are displaying inner processes in Schottky structure (Fig. 7), pn junction, MOS structures and work with software Hermes. Our goal was to help the students to understand these processes and measuring procedures through various interactive animations. The animations have been designed in such a way that they would show animated details of a given object and so help obtaining the knowledge much easier and faster. These original animations are uniqueness of our portal. All interactive animations are free available for everyone interested [14].

III. CONCLUSION

The initial plan was to use the potential of eLearning in education for young experimenters. We used our practical knowledge of designing eLearning courses on educational portal "eLearn central" and our long-term experiences with experimental work in Semitest laboratories.

The course "Semiconductor materials and devices electrical characterization" is being developed by members of the eLearn Central Team. It is a result of cooperation of teachers and students participating at individual and team projects. All our outcomes are a result of reciprocal interactions between teachers and students in the „eLearn central team".

Nowadays the course is in a process of updating of the educational materials. The modular structure of the course allows the course to be innovated constantly according to users' demands.

This course is accessible on the portal "eLearn central" for students on the link http://ec.elf.stuba.sk with access rights only. The aim of this course in future is to prepare the complex educational study material for students participating in the SemiTest Labs' research activities. During the course creating process we have used well known benefits of the e-learning.

The implementation in practice will show, whether we can help students in their work in SemiTest Laboratories in this way.

ACKNOWLEDGMENT

Authors' acknowledgment goes to all who participated on the development of this course; most of all to the Dr. P. Gurnik and Dr. M. Ťapajna, for their huge effort and participation on building SemiTest laboratories and team co-workers Ing. M. Benkovič, Ing. R. Šramatý, Ing. M. Vallo, Bc. M. Petrus, M. Hanáček and many others.

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EURO-DOTS : A new EC Support Action for Doctoral Training in Europe

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Overall objectives of the Support Action

The EURO-DOTS (Doctoral Training Support) action is aimed primarily at improving the offer and the quality of training proposed to European PhD students. It helps fulfilling the new requirements for ECTS credits imposed to PhD students by major European universities for obtaining the Doctoral (PhD) degree in Engineering.
A coherent set of advanced courses in micro/nanoelectronics explicitly accredited by major European universities in the framework of their Doctoral Program, will be made easily accessible to European PhD students, offering the opportunity to collect ECTS credits thorough Europe.
The global objective is to create a delocalized (virtual) platform for supporting the Doctoral Schools in Europe in micro/nanoelectronics.
The courses will respect specific organization criteria (short, intensive one-week modules with optional exam) that will make them very flexible, accessible and attractive as well for high-level continuous education of engineers from industry.
Scholarships will be made available to PhD students for boosting the start-up of the project, while other sources of scholarships will be explored for the long-term continuation of the project.

PhD students and scientific background

The field of Micro/nanoelectronics has reached today a high-level of complexity and is entering in a period of major moves. As a matter of fact:

- In this "more Moore" era for CMOS, major challenges are appearing at the level of deep sub-micron technologies, characterization techniques, device physics, device models, circuit design techniques using low-voltage and leaky devices, spread of device parameters, power dissipation and many others.
- In the so-called "More than Moore" domain, new opportunities are emerging every day with the capability to combine a wide variety of components in a SoC or SiP and microsystems approach, opening the door to numerous innovative applications in RF, automotive, biomedical and numerous others.
- In the "beyond CMOS" field, totally new components are issued from disruptive research, including SET, nano wires, CNT and others, that request to reinvent circuit and system design techniques.

In the framework of the basic engineering curriculum (Bachelor and Master degrees), it is nearly impossible to cover all these fields in detail up to the state-of-the-art level. For this reason, doctoral training programs (doctoral schools) have been created for allowing PhD students to select a set of advanced courses that fit their needs for their PhD thesis.

New rules imposed by major European universities for PhD students

Requirements imposed to PhD students for obtaining their degree have known a significant evolution during the last few years, taking into account the increasing complexity of the engineering fields as explained here above.
Even if some differences exist between universities, typical rules can be summarized as follows:

- Strict admission requirements;

- Final admission after one year, conditioned by the approval of a jury, on the basis of a sound research program;
- PhD students must follow a doctoral training program and collect a total of 12 ECTS credits ;
- Research progress reports must be produced annually;
- At least one scientific publication in an international journal and/or presentation of a paper at a major international conference in the field is mandatory;
- A final PhD exam must be presented in front of an international jury within a timeframe of four years;

ECTS Credits (European Credit Transfer System)

ECTS is a learner-centered system for credit accumulation and transfer based on the transparency of learning outcomes and learning processes. It aims to facilitate planning, delivery, evaluation, recognition and validation of qualifications and units of learning as well as student mobility. ECTS is widely used in formal higher education and can be applied to other lifelong learning activities.

ECTS credits are based on the workload students need in order to achieve expected learning outcomes. Learning outcomes describe what a learner is expected to know, understand and be able to do after successful completion of a process of learning. They relate to level descriptors in national and European qualifications frameworks.
Workload indicates the time students typically need to complete all learning activities (such as lectures, seminars, projects, practical work, self-study and examinations) required to achieve the expected learning outcomes.
60 ECTS credits are attached to the workload of a full-time year of formal learning (academic year) and the associated learning outcomes. One academic year corresponds to 30 weeks of courses.
Therefore, for intensive, modular courses such as the courses considered in this doctoral program, a one-week course, Completed by the personal work and exam, corresponds to 3 ECTS credits.

Credits are awarded to individual students after completion of the learning activities required by a formal program of study or by a single educational component and the successful assessment of the achieved learning outcomes. Credits may be accumulated with a view to obtaining qualifications, as decided by the degree-awarding institution. If students have achieved learning outcomes in other learning contexts or timeframes (formal, non-formal or informal), the associated credits may be awarded after successful assessment, validation or recognition of these learning outcomes.

Problems to be addressed

Today, Engineering Schools or Universities are confronted with the problem of organizing high-level doctoral programs covering several engineering fields at the state-of-the art level, i.e. in direct connection with research. Especially in view of the increasing multidisciplinary nature and content of the emerging research domains, a broad but in-depth coverage of related problems has become indispensable. If major European universities are at the top level in some specific research fields, they can however hardly cover the whole domain of microelectronics and microsystems, both for scientific and financial reasons. The doctoral program they can offer is therefore restricted to some fields, and can hardly cover all the special topics that could be requested by innovative PhD topics.

On the other hand, for PhD students, the choice of doctoral-level courses is mainly restricted today to local courses for various reasons:

- foreign courses are hardly accessible because most courses are spread on a full semester at a rate of 1 or 2 hours per week;
- the cost for attending the few existing modular, intensive courses is actually prohibitive for students;
- ECTS credits are usually not offered today for these courses (no exam organized, no official recognition of the courses);

Another problem to be addressed is the fast moving field of microelectronics and microsystems. Some disruptive developments are expected in these fields in the near future, requesting a rapid and coherent answer of the doctoral courses and/or continuous education courses in order to maintain Europe at the state-of-the-art in R&D. An evaluation of medium and long term needs in high-level courses is therefore mandatory.

This has been since the very beginning one of the salient objectives of the ETCB, the Education and Training Coordinator Board of the European Nanoelectronics Research Platform ENIAC (the European Nanoelectronics Initiative Advisory Council). It was emphasized that the mission of the Nanoelectronics-related research teams in academia was not only to perform ground-breaking research in the relevant areas but also to provide education and experience to graduating students to allow them to successfully pursue a career in Nanoelectronics. Matching the 'technology push' from the science and engineering community with the 'market pull' from the industrial partners and end-users, is essential to ensure that the research is industrially and economically relevant and maximally beneficial to society. This engages academia and industry alike. For this purpose the ETCB had proposed a Strategic Action Plan in which a survey and assessment was to be made of the Education and Training (E&T) curricula in European Universities in nanoelectronics, complemented with an identification of the near and long term needs of industry, an analysis of the supply gap and finally the establishment of an E&T Roadmap that would close the gap. Essential in all of this is that the selection, preparation and adaptation of relevant course modules would be very dynamic and able to respond quickly to identified needs and adequate to address also professionals. As it became obvious that such rapid and in-depth adaptation of courses at master level is rather limited and nearly impossible, it has also been decided by the ETCB to focus primarily on PhD course modules and to include ease and room for adaptation as one of the important criteria. The plan was approved by the ENIAC SCC and the CSA proposal submission received full endorsement.

Some existing experience at the origin of the concept of this Support Action

- Modular, intensive one-week courses (3 ECTS credits including report and exam) offer a good formula that eases the participation to courses in different countries/universities for European PhD students;
- Such high-level, well-focused modular courses address both PhD students (Doctoral School) and engineers from industry (continuous education, see also the ENIAC E&T mission).
- This formula has been successfully experienced with PhD students during the last 4 years at EPFL, where the summer courses in microelectronics have been officially accredited by the Doctoral School. ECTS credits are offered after the successful presentation of an exam. (In 2008, more than 60 such oral exams have been organized in this framework).
- Both IMEC/KULeuven and MEAD/EPFL actually already offer several such high-level modular courses. Their fields are complementary, covering respectively technology and MEMS at one side and Circuit Design at the other side. Moreover, a close cooperation is foreseen for the creation of design courses for technologists, and technology courses for designers (for which already modules exist, such as a Technology Aware Design package at IMEC).

- STU Bratislava is developing and offering the advanced courses related to complex characterization of advanced semiconductor materials, structures, devices, circuits, and systems based on complementary electrical, analytical and optical characterization methods. Increasing sensitivity and resolution down to nanometer region is a very important part of those courses.

Concept of the Support Action

The present Support Action is aimed at addressing the problems described here above. It involves:

- A study of medium/long-term needs in advanced education in micro/nano-electronics;
- A survey of available and appropriate course offerings at European Universities and/or Education & Training centers, that could fulfill the imposed requirements;
- The creation of new courses based on these surveys, filling the gap in existing courses, as necessary and the set-up of a comprehensive set of doctoral-level, modular courses in microelectronics. These courses will progressively cover the full field ranging from advanced device physics and technology supported by advanced characterization techniques to circuit and system design, and address state-of-the-art questions in the so-called “More Moore”, “More than Moore” and “Beyond CMOS” domains; The creation of a framework that would allow PhD students to easily get ECTS credits throughout Europe : financial support, accreditation of courses for PhD ECTS credits, organization of exams, etc. A certificate of attendance and of successful completion of the exam would be issued to PhD students, mentioning the corresponding number of credits. However, the full and unique responsibility for delivering the doctoral degree remains of course at the university of origin of the student.
- The attribution of scholarships to PhD students that fulfill the imposed conditions. Scholarships that are included in this proposal are necessary for the smooth start-up of the European Doctoral School. Other sources of scholarships, such as People (Marie Curie), will be studied during the course of the project and will be proposed for the long-term continuation of the action.
- Proposed scholarships will cover approximately half the costs of the PhD student fulfilling the rules. Considering that the total costs include the course registration fee, travel expenses and subsistence, the scholarship will be limited to the coverage of course registration fee

The organizing consortium consists of partners that have ample experience with such pan-European course offering and that are prepared to join forces in working out a workable concept. It includes IMEC (BE), EPFL (CH), KUL (BE), MEAD (CH), KTH (S) and STUBA (SK). The Action is however totally open Several major Universities, Research and Training Organizations will be consulted in the course of the project and calls will be open for course proposals.

As mentioned above, close links will be established with ENIAC. The EURO-DOTS Support Action fully fits within one of the Objectives of the ETCB (Education and Training Coordination Board) . Moreover, also links with EUROTRAINING and other European initiatives will be explored. The partners in the present consortium are active members of both Actions and are therefore in good position to guarantee this coordination. Last but not least, whenever appropriate, links will also be established in due time with the EIT (European Institute of Technology).

This Action is aimed at paving the path towards a delocalized (virtual) platform for support of the European Doctoral Schools in micro/nanoelectronics in Europe

Old IDESA and New IDESA-2: European Training Programs for Implementation of DSM CMOS ASICs

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Abstract—**IDESA is an EC funded European program for training in VLSI implementation in DSM CMOS technologies that started in 2008. In this paper the outcome of IDESA and lessons learned are discussed and the new IDESA-2 training program is announced.**

Keywords-CMOS; VLSI; deep submicron; training

I. INTRODUCTION

The semiconductor industry introduces a generation of CMOS manufacturing technology approximately every two to three years. The mainstream technologies now are 90 nm and 65 nm while 45 nm is already available in several fabs and 32 nm is expected to reach industrial maturity soon. Although deep submicron technologies down to 65 nm are accessible for EU universities, adoption of these technologies in research and training has been rather slow. The economical obstacles – high silicon prices – have been partially overcome by means of the Europractice Mini@sic model and EC subsidies for university designs in deep submicron technologies [1]. There is, however, another obstacle. Deep submicron (DSM) design flows and tools are much more complex than traditional ones and require new knowledge and skills. To facilitate transition to DSM technologies, the IDESA "train the trainers" training program was launched in 2008, with a series of 4 "hands-on" courses traveling across Europe and 22 advanced seminars recorded and available from the IDESA Web site in multimedia format. All course material and seminars can be freely reused at European universities. The satisfaction level of the participants in the IDESA courses is very high. To extend the impact of IDESA and update the courses with topics relevant to the most advanced state-of-the-art processes, the IDESA-2 project will start in September 2010. The purpose of this paper is to summarize the outcomes of IDESA, discuss the lessons learned and introduce IDESA-2.

II. IDESA AND ITS OUTCOMES

A. Facts and Numbers

IDESA involves 8 partners active for many years in VLSI design: imec, EPFL, TU Delft, RAL, Slovak TU, UT Warsaw, KU Leuven and CEA-LETI. The partners jointly developed 4 advanced courses: an analogue IC implementation course, a RF IC implementation course, a digital IC implementation course and a design for manufacturability (DfM) course. These courses were repeated 7 times each spread over 17 locations in Europe. Table I shows the number of courses and course locations in the 12 countries in which the courses were organized. The IDESA consortium tried to find course locations in the East, West, North and South of Europe in order to make the courses easily accessible for attendees from all EU member states and other European countries. The geographical coverage shown in Table I is quite good. One of the courses (DfM) was given in four locations only (in the UK, in Italy, in the Czech Rep. and four times in imec, Belgium) due to limited number of institutions interested in hosting this course. The reason behind this will be addressed later in this article.

TABLE I.

Country	No. of Locations	No. of Courses
Belgium	2	9
Czech Rep.	1	1
France	1	1
Greece	1	2
Italy	2	2
Poland	3	3
Slovakia	1	2
Spain	1	1
Sweden	1	1
Switzerland	1	1
The Netherlands	1	1
UK	2	4
Total	17	28

Due to generous EC support the participation costs could remain very low: 50 EUR per course day. The participation fee included attendance to all course sessions, extensive printed materials, refreshments and in many cases also free lunches. The participants had to cover their own travel and lodging costs.

As an addition to the courses, a series of tutorials addressing a broad range of specific advanced topics have been prepared by invited experts (most of them not from the project

IDESA and IDESA-2 are funded by the 7th Framework Program of the European Union.

consortium). These seminars were presented in front of live audiences at imec and recorded. 22 of them are now available online from imec Microelectronics Training Center servers [2].

Development of the courses (including extensive course materials and logistics - software support for hosting institutions etc.) was a significant effort: more than 800 person-days.

The total number of attendees was 428 persons from 26 countries. These countries included 21 EU member states and Belarus, Russia, Serbia, Switzerland and Turkey. Six EU member states, among them the Baltic states, were not represented. The highest numbers of attendees (30 or more) were from Belgium, Spain, UK, Italy, Germany and Poland. Table II illustrates the geographical distribution of the course attendees.

TABLE II.

Country	Number of course attendees				
	Total	*Analog*	*RF*	*Digital*	*DfM*
Austria	3	1	0	1	1
Belarus	1	0	0	1	0
Belgium	65	16	11	14	24
Bulgaria	2	2	0	0	0
Czech Rep.	16	6	0	5	5
Denmark	1	0	0	1	0
Finland	7	1	1	3	2
France	8	6	1	1	0
Germany	37	9	4	19	5
Greece	24	12	6	4	2
Hungary	1	0	0	1	0
Ireland	5	1	1	3	0
Italy	50	14	5	24	7
Norway	8	2	3	2	1
Poland	30	16	8	6	0
Portugal	2	0	2	0	0
Romania	1	1	0	0	0
Russia	4	0	3	1	0
Serbia	6	0	6	0	0
Slovakia	10	5	1	4	0
Spain	53	9	30	10	4
Sweden	21	3	14	4	0
Switzerland	9	5	0	4	0
The Netherlands	12	2	1	8	1
Turkey	1	0	0	1	0
UK	51	14	14	10	13
Total	428	125	111	127	65

Among the attendees there were 238 PhD students and teaching assistants, 88 academic teachers and 103 researchers and designers. They came from 132 institutions. This is about 20% of the estimated European academic teaching staff and PhD students potentially interested in the courses. IDESA-2 will be launched to expand the penetration.

The average number of course attendees was between 16 and 18 at the analog, digital and RF courses. This means that almost all these courses were fully booked. The average for the DfM course was at 60%.

B. Some Problems and Solutions

1) *Course Development and Delivery:* The courses have been prepared by international teams including academic teachers and researchers from partners' institutions: imec, EPFL, TU Delft, KU Leuven, UT Warsaw. Each course had its leader responsible for course development. Thanks to the very good understanding between the partners this turned out to be a relatively easy task. However, delivery of the courses, and in particular organization of the computer lab exercises, created initially serious technical and logistical problems. Each of the four IDESA courses consists of lectures and computer labs with "hands-on" demonstrations of design tools and techniques. Nearly half of the overall course time is allocated to these lab exercises. Each course participant has to carry out a set of particular design tasks him- or herself. Such "hands-on" courses are usually organized on the site of the course provider, where all the technical infrastructure is readily available. In IDESA this is not the case. Each course was given for the first time at the site of the IDESA partner responsible for it, but the subsequent courses were traveling across Europe, where every hosting site had somewhat different hardware, network infrastructure, operating system versions etc. Many hosting sites did not have all the software tools and/or sufficient number of software licenses. This problem has been solved by RAL together with software vendors by making the necessary software and temporary license files (valid until the end of each course) available. The hosting site made their servers available remotely for the authors of the lab exercises, allowing them to check the software installation and make sure that everything worked as expected before start of the course. In this way technical problems have been successfully overcome. In IDESA-2 the same course organization framework will be used.

2) Marketing the Courses: Another problem was to spread the information about IDESA and its offering as widely as possible. Despite numerous e-mail based info campaigns (e-mails sent to all EUROPRACTICE members), conference presentations, the IDESA Web site and links from other Web sites (e.g. [4]) the IDESA team members learned many times that many academic teachers and PhD students potentially interested in IDESA courses were not aware that such high quality and low cost courses existed. It is not easy to deliver the message to all interested people when mailboxes are full of all sorts of commercial advertisements and spam... This problem will also exist in IDESA-2 and more effort will be needed to spread the information about the project and its offering.

3) Registration: One more problem was how to organize the registration process. It was decided to arrange a single Web based registration site at RAL. This site (linked to the

main IDESA Web site [3]) provides detailed information about the scheduled courses, handles registration and payments. RAL is also the "IDESA interface" to the course hosting sites. Registration for IDESA-2 courses will be also handled via the same RAL-hosted Web site.

4) Access to Design Kits: The registration process included arrangement of individual non-disclosure agreements for the course participants. Imec has successfully negotiated with TSMC conditions of availability of PDK of their 90 nm mixed signal CMOS technology. Each course participant has to sign a personal NDA before the course and send a copy to imec. In this way it became possible to base all the exercises on a real industrial DSM process.

5) Academic Perception of Design-for-Manufacturability: Few universities volunteered to host one of the DfM course sessions. At the same time, the level of subscription for the DfM sessions was 40% below the average for the analog, RF and digital implementation courses. Manufacturability issues, however, do have a significant impact upon the IC implementation flows for 65nm and beyond. Analog, mixed RF and purely digital circuits are all affected. Increased marketing and PR actions for the DfM topic have failed to raise the interest to the level we have seen for the other courses.

C. Outcomes and Lessons Learned

All courses were evaluated by the attendees. The evaluation forms were extensive, included detailed evaluations of the contents of the courses, quality of teaching (overall and for individual trainers) and organizational aspects. Suggestions how to improve the courses were welcome. These suggestions will help to make the IDESA-2 courses even better.

In general, the course attendees were very satisfied with the course contents, the style and quality of training and the materials provided. Most attendees declared that the courses they attended were very relevant to their current and/or future work. Many also declared their intention to reuse the course material in their training activities. Among those who didn't some attendees considered the course material too advanced for their teaching. Another obstacle indicated was lack of access to the software used in the courses, in particular the ADS toolset from Agilent for RF design, which is not available via EUROPRACTICE. Most of the attendees also declared an intention to submit deep submicron designs for fabrication in the future, but not in 2008 or 2009.

The lab "hands-on" sessions were indicated as the most valuable component of the courses. It seems that the level of theoretical knowledge among the course attendees was quite high (although not equally high in all courses and on all topics), but what was missing were practical design skills. Indeed, design and verification of complex designs in deep submicron technologies involves a number of new tools or steps not easy to master, with lots of new functionalities and options. This is the reason why many attendees suggested longer lab sessions, asked for reference material related to the tools used and for more design examples.

The numbers presented in Table II indicate that while the analog, RF and digital design courses were very popular, the DfM course turned out to be of somewhat lower interest. However, in post-course feedback most DfM course participants agreed that the lecture material was of essential importance to their design activities. In hindsight, the students regretted any initial hesitation to attend. Quote:"I was in the DFM course and it was very good. I would like to send 2 more staff as soon as possible. Do you have dates for the next DFM sessions in 2010?"

The main outcomes of IDESA can be summarized as follows:

- the vast majority of the participants rated the courses as very good,
- practical lab sessions were considered as especially valuable component of the courses,
- many attendees declared that after the courses they would design their first chips in deep submicron technologies,
- most attendees from universities declared that they would reuse the course materials in their teaching,
- while the analog, RF and digital design courses were very popular, the DfM course turned out to be of somewhat lower interest. Additional work needs to be done to convince academia that a focus upon DfM is essential to implement functional and reliable circuits. Manufacturability is not about technology, manufacturability is about design.

The overall outcome is definitely positive. It is worth noting that in the first half of 2009 the number of 90 nm designs submitted to EUROPRACTICE for prototyping was higher than in the whole 2007 and 2008 despite economic difficulties. In order to stimulate the application of the knowledge acquired in the IDESA courses, Europractice again organizes design contests in 2010. Applicants can win free prototyping on a 90nm mini@sic run. [5]

The economic crisis clearly had some adverse effects on IDESA. High travel costs forced many potential participants from such non-EU countries as Belarus and Ukraine to cancel their course registrations despite travel grants of 300 EUR per person offered to them.

III. IDESA-2: Similar, But Not Exactly The Same

The IDESA-2 project, which starts in September 2010, will continue the main activities of IDESA. The course contents will be updated where necessary, taking feedback from IDESA courses into account. However, the overall scheme of the courses will remain the same. Again, each course will be repeated seven times in various places in Europe. The portfolio of advanced seminars will be extended with new topics. The proposals are being collected now.

It is planned to open the courses to design engineers from European SMEs. However, to avoid unfair competition with commercial course providers, the non-academic course

attendees will have to pay a participation fee in line with market prices for commercial courses.

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Teaching CMOS Circuit Design in Nanoscale Technologies Using Microwind

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Abstract—**This paper describes the experience in teaching integrated circuit design using an educational tool called Microwind through a Project-Based Learning approach. The evolution of the tool in the context of technology scale down is described, with focus on nanoscale technologies. An evaluation of the courses taught in two institutions (INSA France, and UniSA Australia) shows high levels of student satisfaction.**

Keywords- Integrated circuit design, VLSI Design, nanometer technology, project-based learning, lifelong learning.

I. INTRODUCTION

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nanoscale technologies for industrial production of high performance integrated circuits (IC). Table 1 gives an overview of the key parameters for technological nodes from 45 nm, introduced in 2007, down to 11 nm, which is supposed to be in production in the 2015-2018 timeframe (Fig. 1). Mass market manufacturing with the 32 nm technology is scheduled for 2011 [1] [2].

TABLE I. TECHNOLOGY ROADMAP DOWN TO 11-NM

Technology node	**45 nm**	**32 nm**	**22 nm**	**16 nm**	**11 nm**
First production	2007	2009	2011	2013	2015
Effective gate length	30 nm	25 nm	18 nm	12 nm	9 nm
Gate material	Metal	Metal	Metal	Dual?	Triple?
Gate dielectric	High K	High K	Very High K	Very High K	Very High K
Raw Mgates/mm^2	1.5	2.8	5.2	9.0	16.0
Memory point (μm^2)	0.3	0.17	0.10	0.06	0.03

Shifting to a new technology node impacts upon the design methodology, and requires improved technology models and tools to accurately predict the performances of the circuits. Engineering students need to be abreast themselves with the rapid changes in technology and design practices. Courses in IC Design [3] [4] must also aim to equip students with the skills of independent learning and lifelong learning. Due to time constraints in a semester long course it is often not feasible to introduce students to complex commercial design tools and at the same time expect them to develop practical circuit design skills and independent learning skills.

We present project-based approaches to teaching adopted in two institutions in Australia and France, both aimed at actively engaging students in stimulating learning experiences for the development professional design skills using the latest semiconductor technologies. We also illustrate the educational tool Microwind [5], developed to support the design of CMOS basic cells and well suited to project-based learning approach. In this paper, we focus on educational developments, teaching challenges, proposed design flow and associated tools in the light of these issues. We also present evaluation of the courses by UniSA and INSA students based on the same evaluation questionnaire.

II. DEVELOPMENTS IN CMOS TECHNOLOGY

A. General Trends

The introduction of every new technology node in the past years has represented massive improvement in MOS device performance. At the transistor level, the channel length of MOS devices is automatically scaled with a new technology node. Roughly speaking, the node corresponds to half of the gate layer pitch, although the definition differs depending on the application domain. Two approaches have been introduced recently to improve transistor current capabilities:

- Decreasing the oxide thickness t_{OX}. The oxide thickness has been reduced to 1.2 nm (5 atoms). Unfortunately, the gate oxide leakage is exponentially increased, which increases the standby power consumption. Starting with the 45 nm generation, so-called “metal gates” have been introduced, based on Nickel-Silicide (NiSi) or Titanium-Nitride (TiN), as illustrated in Fig. 2(a) and (b).

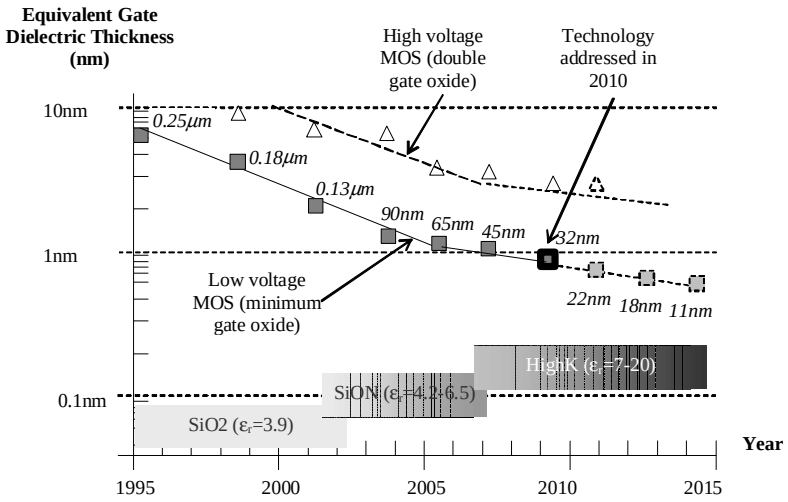


Fig. 1. Technology scale down and nodes, down to 11 nm.

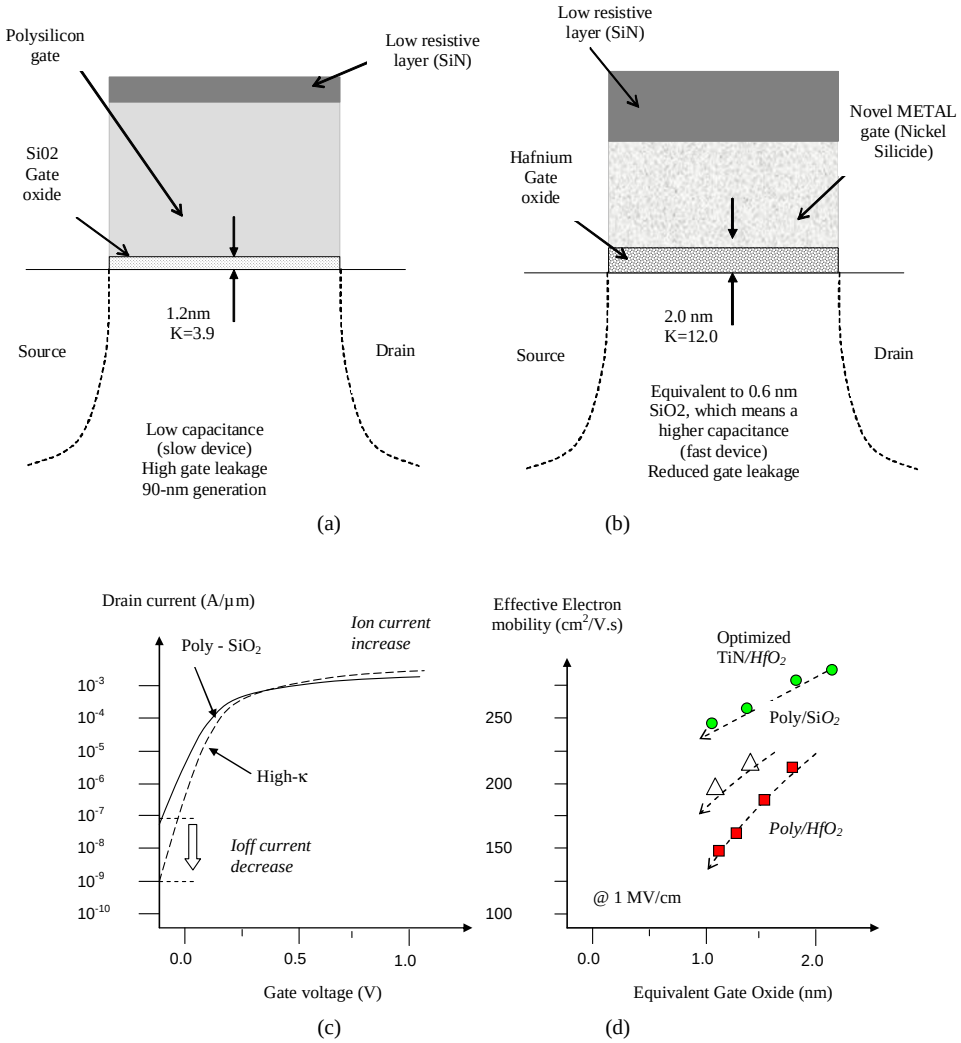


Fig. 2. Compared to poly/SiO2 gates (a), the metal gate combined with High-K oxide material (b) enhances the Ion current and drastically reduces the *Ioff* current (c). Electron mobility vs. Equivalent gate oxide thickness for various materials (d) from [4].

- Increasing the carrier mobility μ. Starting with the 90 nm generation the concept of strained silicon has been exploited to enhance the carrier mobility, which boosts both the n-channel and p-channel transistor performances. The 3rd generation of strain engineering used in the 32 nm technology massively boosts MOS performance [1] [2].

B. *Challenges*

It is acknowledged that the students need to develop as lifelong learners if they are to adapt to the rapid technological changes and the consequent changes in design concepts and methodologies. In addition, it is necessary for them to develop the important graduate qualities of problem solving and critical thinking in order to successfully operate in a continually changing and challenging field of VLSI Design. It is therefore important to consider the following issues:

- The commercial chip design tools available today are very powerful, and are capable of capturing the design and verification needs of modern ICs. However, these tools are highly complex and need long time to learn.
- It is very important for students to develop thorough understanding of the complex process technologies [3] [6] and their impacts on design alternatives using intuitive 2D/3D technology visualizations. Therefore it is necessary to use design tools that are not only less time consuming to learn but also provide intuitive design, simulation and visualization environments.
- Student diversity must be considered. From a pedagogical perspective, any gap in the background knowledge must be addressed first before effective learning of new concepts and skills can occur.

III. PROPOSED EDUCATIONAL SCENARIO

In order to address the design tool issue both UniSA and INSA courses use a set of user friendly design and simulation tools, namely Microwind and Dsch [5]. These tools and associated text books [7] [8] incorporate the most recent CMOS technologies and provide an interactive learning environment for the development of skills in design and analysis of integrated circuits.

A. *Educational Approach*

The design courses proposed to students for physical design of layout-level functional blocks include:

- An introduction to the technology scale down and its impacts on device integration, performance and design challenges.
- A tutorial on MOS devices, based on problem-based learning, introducing width/length effect, *Ion/Ioff* and *Vt* illustration, for both N and P devices (Fig. 3). To develop skills in modeling [3] and simulation the set of user-accessible SPICE model parameters is reduced to around 30 most important ones for BSIM4.
- The design of inverters, and a simple ring oscillator, and a small student contest to achieve the maximum oscillating frequency on a common technology node.
- The design of basic logic gates introducing interconnect design, compact design strategies, and impact on switching speed and power consumption.
- The design of analog blocs introducing amplification, voltage reference, addition of analog signals, and mixed-signal blocs [4].
- A capstone design project, e.g. microprocessor.

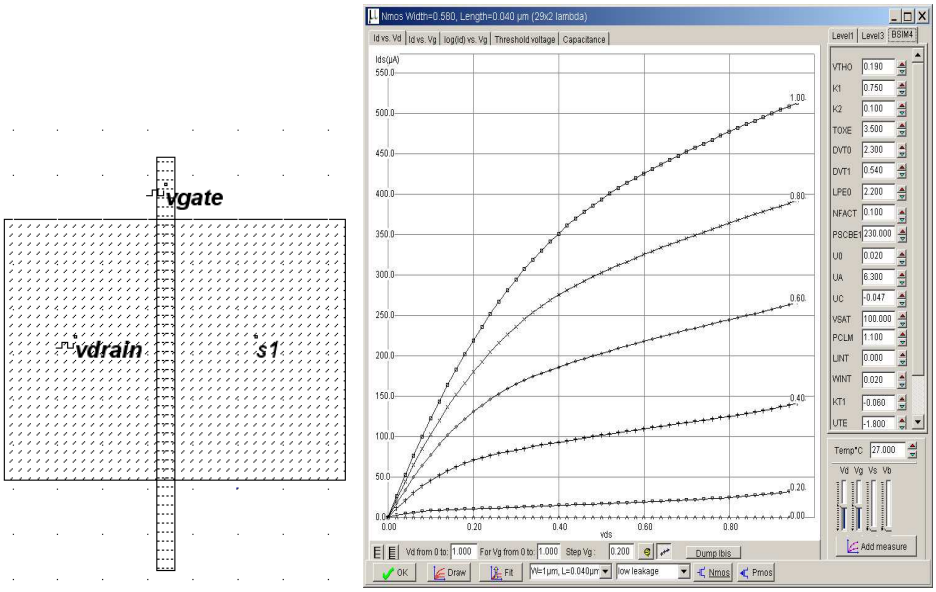


Fig. 3 : Student drawing of a MOS device with simulation properties (left), corresponding I/V curve using BSIM4 (right).

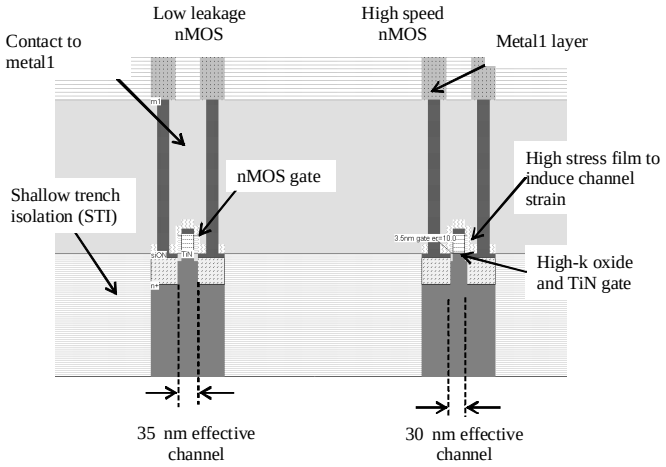


Fig. 4. 2D cross-section of Low-leakage/high speed MOS.

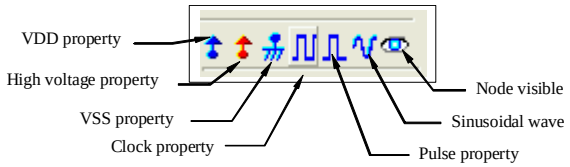
B. *Design Tool*

Microwind is a CMOS circuit editor and simulation tool, for logic and layout-level design, running on Microsoft Windows. It has been developed since 1998 through several versions, and is available as a freeware (lite version [5]) for educational purpose, and sold to universities through Ni2designs, India. Microwind allows students to draw the masks of the circuit layout (Fig. 4a), use a set of simulation properties (clocks, pulses, DC voltage sources, Fig. 5a) to build a test scenario, and validate the current/voltage relationships through built-in analog simulation (Fig. 5b). Our approach aims at giving students immediate confidence to design MOS devices. The approach consists of a step-by-step illustration of the most important relationships between the layout and its performance. We concentrate on 2D (Fig. 4), 3D views (Fig. 6), static and dynamic characteristics (Fig. 5), and the MOS model parameters that are considered most significant for educational purposes (Fig. 3-right).

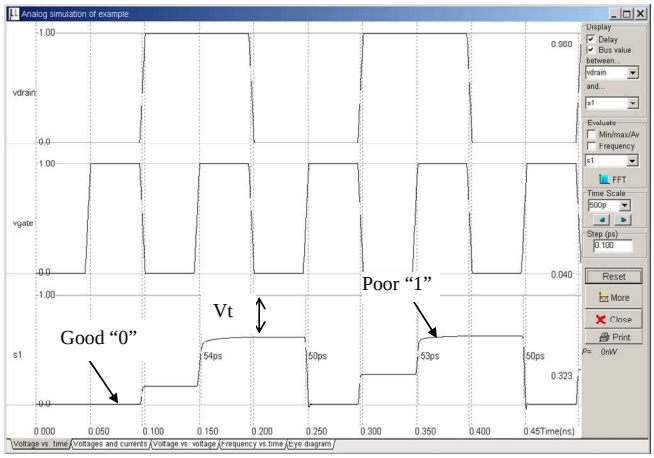
Through careful investigation of the simulations students are able to gather information about the key properties and drawbacks, for example junction capacitance effect that samples undesired intermediate voltage, threshold effect that jeopardizes the high voltage levels, and ultra-fast charge/discharge (in the picoseconds range). Microwind's layout library (MOS generators, and Cell compiler from Verilog-HDL description) is used progressively to ease the layout design phase.

C. *Project-Based Learning*

Project-based learning methods have been developed for the IC design courses at both UniSA and INSA. UniSA offers a course titled *VLSI Design*, which focuses on Digital CMOS IC design. It is offered in Masters by coursework programs and also as a final year course in undergraduate programs. Students are expected to have the necessary background knowledge and experience in digital logic design and electronics. The issue of student diversity is addressed by following a structured project-based approach. At INSA a similar approach is adopted for an introductory course titled *Physics and Modeling of Semiconductor Devices*, which is offered in the first year of a two-year *Masters* program *in Automatic Control and Electronics*. However a more open-ended approach is adopted in a second year course titled *Analog CMOS Circuit Design*.



(a)



(b)

Fig. 5. Properties added to the layout (a), and time-domain simulation of the MOS using BSIM4, showing analog memory effect due to junction capacitance and threshold voltage drift (b).

At both UniSA and INSA, the aim of the project-based learning (PBL) approach is to engage students in a stimulating learning experience for the development of professional design skills, and for the development of independent and lifelong learning abilities. The students do simple projects in the early stages using step-by-step *self learning guides*. Critical questions and increasingly complex tasks are gradually scaffolded within the projects.

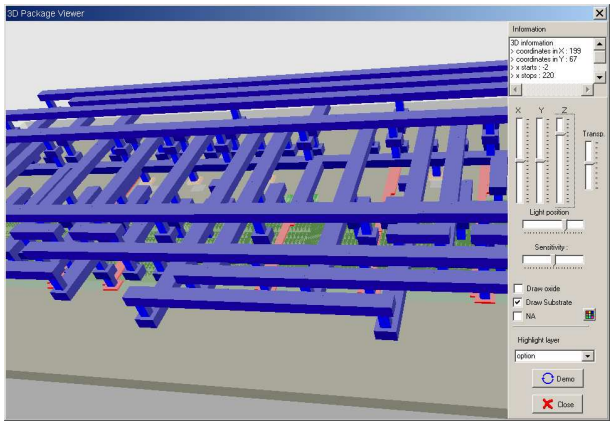


Fig. 6. 3D viewer showing the interconnect structure of a ring oscillator designed by students, with zooming and rotate functions.

These early projects, done mostly in a self learning manner, assist students in

- Reviewing/developing fundamental concepts
- learning how to use the design tools
- developing problem solving/critical thinking skills
- developing independent learning skills

On completion of each of the early projects the students get the satisfaction of designing a circuit that performs some useful function. This is helpful for confidence building and motivation, particularly for the students who are new to the idea of independent learning and whose previous educational experiences may have been quite different from the engaging PBL approach. The projects gradually increase in complexity requiring students to engage in deeper problem solving and critical thinking [9]. Finally there is a capstone project on designing a microprocessor which challenges students by putting the knowledge and skills they have developed to test.

Students develop design skills at layout level, are able to optimize the layout to increase speed, reduce the silicon area, and to check the layout for design rule violations (DRC). They gain valuable experience on the challenges involved in designing and simulating complex integrated circuits and are ready to explore professional tools available to industry.

IV. Evaluation By Students

The IC design courses at INSA and UniSA were evaluated anonymously by students using the same questionnaire. The courses at both the institutions consistently received high rankings in all the evaluation items. In the last five years, on average more than 90% of the respondents expressed satisfaction with the overall quality of the courses [9]. The project-based strategies were also evaluated using the specially developed questionnaire given in Table II. Fig. 7 presents the student responses to the questionnaire using a Likert scale of 1 to 5 (1–strongly disagree, 5–strongly agree). Clearly the students found the PBL strategies very useful for their learning.

TABLE II

Questionnaire for Evaluation of the PBL Approach

#	Question statement
1	I was able to work out how to use the CAD software by using the project handouts provided
2	I was able to learn circuit design techniques on my own by doing the projects using the project handouts
3	The handouts assisted in revisiting some of the background knowledge required for the course
4	The questions given in the project handouts helped me to think critically
5	The projects helped me put the theory of VLSI Design into practice
6	The final capstone project challenged me to test my learning in the course
7	I feel confident about completing similar capstone projects independently
8	The skills I learn in VLSI project work are useful to me
9	Overall I am satisfied with the project-based learning approach used in the VLSI Design course

V. Conclusions

The use of the educational tool Microwind that enable students to develop circuit design skills using modern deep submicron technology has been one of the underlying factors for the successful delivery of the digital and analog integrated circuit design courses in two institutions in Australia and France. Engaging students in design work involving a range of latest technologies has enabled them to understand the impacts of technology scale down on factors such as speed, power and noise. Using project-based learning methodologies suited to the teaching context, digital and analog IC design courses have been delivered with high levels of student satisfaction. Collaboration among faculty members at the two institutions has led to the production of a range of learning resources to support students through project-based learning and to assist them in developing independent and lifelong learning skills. These resources are available at www.microwind.org and http://tiny.cc/UniSAVLSI.

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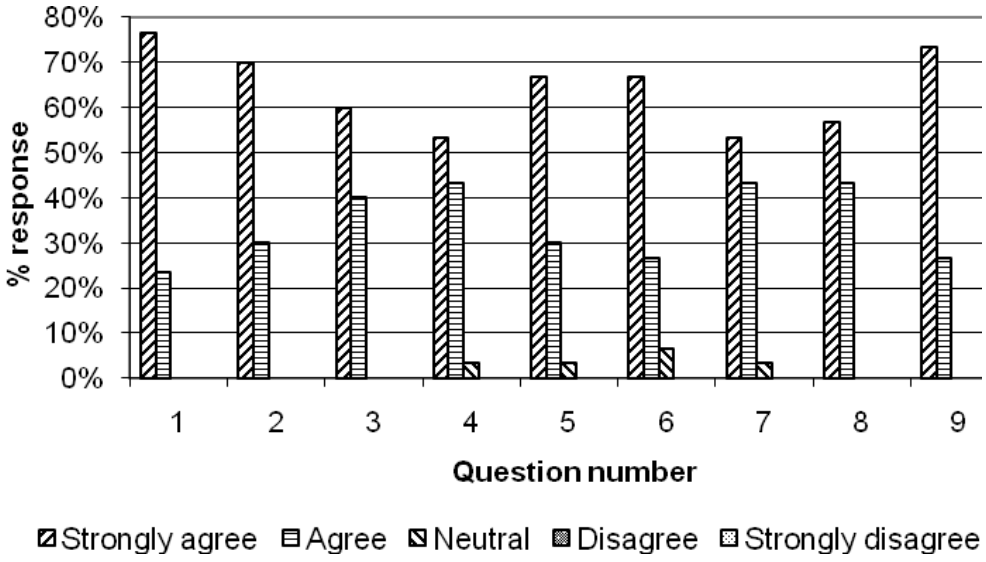

Fig. 7. Student responses to evaluation of the PBL approach, from [9].

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A Pilot Course in Vital Electronics

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Abstract

Vital Electronics, Testbench, Innovation

This paper describes the paradigm of "Vital Electronics" (defined in the text) and an associated pilot course. Vital electronics is the response to the challenges of the "post VLSI era," to restore the enthusiasm and interest of students in microelectronics systems. This approach can be integrated within I-GEMS [1], an IEEE-sponsored Global Design Environment, for reliable nano to global scale Critical Embedded Systems.

1. Vital Electronics

Vital Electronics is the study and use of electrical components, circuits, networks, and systems to achieve a design goal of protecting, saving, and improving critical infrastructure, and hence the quality of life. Vital Electronics' domain is a heterogeneous computing environment derived from sensors networks, embedded systems, and ambient intelligence with intelligent, robust, and trustworthy nodes capable of building **Application-Centric Embedded Computers** from "off-the-shelf" virtual computational and networking parts.

Vital Electronics makes Embedded Computers more capable, reliable, energy-efficient, and optimized to their tasks. These Embedded Computer inhabit our critical infrastructure and other key applications, at increasingly low-levels, and with increasing interconnectedness with their peers. At the same time, Vital Electronics enhance the ease, and speed of the design of reliable Embedded Computers, and their associated Embedded Systems through the reuse of proven and certified "design elements," and other "virtual components."

Vital Electronics is founded on the synergistic interaction between Moore's Law, Metcalf's Law, High-Level System Design Tools and MEMS Sensors and Actuators. The increasingly capable Programmable Systems on a Chip (PSoC) such as Cypress Semiconductor's PSOC family with its companion PSoC Creator tools are the key building blocks of Vital Electronics

2. Course Description

Our initial planning assumed two courses in Globally Integrated Security Environment (GISE), run simultaneously, one in the United States and another in Germany [2]. To reduce complexity, logistics, and distance learning challenges, it was decided to focus the Pilot Course on Vital Electronics, as the cornerstone technology segment of GISE.

The course was organized around a hands-on introduction to one such family of PSOCs developed by Cypress Semiconductor, which enables implementing reliable, low-power wireless complex sensor-centric systems incorporating up to 250 nodes. The focus was on a hands-on background in Cypress PSoC®-based Embedded Wired and Low-power, long-duration Wireless Sensor Networks. Attendees were introduced to a wide range of applications including: Home / Building Automation (Smart Grid and Security); Human Input (Cap and Touch Sensing); Medical Devices and Well-Being Equipment; Industrial Process Monitoring and Control; Security, Structural Monitoring; Sports and Leisure; Asset Management, Robotics, Public Transportation.

Cypress PSoC® devices feature: an FPGA-like programmable interconnect fabric, configurable analog and digital blocks, 8 or 32 bit CPUs, Flash program memory, SRAM data memory, and configurable I/O integrated into a variety of compact packages.

This architecture allows the user to rapidly create systems, replacing multiple traditional MCU-based components, with one, low-cost single-chip programmable PSoC device. The Cypress CyFi™ low-power physically compact Direct Sequence Spread Spectrum (DSSS) transceiver, and the logically simple, small-memory footprint lightweight wireless

network protocol stack, enables one to build wireless sensor networks incorporating up to 250 nodes to be designed using “drag-and-drop” tools.

3. Security Application-Centric Projects

There were three student projects in the pilot course. One of them was the Generic Critical Infrastructure Protection project led by Harry Charache, a student with a security, but not engineering background. The student has designed and built a sensor network called GNAT in the Critical Infrastructure Dependability Lab (CIDLab) at the University of New Hampshire as shown in Figures 1 and 2

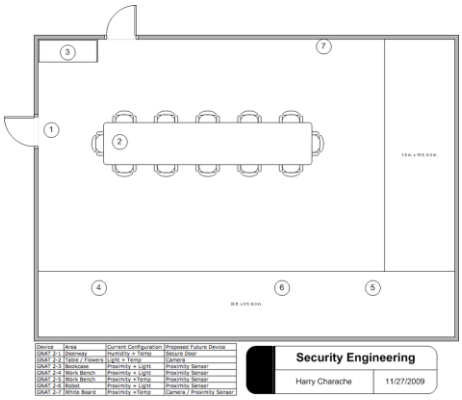

Fig. 1. The placement of GNAT2 sensor nodes in CIDLab.

Fig.2 General view of CIDLab with sensors hidden.

A series of experiments and measurements where conducted to characterize the behavior of GNAT2 computer in case of anomalies e.g. personal intrusion to the lab. The other two pilot projects included Invisible fence: Deployable Proximity Alert System (developed by former US Marine combat veteran Steve Doran) – Figure 3 shows it detecting an approaching vehicle, and Grid security, an energy grid remote monitoring system (developed by working power systems engineer Doug MacMillian).

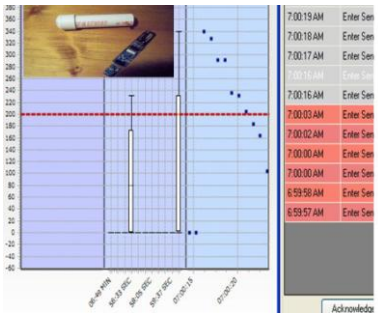

Fig.3.DPAS (inset) and detection of approaching vehicle measures the light change in CIDLab.

4. Summary and Assessment

All students have been very enthusiastic about the course and want to continue the effort the next semester. We plan to offer the course again in cooperation with our German partners. We also plan to offer the reduced version of the course for practicing engineers through the IEEE Boston Section short Course and Lecture Series continuing education program, as well as via a course introducing Vital Electronics for non-engineers. The first project is being continued as a master thesis. The third project should lead to a smart grid remote monitoring industrial application. On a negative side, despite outstanding support from Cypress, the laboratories should be reworked and enhanced to speed up the necessary learning curve.

Acknowledgement

The authors would like to thank Cypress Semiconductors for their generous support of the vital electronics program and specifically to TJ Rodgers, CEO, Patrick Kane, University Program Manager, and Professor Alex Doboli SUNY Stony Brook.

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EuroTraining
– Supporting University Programmes in Nanoelectronics

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Abstract—**This paper describes how the EuroTraining project supports a timely introduction of new nanoelectronics university programmes in Europe. The provisions include training courses, training material and training roadmaps describing the structure and content of nanoelectronics curricula. In order to facilitate the European integration of the new curricula courses based on the ECTS system are offered and training material free of copyright and IPR is emphasized.**

Keywords-training, nanoelectronics, curricula, courses

I. INTRODUCTION

The goal of the EuroTraining project is to enhance European industrial competitiveness by providing easy access to European training courses and by stimulating the development of new courses in the field of nanoelectronics. EuroTraining is concerned both with university educational programmes and with professional advancement training and maintains a web-service providing a comprehensive course directory and links to course material for university courses and for professional advancement courses.

Furthermore the project has recently provided a training roadmap describing the academic training requirements within nanoelectronics [1]. Technology roadmaps show that the development of microelectronics into deep submicron technologies (nanotechnologies) causes fundamental changes in the coming years as the scaling limits of the traditional CMOS processes are reached. These changes have impact both at the system design level, at the circuit and device design level, and at the manufacturing technology level. In order to cope with these changes, new curricula in engineering education are needed.

This paper describes how EuroTraining supports the implementation of new university programmes in nanoelectronics.

II. PROVISION OF TRAINING COURSES

The objective of the EuroTraining project is to provide a European Training Infrastructure facilitating the provision of high calibre training across Europe. The structure supports professional advancement training as well as academic training. The training action enhances the development of the European knowledge-based society in the field of nanoelectronics.

The EuroTraining action offers access to a comprehensive range of advanced training courses, course material for European nanoelectronics university programmes and employee training support. Special attention is devoted to develop and make available courses supporting the CMOS technology targeting digital components and complex digital Systems on Chip (*"More Moore");* to master diversification targeting non-digital applications, heterogeneous integration in Systems-on-Chip or Systems-in-a-Package (*"More than Moore")* and to prepare for the technology generation beyond the CMOS scaling limits *("beyond CMOS").*

The courses offered are structured in three levels:

1. *ECTS accredited courses:* European Credit Transfer and Accumulation System (ECTS). For successfully completed studies, ECTS credits are awarded. The credits facilitate the transfer and progression throughout the Union. Currently the ECTS accredited courses are mainly utilized as part of the PhD programmes.

2. *Quality Labelled courses:* The quality labelling procedure has been initiated by EuroTraining with the objective of improving the high quality of delivery of courses given by European Course Providers. Quality Standards outlines key components of effective education and allows course providers to evaluate their efforts in relation to these criteria. This evaluation procedure has the ability to check that the Course Providers are delivering high quality courses to students, and provides feedback and advice so that the quality can be improved in future courses.

3. *Other courses:* This category includes all other kind of courses or events (e.g. conferences) offered on a European level.

Annually EuroTraining offers more than 500 courses. Nearly half of these courses are either ECTS courses or Quality Labelled courses.

Since the start in 1995 of the preceding EuroTraining project 5.400 courses have entered into the web service and more than 1.2 mio. training users have accessed the service in order to find the right training. The general rationale of the project is shown in the below figure:

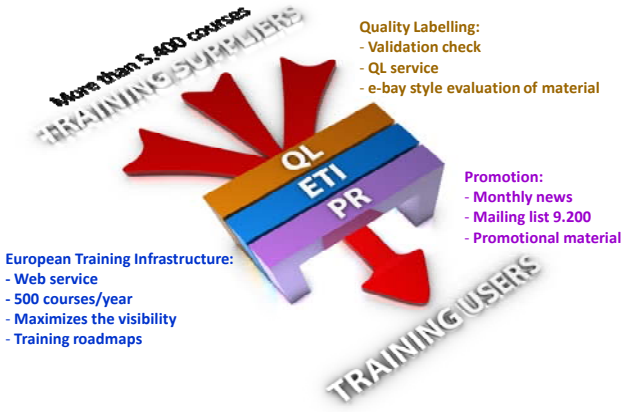

Figure 1. Course delivery from suppliers to users

III. PROVISION OF TRAINING MATERIAL

Most universities have small numbers of PhD students in each subject area for which reason they cannot afford to entirely develop their own courses. At the same time the innovation circle is becoming faster and faster. Therefore the basic development of courses, text books and training material must be shared among the universities.

The development of training material is normally a process going from writing R&D reports and scientific papers which are converted to lab exercises and lecture notes which later become an entire course. Over the years more mature course material materializes into textbooks published by international publishers. This value chain for the development of course material is shown in figure 2.

While scientific papers and textbooks are disseminated globally, the course material developed is only disseminated locally. This means that other users (universities) may have to wait for textbooks to be published some years downstream of the actual course material. By making the course material available through EuroTraining it becomes available globally and consequently new nanoelectronics courses become available much quicker.

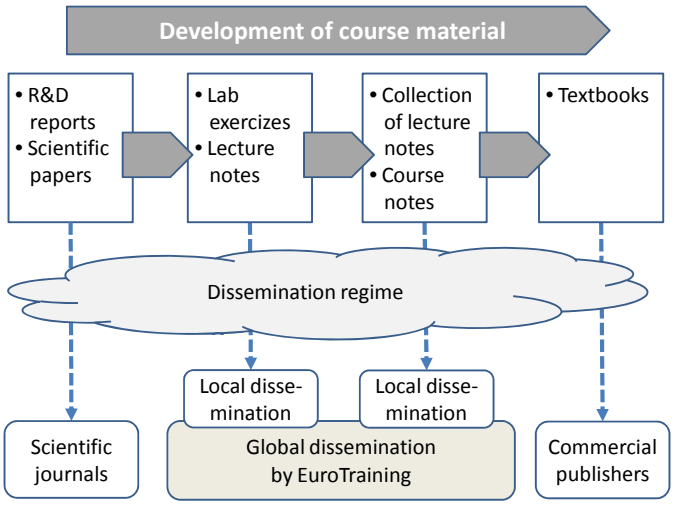

Figure 2. Development of course material

EuroTraining therefore offers a course materials brokerage facility. The course material is organized in categories supporting various technologies, e.g.:

- Materials
- Nanotechnology
- IC (Analogue and Digital)/ASICs
- Nanoelectronics
- Micro/nano systems
- RF devices
- Design Tools and CAD

The training material is structured as either a set of links to course material providers or direct access to a database containing training material that is free of copyright or IPR. In order to maintain the links EuroTraining runs a regular check of the consistency which leads to a quality label called QBIL (Quality Bank of Internet Links).

IV. UNIVERSITY CURRICULA DEVELOPMENT

Nanotechnology is having increasing impact on university curricula in electrical engineering and physics. The advent of nanotechnology brings about new possibilities in nanoelectronics, including increasingly complex systems on chip, sophisticated technology fusion between electronic devices and non-electronic devices (such as bio-devices or chemical devices), and possibilities for developing fundamentally new nanoscale electronic devices. New engineering curricula in nanoelectronics must take these developments into account.

Therefore EuroTraining has developed a training roadmap describing the requirements with respect to developing new nanoelectronics curricula. Major influencers in the development of new curricula have been defined and

discussed and a model for the development of new curricula has been presented [1].

University curricula in nanoelectronics are still in their infancy but good examples of programmes already exist. The roadmap describes some representative examples of state-of-the-art curricula from major European universities.

In the development of new curricula, important issues are:

- versatility and flexibility to bridge gaps between computer engineering, electrical engineering and physics.
- internationalization to utilize peak competences in different locations.
- Matching of the competences of newly educated engineers to the local needs of industry and society.
- teaching resources available in the form of competent teachers and teaching material.

V. FURTHER INTEGRATION OF KNOWLEDGE

Recently EuroTraining has taken the initiative to further integrate the resources made available by the huge amount of FP7 projects working on semiconductor design. This initiative is organized in a project called “R&D Access” with the aim of identifying R&D results on semiconductor design from FP7 projects and to provide these results to partners from outside the consortia. The R&D results are divided into four categories:

1. Training and Education
2. Intellectual Properties
3. Design Tools
4. Design Methodologies

The dissemination platform facilitates the access to project results generated in huge numbers of Integrated Projects (IP), Network of Excellence (NoE), Specific Targeted Research Projects (STREP) and Coordination and Support Actions (CSA) from the FP7 programme. When the platform is implemented and routines for best practice have been established also relevant project results originating from e.g. FP6, ENIAC, ARTEMIS and national programmes will be invited to join the ACCESS platform.

The ACCESS platform is based on a web system developed as an extension to already existing European services like EuroTraining, IP Design-Reuse [2] and EDA network [3]. Since these services will be improved and already have nearly 40.000 subscribers the new combined ACCESS platform will be born with a tremendous user community.

The new site will become available at www.rd-access.eu

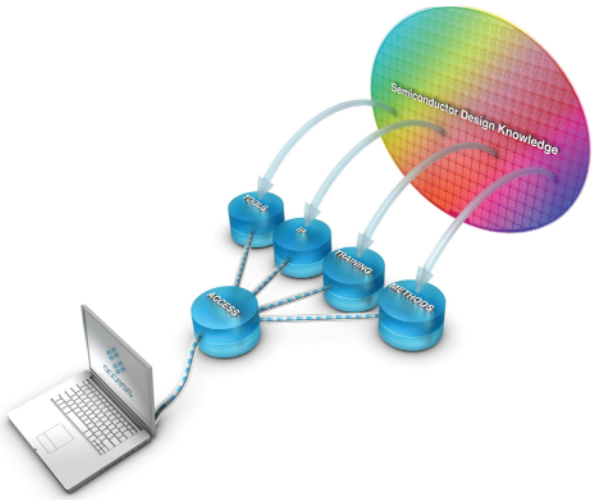

Figure 3. Integration of R&D knowledge on IP, Tools, Training and methodologies.

VI. CONCLUSIONS

Developing new university programmes in nanoelectronics require extensive resources and knowledge. Many universities cannot afford to develop entirely new programmes for which reason the work must be shared with other universities. EuroTraining supports this trend by offering access to advanced ECTS accredited training courses, training material and training roadmaps describing the requirements with respect to developing new nanoelectronics curricula.

All services offered are gathered in the European Training web site, promoting the training services and attracting participants: www.eurotraining.net.

ACKNOWLEDGMENT

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Learning-by-Gaming in HW/SW Codesign

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Abstract **— HW/SW Codesign is a part of renewed Computer and Systems Engineering Master Curriculum at Tallinn University of Technology. Already historically, practical works are related to computer game design elements on different FPGA-based prototyping platforms. Current platforms, based on Xilinx Spartan-3 chips, enable complex designs where the only restrictions are the course duration and student imagination. In this paper, the status of course along with the most interesting student design examples are provided and analysed. The students' feedback is used to refresh the course material and complexity of laboratory task set.**

Keywords – Hardware/Software Codesign, system-level design, education, computer engineering curriculum

I. Introduction

With the growing industrial importance of hardware/software codesign the necessity for educating engineers in this field is a regular part of CE curriculum around the world. But purely theoretical knowledge is impractical without hands-on experience with recognised EDA tools and advanced development platforms. The complexity of modern HW/SW design can be effectively overcome with interactive and entertaining laboratory works [1].

Game design projects are widely and successfully used for teaching programming, and it was decided to apply the same method for HW/SW codesign. In a similar work [2] an FPGA was used to implement an object detection algorithm for a robot soccer game. Although probably designed as a student project in the frame of a certain course, the paper focuses mainly on design issues.

HWSW Codesign [3, 4] has been read in Dept. CE of Tallinn University of Technology since 1998. After several redesigns of the curricula and implementation of Bologna system, it is now defined as part of the Master level curriculum of Computer and Systems Engineering at faculty of Information Technology.

The course objectives are defined as follows: After completing the course the student is expected to:

- be able to select the proper modelling languages and tools
- be aware of the design space limits and freedom in case of pure HW or SW design or in case of a blended system
- be able to analyse a model concurrently in the HW and SW contexts
- be able to partition a design on a basis of estimations and analysis
- possess the skills to implement different cross-domain interaction schemes and protocols
- be able to use standard off-the-shelf software implementations as well as IP core (soft, firm, hard) processors
- be able to analyse a design in the frame of dynamic reconfiguration on a basis of temporal quality requirements
- know the contemporary HW/SW mixed system implementation platforms and frameworks
- be able to accomplish team tasks

Currently, the course is provided during the spring semester. Students possess a significant flexibility in planning their curriculum and are free to choose whether to take the course in the first or the second year of their master studies. The course is therefore accessible to them either in the second, or the last semester.

Those students who are taking the course in the first year usually have only a limited experience with digital electronics design, but are likely to have taken the introductory course to hardware description languages (HDL-s). However, the synthesis of digital circuits has been explained at this point only in the broad strokes.

The other students may have taken one or several of the following courses: Digital System Design, Labs on Digital System Design, Computer Engineering Project, Digital Systems – Team Project, Computer Engineering – Team Project, VLSI Synthesis, System-on-a-Chip Design, and several others.

All of the listed courses are optional and as a result students arrive with a notably different background knowledge and experience. This was taken into account when planning the laboratory works for the course at hand and it is reflected in their structure.

II. Structure of the Practical Works in HW/SW Codesign Course

A contemporary laboratory part of the course was introduced in 2008. It consists of four levels in ascending order of complexity:

1. Introductory – first hands-on experience with XESS XSA-3S1000 boards [5], downloading and programming previously implemented tutorial designs.

2. Beginner – simple HW-design using VHDL or Verilog.

3. Intermediate – design of a VGA demo along with PicoBlaze controlled moving element on a screen. VGA generator is reused from one of XESS tutorials. The emphasis is on programming and instantiating of the soft-core processor and VGA IP cores.

4. Advanced – enhanced design where HW/SW trade-offs have to be investigated and results analysed.

The first lab is carried out under direct supervision and is mainly intended for those students who lack experience with digital system design in general or with the FPGA prototyping boards. Students learn the main features and capabilities of Xilinx ISE, the Xilinx Spartan-3 chip and the development board. After that student teams are free to take the development kits home and visiting the laboratory becomes voluntary. Freely available versions of the development software are enough for this course, and about half of the students found it more convenient to work at home. The difficulty level of the introductory designs is that of simple decoders and small state machines.

The aim of the second lab is to apply the theoretical knowledge of HDL-s. The designs are still simple at this level, but the students are now to pass through all the development stages – from specification to chip configuration – independently, and they are free to match or challenge their HDL and hardware knowledge by choosing an appropriate design. By doing so students usually find this work practical regardless of their previous digital design experience. However, the selected designs significantly vary and their range extends from simple arithmetic-logic units to more complex ones, such as interface controllers.

The previous two laboratory works form a solid ground for the next steps and by the third laboratory work all students are prepared well enough to combining software control with hardware components. At this point the hardware part of the design is still accomplished by putting together predefined IP blocks. The aim is to learn how to accommodate both software and hardware within a single design, and to get a feel of using programmable soft-core processors, their instruction set, features and particularities.

For better student motivation the tasks in this laboratory work had to be made interactive and with a visual feedback. An FPGA development board with an attached keyboard and a monitor would make a good platform for that – this way students get a feel of a real system, capable a complex interactive behaviour.

Since it is not the aim of this work to familiarize just with the keyboard and screen interfaces, the corresponding IP cores were provided. To further abstract the students away from the interface details, the keyboard and video controllers were accordingly adjusted for the task of this lab.

All the complexity of image manipulation is covered by the provided VGA generator, which maps the pixel data to the corresponding memory cells. Additional multi-port memory controller significantly simplifies memory access. Both video and memory controllers are freely available from the board manufacturer's website.

The configurable keyboard controller disguises the process of key recognition and, depending on the current functioning mode, issues out a short code for a pressed key set. For example, if only the “arrow” keys are used in the design, then the keyboard controller is configured to generate an encoded 2-bit word.

Generally, students are free to choose any soft-core processor they fancy, but the majority prefers the Xilinx PicoBlaze, as it is very stable, easy to use, well documented and its instruction set is rich enough for most simple control oriented tasks. PicoBlaze also performs very well in terms of die area, as it is specifically designed for the FPGA implementation.

All major components are therefore provided, but any additional functional units and glue logic are the responsibility of the students. Most of the student designs in this laboratory work are relatively simple implementations of well-known video scenarios, such as a “snake” game, a text editor or a calculator. The reason behind such selection is simple application logic, few required colours (black-and-white in many cases) and limited amount of data manipulation.

In the final laboratory work students have to design the whole system from the ground up, including HW/SW partitioning trade-off considerations. The aim is to learn how to correctly partition hardware and software according to certain constraints, such as logic area, power consumption or development time. Such analysis turned out to be very difficult for some of the students to perform, as they had little experience in digital design, and practically all failed to make exact estimations.

The required several different HW/SW partitions together with limited digital design experience represented another difficulty - now part of the application logic, which would normally be done in software, had to be implemented in hardware. In addition, the previously used IP blocks may have had to be modified to suite the application. Many found it easier to completely redesign a functional block or an interface controller than adapting an existing one. However, examining and understanding the interface specifications had to become part of the work, if that were the case.

III. An Example of a Game Design

One of the proposed laboratory works is a simple implementation of the Sokoban game [5]. “Sokoban” is a Japanese word for warehouse keeper. Basically, the job of a

warehouse keeper is to place boxes within the warehouse in an organized manner, and this is the key idea in the Sokoban puzzle. The rules are simple and yet give rise to challenging puzzles ranging from simple to extraordinary complex ones. The game consists of a warehouse made up of walls that form passages. Within the warehouse are the pusher and an equal number of boxes and storage locations. The pusher can only push a box, never pull, and only one box can be pushed at a time. The goal is to push all the boxes into the storage locations.

This application is well suited for the task in several ways. Firstly, the design is comprised of several functional modules and a fixed communication schema between them. This allowed to implement certain modules in either hardware or software without affecting the rest of the design. Secondly, the game is visually comprised of a very limited number of different objects and its logic is carried out by repositioning them on the screen. The application simply honours keyboard activity and maintains a map of the game objects. This is quite easily achieved in both software and hardware. Finally, the custom VGA engine is capable of displaying one hundred (ten by ten) predefined images on the screen.

The system consists of the game logic processor, the memories, the video controller, and the keyboard controller. The employed video standard is VESA 800x600 @ 72Hz. The reason behind the selection was the required horizontal clock frequency (50MHz) that matches the frequency, supplied by the development board. The video picture is comprised of 100 (10 x 10) image locations which form the game map. The map is stored in the map RAM, which can be accessed by the processing unit and the video adapter. Each location on the map contains an image, which are stored in image ROM and are accessed only by the video adapter. To form the right VGA signal, the video adapter keeps track of the imaginary cathode ray position on the screen and then, in order to retrieve the pixel colour value, turns first to the map RAM and then to the image ROM. This procedure is pipelined.

The memories are implemented using on-chip block RAM (BRAM). Each object image is 80 x 60 pixels in size and there are up to 16 images in the set. With a 9-bit colour depth the set would not fit into BRAM and so the images are stored shrunk in a 20 x 15 pixel aspect ratio. They are later enlarged by the video adapter by simply repeating each rows and columns of the image four times during display.

The PS/2 keyboard controller accepts the data sent by the input device, extracts the key information, encodes it for convenient processing and sends an interrupt to the processing unit. Figure 1 illustrates the apparatus setup – the development board in the centre, the VGA screen and the keyboard.

Figure 1. Apparatus setup.

Several designs with different hardware/software ratio were implemented. While the VGA adapter was reused in all configurations, the keyboard controller and game logic processor were done in both software and hardware. The Xilinx PicoBlaze processor was employed to run the software. The block diagram of the system is depicted in Figure 2.

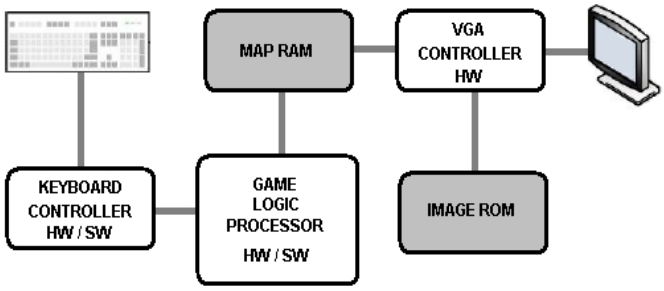

Figure 2. Block diagram of the a game system.

Students reported the following development times of various game components:

Table 1. Development times (in hours) of the game components.

	HW	SW
Game logic controller	8	16
Keyboard controller	1	3
VGA controller	32	n/a

Three different solutions, one of which was pure hardware, were then compared for development time, FPGA logic utilization and power consumption. The results showed, that the pure hardware implementation, due to a complex FSM, was not the most compact in terms of the number of used CLB-s, but required the least power and was faster to design and debug (41 hours [32+1+8] versus 43 [32+3+8] and 49

[32+1+16] for other solutions). The latter fact can be explained by larger digital design experience compared to software development of that group of students. Also, these students practised a mixed language design (VHDL + Verilog), depending on their preferences and readiness.

IV. International Concerns

English was selected as the primary course language as it is the language of a large portion of technical literature and documentation, and is planned to be part of new INTELS international Master curriculum [7] at Tallinn University of Technology. This makes the course suitable in other countries where English as a study language is in use. Generally, the required development boards or the FPGA vendors are not limited to the ones used in our university. But in any case the employed software can be downloaded from the internet at no charge and the boards, which are among the most affordable, can be purchased from the manufacturer web-site.

In addition, this course is a good candidate for blended e-learning because most of study activities can be done outside of classroom using free-ware development tools and lent prototyping kits. Most of the course materials are planned to be open course-ware available through the Estonian e-Learning Development Centre repository.

V. Course Results and Conclusions

The proposed set of laboratory works embraces the whole range of the course goals, and their accomplishment is a good indicator of whether these goals are achieved or not. Unfortunately there is not enough data to evaluate the situations when students gave up after solving the first couple of laboratory works and dropped the course. Although the majority did manage to fulfil the tasks successfully, about 30% of students failed to solve the most complicated laboratory task but a good grade is still possible when essay is presented and assessed by peer students positively.

Another demonstrative fact is that students, who successfully solved all laboratory tasks, didn't have difficulties in solving additional course tasks – analysis of HW/SW codesign related paper or thesis and a presentation of a written essay openly to extend the overall knowledge about the domain for all course participants.

Both positive and negative feedback was received during the course. Generally students appreciated the opportunity to design something real and challenging. Some of them recognized this course to be the only one during the semester which put them to work in teams with full intensity. Some of the more successful game designs are demonstrated to first years undergraduate students during the Introduction to Speciality course [8], as an example of how laboratory works can be both practical and interesting.

On the other hand a significant complexity gap was mentioned between assignments 3 and 4. Apparently a jump from component based design to fully custom was too big. In addition, complexity of the labs was overwhelming for roughly 30% of the students. The main reason was lack of HDL knowledge and insufficient number of working design examples, especially for the more complex tasks. Currently, these problems are being addressed: the tutorials are being revised and at least basics of HDL-s are compulsory for all arriving to course.

VI. Future Work

Apart from considering all the negative feedback that was previously received, future enhancements include experimenting with more powerful and flexible soft-core processors, rather that the PicoBlaze, for the following reasons:

- The general complexity of games (e.g. large number of game control states, the need for trigonometric calculations) are too often exceeding the PicoBlaze processing power.
- The PicoBlaze can only be programmed in its own assembly language, which limits the use of freely available game codes. Development of translation skills from a high-level code to assembly language is not one of the course goals.
- The PicoBlaze is designed to operate with a singe-cycle access on-chip memory. Although on-chip block memory can be explicitly rewritten using JTAG interface, there is not enough JTAG programmer modules in the laboratory to distribute along with kits. As a result the whole design has to be resynthesised by the student if the software is modified, which is very inconvenient and time-consuming. Fixing and reloading just the program is a better way to debug the system, but to do so the program must be stored in an external memory. In addition, employing only the on-chip memory would mean limiting the experience of using more capable, though slower, external dynamic memories.

Among the more powerful soft-core processor candidates is the Xilinx MicroBlaze. Being widely used in the industry, it represents a significant interest in an academic sense. It also by far outperform the PicoBlaze in the above listed areas. However, the flexibility of MicroBlaze makes it more difficult to configure and manage, demanding a significant portion of students' time during the course. Consequently, a large amount of work has to be prepared beforehand, as the current emphasis is on implementing of a learning object, which is intended to shorten learning time and to offer students a systemic set of IP-s ready to embed into real application. Another drawback of the MicroBlaze, in the frame of this course, is its restricted suitability for distant studies – the trial period of the freely available Xilinx ISE Embedded Edition evaluation suite is limited to 30 days. As the course lasts longer, student have to return to the university laboratory, where computers are equipped with full-licensed EDK tool.

Other soft-core processors, which are considered as alternatives to the PicoBlaze, include the OpenRISC processor [9] and the COFFEE RISC core [10]. A significant advantage of these two processors over MicroBlaze is the access to their source codes.

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Teaching The Principles Of System Design, Platform Development And Hardware Acceleration

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***Abstract*—Development of embedded systems composed of tightly coupled microelectronic devices and several stacks of software layers adapted to it has evolved into a more platform based design methodology. We offer a lecture in the field of ESL design that provides a broad spectrum of theoretical background. It is escorted by a laboratory where starting from a C source code a platform with a hardware accelerator for JPEG compression is designed. Small tutorials teaching basic skills of hardware modelling with SystemC and TLM are offered. Hence, we provide a course split into three teaching forms that imparts knowledge about state-of-the-art platform design together with the qualification of understanding industrial system modeling standards and tools.**

I. Introduction

Embedded system computers increasingly ease our everyday life. Cell phones, vehicles, medical equipment or home entertainment devices are unrecognizably steered by an increasing number of electronic chips. Embedded systems and their software have become the dominant driver for microelectronics and systems engineering.

Platform-based system designs are common for the class of devices mentioned above. Platforms offer advantages like short time to market, high reusability and better reliability compared to full-custom solutions. Thus the cost for consumer devices with complex but standardised technologies is kept low [1].

Our course imparts knowledge about designing these platform-based systems for students related to the field of computer science. It illustrates common techniques and mechanisms not only for design but also for implementation and verification. Hence, they are taught in every field a design is involved with.

Section II explains our teaching philosophy, which splits the corse up into three different presentation forms. The developed laboratory framework is described in section III with its detailed schedule in section IV. The student's feedback is summarized in section V, which is followed by a conclusion in section VI.

II. Teaching Philosophy

Students attending this class are already advanced in their study of computer science, information technology or electrical engineering. We offer a course with a wide variety of teaching in the field of system design and especially platform-based design. Platforms are the most common way of developing modern systems. The content is taught in three different ways: a lecture, dedicated tutorials and a laboratory (see figure 1). This differentiation ensures an optimized transfer for the theoretical and practical knowledge as described in the following three subsections.

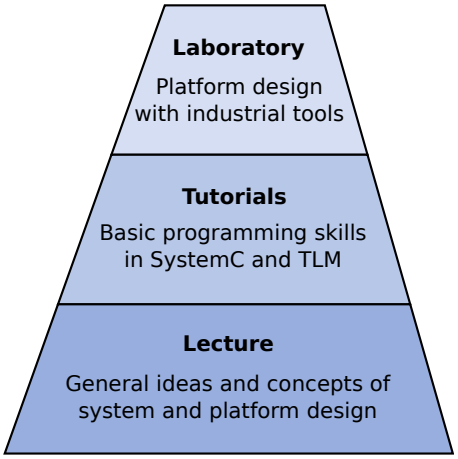

Figure 1. Course Structure

A. Lecture

Our lecture focus on teaching general concepts for system design and platforms. This is the theoretical part of our offering. It covers the various aspects of electronic-system-level (ESL) design like system-on-chip (SoC) design, bus communication, application-specific instruction set processors (ASIP), multi processor System-on-chip (MPSoC), networks-on-chips (NoC), low-power system design, test, verification and debug.

Every major topic comes along with references of state-of-the-art literature and implementation examples. These examples, either good or bad realizations, help developing a better and deeper understanding of the theoretical teaching content.

B. Tutorials

Our tutorials help to clarify the concept of the modeling language SystemC [3], [4], [5]. SystemC is one of most

common industrial modeling language and also the introduced tool Platform Creator from Coware is based on it. We experienced that getting to know how SystemC works also helps understanding how complex modelling systems like the Platform Creator are build. And this again allows developing new components for the Platform Creator like it is done during our laboratory.

Eight well chosen tutorials guide our students through the basics. The complexity of the programming tutorials increases with each new tasks. It starts with developing a 8bit counter equivalent to a HDL implementation. More advanced topics are test bench and stimulus generators. When the students get adapted to the new model language, we proceed with transaction-level-modeling (TLM). These exercises are concentrating on how communication between sources and sinks can be abstracted by invoking SystemC channels like FIFOs or buses.

C. Laboratory

The laboratory is organized in teamwork like real design teams. The idea is to enable the group of students to develop their own functional platform with the help of the Coware Platform Creator, an industrial design tool [2]. The point of origin is a generic C implementation of a JPEG compression. Integral elements of the final platform are an ARM processor, a memory mapped system bus, a system memory and a self-written hardware accelerator. The compression algorithm is tweaked so that it is executed on the ARM core together with the developed accelerator.

The students collect industrial-like experiences in many fields of system and platform design. For example the Platform Creator imparts their tooling skills with a modern design tool with industrial relevance. Additionally the Coware's tool environment allows developing the platform in a shorter time than a development from scratch.

III. Laboratory Framework

In the laboratory, our students are challenged to design and evaluate a platform for a special purpose with the industrial tool Platform Creator from Coware. In our special case we are focusing on accelerating a JPEG compression algorithm with a dedicated DCT Unit (see Figure 2). In order to achieve this goal the laboratory is divided into four working phases: tool-handling, platform design, software adaptation and JPEG acceleration.

A. Tool-Handling

When students join our laboratory they have no knowledge about the tool Platform Creator. Therefore at the beginning we offer exercises focusing on different aspects of the tool. At the beginning a sample platform is generated. This minimized system is utilized to explore the process of compiling and running an application. Since we develop the hardware as well as the software, debugging is required for both sides. It is important to mention that the tool handling is the main focus of the exercises and not developing the system.

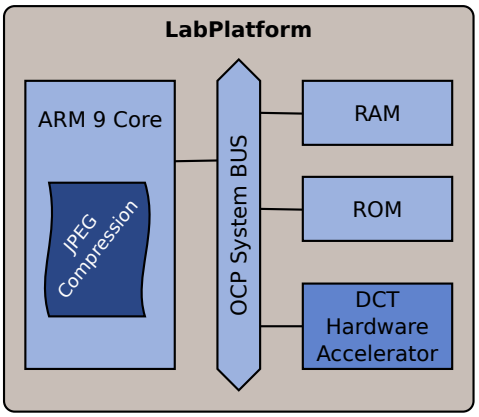

Figure 2. Platform for JPEG Compression with DCT Acceleration

B. Platform Design

Platform Creator enables developing the platform on the system level in a very elegant way. It offeres a wide range of predefined IP blocks like an ARM core or bus structures. During the first design phase the hardware accelerator is suppressed. The ARM core is connected via an OCP system bus to two memories. In order to guarantee that the platform is actually working a simple test program is cross-compiled and downloaded to the microcontroller.

C. Software Mapping

We provide a pure C implementation for our students which is not meant to run on the platform built in the previous phase. Their task is to adopt the source code to the new environment. Major distinction is the fact, that no file system is present on the target platform. Hence, an important step is to model all I/O accesses as memory requests. This includes that the input data have to be prepared for the software modification. The students are asked to realize their own approaches.

The Platform Creator allows to debug the hardware system as well as the downloaded software. A SystemC Debug interface and a GDB server accompany themselves, which gives the designer/programmer full control and transparency of its actions.

D. JPEG Acceleration

The last step in the laboratory is to accelerate the DCT for a JPEG compression. Here the students develop a strategy of how to communicate with the accelerator, modify the software code and design the actual accelerator.

For this task, the attendees extend the IP pool from Platform Creator. The tool supports two implementation styles. A C-style and a HDL-style. In both cases the functionality of the the IP block is encapsulated from the communication with the other components on the platform. The benefits are obviously. The students can start with the algorithms' partitioning without caring about the HDL implementation of the hardware accelerator. When the system executes successfully, the C model is replaced by a cycle accurate HDL implementation.

Duration	Section	Details
4 Sessions	Tool Handling	QuickStart: First Platform - Assamble a sample system - Instanciate a OCP bus SystemC Explorer - Using the build-in hardware debugging tool SystemC Shell - Commandline tool for SystemC simulation Component Wizzard - Introduction to the library approach - Creation of user-defined components
1 Session	Platform Design	Designing a platform for an ARM9 core - Understanding the design constraints - Composing the initial acceleration platform
3 Sessions	Software Mapping	Programming the Core - Writing test program - In-system debugging with GDB Algorithm Adoption - Introduction to JPEG compression - Source code modification
5 Sessions	JPEG Acceleration	Modification of Hardware and Software - Encapsulating the DCT from the software - Extending the bus system - Designing SystemC acceleration component - Implementing software call-routins Hardware Acceleration - Design hardware block for DCT - Integrate hardware block in the acceleration platform

Figure 3. Laboratory Schedule

IV. Laboratory Schedule

The laboratory is organized in weekly sessions respectively three hours. During each session the students are supervised and have the opportunity to ask questions. But they have also access to the laboratory beyond the guided sessions in order to complete their coding and debugging. At the beginning of each session tasks and goals are defined. This mechanism helps us to keep every group on track and shows the students if they work in time and if they achieve the expected progress.

We organized all sessions in four sections. The topic of these sections are tool handling, platform design, software development and JPEG acceleration. The schedule for each topic is given in figure 3.

The first section covers tool handling. This section tends to be very steered by the supervisor because we try to get our students as fast as possible productive with the new development environment. We figured out that the tool is too complex to let students explore its capabilities themselves. The required time is simply too large. But it is also imported to collect first user experiences. Thus we decided to create small challenges for this first section. They are not directly reusable for the actual accelerator platform design but demonstrate tool specific development techniques and strategies.

In the beginning we ask our students generate a first and very simple platform. It's a timer connected to a reset logic with a testbench unit. They shall understand the working directory structure and the method for design entry. The communication via busses and its memory map is introduced by adding a OCP bus connecting the timer with the testbench unit. Coware provides two tools for simulation and debugging. The SystemC Explorer is a GUI for platform debugging. It provides many visual representation like value traces, TLM port traces and process traces for checking the platform's execution. The build-in SystemC simulator can also be accessed via a GUI but Coware also allows to control the simulation via a SystemC shell (scsh). Our students learn to employ these tools on their simple platform.

Equipped with these skills the independent working effort

increases drastically. They shall composed an minimal platform for an ARM9 core. We provide an ARM specification that contains information about how the outer system has to look like concerning the address mapping and memory organization. In order to get the software properly working this specification needs to be fully adopted.

The software mapping is subdivided into two parts. First, our students are asked to program the ARM core with a pice of self-written C code. This program should be short and simple. It mainly serves as test for the cross compilation and software debugging on the virtual platform. Second, we introduce JPEG compression to compensate potential knowledge gabs in the field of image processing. The detailed understanding of JPEG is essential for the next step. We provide a C implementation of a functional reduced JPEG compression. The source code is meant to run on a normal PC with a terminal and a complex file system. The students need to identify parts in the source code that rely on these aspects and have to find alternatives that are feasible on the virtual platform.

The final section of the laboratory is JPEG acceleration. We chose the DCT for to be released because it is highly parallel and well portioned in the provided source code. Thus our students do not face too many problems with encapsulating the DCT from the remaining compression algorithm. The bus has to be extended for the new component and the SystemC component itself has to be designed and instantiated. For the first version the provided c-code is reused at the acceleration component. For the final version the software code shall be replaced by synthesisable VHDL code. The compression algorithm on the ARM core requires call-routines for read and write access to and from the accelerator in order to get working as intended.

V. Feedback from Students

The prevailing feedback is very positive. The project complexity and freedom to implement their own solution motivates our students. At the beginning we often have to discuss the necessarily of the detailed tool introduction. Our students tend to underestimate the effort of getting productive with an mature development framework. But our first year experience tells us that this time consuming introduction is necessary if our students shall be able to get all the work done during the mandatory time for the laboratory.

From time to time students do not see the necessity to have extra tutorials where basics of SystemC are touched. From our point of view this fundamental knowledge is important for an universal education. Without this manual coding experiences it is hard to estimate work effort on a higher level of abstraction.

VI. Conclusion

With this separation in three different teaching forms we are able to provide a high quality background during our lecture session paired with challenging implementation and evaluation tasks in our tutorials and laboratory at the same time. The attendees get to know implementation techniques for modern ESL design in theory and are asked to develop an own platform in our laboratory. The fundamentals of TLM with SystemC are detached from the complex platform development to ensure a deeper comprehension in both fields.

Acknowledgment

The authors would like to thank Intel Braunschweig who are sponsoring the professorship for our VLSI education. We also would like to thanks partners Coware and Europractice who have provided tools and licenses for this course.

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The Model Railroad Project as an Inspiring Platform for Microelectronics Education

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Abstract—**This paper argues that on the one hand, e-learning tools provide excellent learning options to the students but that on the other hand, e-learning tools might also be the cause of an increasing gap between theoretical knowledge and its practical applicability. This paper reports on the experiences the authors have made with a very old teaching concept, the model railroad. The three main advantages of this project are: (1) teaching can be done on all levels ranging from simple wiring to high-level programming of graphical user interfaces, which all embed the teaching of micro electronics; (2) the subprojects of the model railroad often demand for collaborative work in small teams; and (3) the participating students experience and live soft skills rather than learning about them in a seminar.**

Keywords - problem-based learning, practical learning; complex tasks, model railroad as an example

I. INTRODUCTION

During the last twenty years, teaching has observed some major changes in how it is done: Due to the improvements in hard- and software, e-learning has become omnipresent in almost all disciplines, including engineering of various sorts. Frequently expressed supports for e-learning include: e-learning can be used anywhere and anytime; the link between teachers and learners can be loosened, i.e., they can work asynchronously in time; and certain tools, such as simulation packages, provide the learner with technically difficult insights in new ways [1].

In addition to the actual teaching content, automated quizzes and animated learning material can support the learners during their preparation for the exams. In this e-learning setup, the examination grades increase, even though the direct interaction between teachers and learners might decrease.

Based on the achievements of e-learning, most research activities focus on developing new and/or improving existing e-learning tools. However, in light of all these results, the authors of this paper have also experienced certain problems with e-learning-based education: the gap between *theoretically* learned concepts and *practically* applicable skills are *growing*. In other words, even though the students are able to precisely repeat the acquired knowledge on a *theoretical* level, they have more and more difficulties to apply it to technical (real-world) problems. A possible reason for this case might be the inconsistent use of didactical and pedagogical models for developing e-learning environments [2]. Another cause is the loss of sensuous experiences by using e-learning. The involving of several of senses can increase learning effects [3]. The approach of activity learning argued learning environments in which learners can learn by discovering and experimenting [4].

Knowledge that cannot be applied in practice degrades to a set of meaningless symbols, and is known as *tacit knowledge* in the literature [5]. Its existence in engineering sciences might be quite surprising for many readers, since engineering sciences are on physical entities by their very nature. The authors of this paper have observed that not only the teachers but also the students realize that they have collected a lot of practically non-applicable knowledge. This development has severe consequences for many students: eagerness, motivation, and enthusiasm are progressively substituted by laziness, frustration, and boredom.

To the authors of this paper, *motivation* is *the* key factor for any successful learning attempt. In order to provide more motivation to the students, the authors have started the model railroad project at the Institute of Applied Microelectronics and Computer Engineering. The intention of the model railroad project is to support activity learning by using several senses. The Model Railroad project provides a platform for problem-based learning (a very accepted and in medicine education current learning method, based on authentic and complex tasks) [6], blended learning (a mixed learning method between distance and attendance learning) [7] and discovery learning (a student centered learning method, in which students get the chance to discover and solve problems by their own) [8]. The project's physical setup is described in Section 2.

Many readers might associate a model railroad with playing and having fun. But besides having fun, i.e., motivation, a model railroad can also serve as a platform for serious teaching; the teaching content ranges from low-level wiring to high-level controllers that are based on field-programmable gate arrays. Section 3 provides an overview of the teaching contents that have already been covered within several subprojects.

Several formal and informal evaluations have analyzed how the model railroad project and its various subprojects affect the students' learning behaviors and outcomes, which are summarized in Section 4. It might be interesting to note that in addition to the pure subjects, the model railroad project also supports other skills, such as working in groups, communication skills, planning and organization, and reflecting learning strategies and learning methods as well as the adequate handling of tools. Finally, Section 5 concludes this paper with a brief discussion, which includes a brief description of future subprojects.

II. The Model Railroad Project

The model railroad is intended for the institute's students, which are mainly from the electrical engineering and computer science studies. Therefore, the three major design goals are (technical) functionality, flexibility, and simplicity. Furnishings, such as landscaping, tunnels, bridges, mountains, trees, lakes, cars, etc., which are a main focus of most home-owned model railroads, are less important or not suitable, since they might interfere with the intended technical experiments.

Figure 1. Overview of the model railroad project.

Due to space limitations in the laboratories, the project employs trains and tracks of size N, i.e., a scale of 1:160. The tracks are mounted on a board of 1m x 3m in size. Figure 1 provides a fairly good overview of the model. From the figure, it can also be seen that the model basically consists of two parallel circles, two main railroad stations, several side tracks, as well as an elevated plateau. The very many switches and crossings allow for a large variety of operational alternatives.

In contrast to most privately owned model railroads, the present project has employed a digital control mode of operation by means of the digital command control (DCC) protocol [9]. The digital control has the following advantages: every train can assume its own speed, thus playing is much more fun, and it allows for several exercises with the focus in micro electronics. Furthermore, a digitally controlled model can be connected to a PC, which offers plenty of software exercises.

In addition, the institute currently runs another project, called the model-railroad-in-a-suite-case in which a model railroad is put into a box of about 90cm x 90cm in size. Both projects are very similar with respect to the student work. However, the suite case project also tries to integrate the PC-based control by employing an embedded processor and a touch screen.

Figure 2. The model-railroad-in-a-suite-case.

III. Teaching Subjects

For the technically oriented reader, it should be obvious that the model railroad can be used as a problem-based learning environment [10] and that it offers exercises on all levels ranging from low-level wiring to high-level controllers. The model railroad project involves the following tasks:

- Simple wiring for providing common ground as well as power supply for all the tracks, trains, and controller boards. The latter have to be connected by wires to the actual switches.
- Since the entire model railroad consists of three physical parts, the project also requires some cross bars, which have to be layouted. These cross bars feature not just simple power supplies but also the communication infrastructure.
- Within this project, the students develop their own switch controller boards. Each controller board

consists of a processor, which handles all the communication to the host PC, and some hardware power drivers. Most students resort to ready-to-use Olimex development boards, but some use complex development boards that are based on field-programmable gate arrays (e.g., Altera Stratix II). The former approach involves just microelectronic basics whereas the latter involves the entire design process, including the usage of VHDL, the integration of a Nios II processor, and the attachment of the power drivers.

- The development of the switch controllers also requires the design and implementation of a suitable communication protocol. This encompasses low-level programming for controlling the output pins as well as the integration of a proper protocol stack, such as RS232, USB, and/or Ethernet.

- The entire model railroad is controlled by a host PC. This PC runs a graphical user interface that is to be developed by the students. Besides ``regular'' C++ programming, this task also involves the design of graphical user interfaces as well as the understanding of usability.

In summary, this project allows for teaching on various levels, below and above micro electronics. Thus, the teaching of micro electronics is not isolated but embedded, which requires the design and implementation of further interfaces. This in turn allows the students to understand the functionality of the entire system.

A further conceptual aspect is that teaching in the context of the model railroad does not happen on one of the layers described above. Rather, the teaching is embedded into small subprojects. Three examples are:

- **Wireless Train Control:** Normally, the digital model trains employ a small digital controller, which receives its commands via the rail tracks. This communication is *very* error prone; two student teams developed two different wireless train controllers. Such a wireless controller is based on a ZigBee communication node, a small controller, and the actual motor controller (H-bridge). Also, these two projects require the entire programming.

- **Step Motor Drive:** As an innovation, one student team has developed a new train drive that is based on a step motor. In comparison to a regular DC motor, a step motor allows a train to go infinitely slow. Because of the differences in technology, this subproject also requires the development of a dedicated power drive.

- **Embedded Touch Screen Control:** In a current project, one student team develops an embedded touch screen control system. In addition to all the task describes above, this subproject requires the integration of a touch screen and its programming. Currently, the students favor an architecture that consists of two Nios II soft core processors that are realized into one field-programmable gate array.

IV. Results: Formal and Informal observations

The model railroad project is constantly monitored by formal and informal evaluations. The formal evaluations are done by means of a questionnaire [11]. Briefly summarized, the main results are that the students do like the project, and like the rather informal working atmosphere. Although nearly half of the participated students did not expected motivational effects the project might have been on their learning effects, they experienced a very high motivation. Furthermore the students stated the casual contact to the tutor and they were able to identify their own interest by participating in the project. The results of formal questionnaire also show that they were able to fuse theoretical knowledge and practical experiences.

Figure 3. Brainstorming phase: Students discussed the main task and divided it into their subtasks.

The results of informal observation show that the students developed certain soft skills that are highly relevant in engineering jobs. For example, since the tasks are often explained in a rather open form, the students have to first specify and partition the work for all the group members. In the projects that have already been done, the students have done this in a very collaborative way. Furthermore, the students have maintained this collaborative attitude during the duration of the entire subprojects. A second interesting observation is as follows: Since the tasks are not presented in a complete, and instructional step-by-step way, the students have, as can be seen in Figure 3, to develop a plan how to accomplish the given goal. In so doing, they developed rather general problem solving strategies. Even after this project, they are able to handle and solve complex tasks. In contrast to soft skill seminars, the students not just talk about soft skills, they live them during the project.

V. Conclusion

This paper has presented the model railroad project as it is been done at the University of Rostock. Currently, the intermediate goal of the current activities is to develop a

running system. The authors have observed that due to the nature of this project, the students acquire knowledge on various levels. It might be important to note that the learning tasks are not on separate items but that they are embedded into a broader context, which has major effects on the undergoing learning processes.

In addition to the technical contents, the students also develop several soft skills in an hands-on manner. These soft skills particularly include the collaborative organization of a chosen subproject, and the way, they mutually provide help to each other.

Future research will be going into two different ways. First of all, the project leaders will select subtasks for regular classes, once a first running system is completed. Second, the project will integrate even more educational support. The goal will be to get a better understanding of the underlying learning processes. Once this has been achieved, the second goal will be the development of improved tasks that will be leading to a better education.

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Multimedia in Optoelectronics and Sensorics

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Abstract— **This paper deals with various multimedia elements in microelectronics education and their use in Virtual tour presentations. Virtual tours of laboratories of Department of Microelectronics are assigned for general public, but most of all for potential students of Bachelor Study Programme Electronics and Master Degree Programme Microelectronics. Author's experience in creation of Virtual tour of Optoelectronics and Sensorics is described. It shows the important role of students' team work in process of making a web presentation better. Different types of present-day multimedia implementations as the main presentation elements help to make any scientific branch more popular and more accessible for a variety of visitors.**

Keywords-multimedia; microelectronics education; team work; Virtual tour; Optoelectronics; Sensorics;

I. INTRODUCTION

Optoelectronics and Sensorics are two of the fastest developing branches in Microelectronics. Thanks to the technological progress, optoelectronic and sensoric materials and devices are mass produced and widely used in everyday life. Precise production and progressive technologies allow to produce more efficient, reliable, and relatively cheap products.

The range of optoelectronic and sensoric products comprises LED lightening (from car industry, interior lightening to advertisement, in torches); laser equipment (e.g. in optical drive units); photovoltaic devices (e.g. high efficient thin layer solar cells); various devices for modern optical communication systems (fiber optical repeaters, new generation of optical fibers); chemical sensors (e.g. atmospheric monitoring, detection of explosives); touch sensors ("touch screen" displays, keyboards…); LVDT sensors (in tool inspection and gauging equipment), and many others.

In spite of the increasing importance of Optoelectronics and Sensorics in new technologies, there is a lack of students interested in studying these disciplines at Dept. of Microelectronics on Faculty of Electrical engineering and Information technology at Slovak University of Technology in Bratislava. Therefore there is need for helping students to get basic information about Optoelectronics and Sensorics and motivating them for study and experimental work in these progressive branches.

One of the ways to accomplish these goals is by presenting research and pedagogical work in laboratories of Optoelectronics and Sensorics via internet presentation. These presentations were realized as a virtual tour by two separate students' team projects. The virtual tours are available for all Internet community and they provide basic information for laicuses; more interested visitors can also find here details of the present research in the laboratories.

A. Team projects on Department of Microelectronics

Since 2005 team projects are a part of education at our department. Nowadays, students are encouraged to work collaboratively on academic projects and in various competitions. These projects aid students in developing their essential skills, which they will need when they enter the working environment.

B. Multimedia in the role of design attraction item

A variety of multimedia elements are used within these virtual tours. Multimedia represent the convergence of text, pictures, video, and sound into a single form. The term is used in contrast to media which only use traditional forms of printed or hand-produced material. The power of multimedia and the Internet is in the way how information is linked. In education, multimedia is used for creating electronic educational materials, such as computer-based courses or web presentations that let the user go through series of videos, text, and illustrations describing the particular topic.

II. MULTIMEDIA

For realization of a multimedia project that would popularise Optoelectronics and Sensorics a platform was needed to be analysed as a first step.

The instruction of the project was to choose a website as a form of virtual tour presentation. Virtual tour (Virtual reality tour) is a virtual reality simulation of an existing place or a location. Usually it consists of 2D panoramic photos, series of audio or video footage, real object models, and many other multimedia elements (audio effects, music, text). In comparison with the real tourism, Virtual tour is usually reachable on your personal computer via Internet. People interested in particular places do not need to travel long distances, but they can "walk around" and get real feeling about the desired unknown locality [1]. Virtual tour is one of the best forms of uniting variety of multimedia elements and combining them in a way to catch visitor's eye and attract his attention to the presented content.

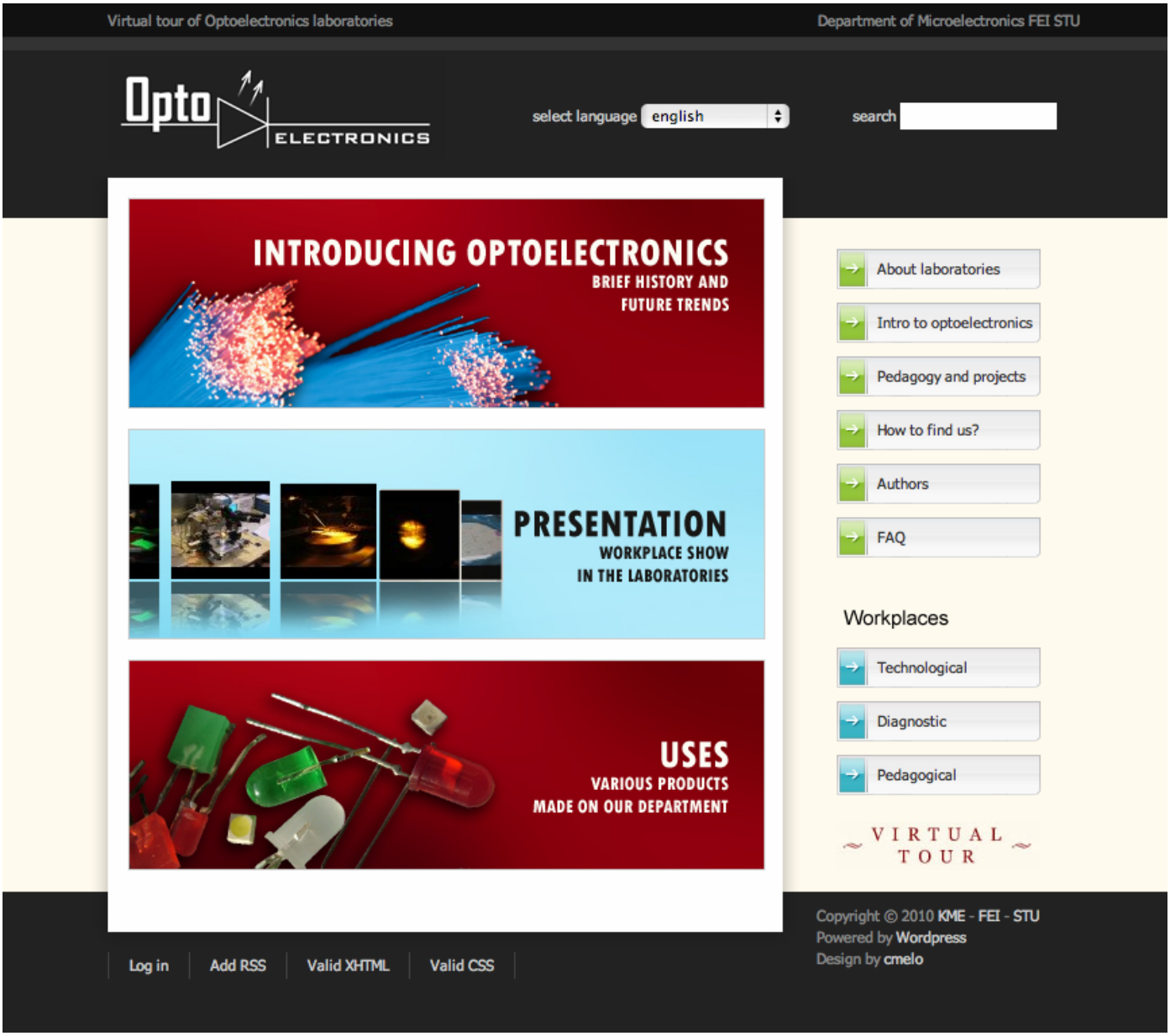

Figure 1. Homepage of Virtual tour of Optoelectronics laboratories

Presentations "Virtual tour in the Optoelectronics laboratories" (Fig. 1) and "Virtual tour in the Sensorics laboratories" are supplemented with video clips, an interactive flash presentation, photos, a glossary, and also with a short overview on historical, present, and future trends in optoelectronics, microwave engineering, and sensorics. It is designed in both Slovak and English language.

Taking into an account the demands of these virtual tours and maintaining graphical, administrative, and editing unity for all Virtual tours of Department of Microelectronics [2], the content management system WordPress was used [3]. WordPress is an open source blog publishing application powered by PHP and MySQL which can also be used for content management. It implements hundreds of various features and allows additional plug-in implementation. WordPress is the most popular blog software used nowadays. Most important features of WordPress in our project are open source licensed, including simple implementation and modification, user-friendly administration interface and free updates. Two sections of Department of Microelectronics already had their Virtual tours designed in CMS WordPress. This fact was one of the crucial in choosing the same system.

In the web presentations, the following multimedia elements were used: interactive flash photo gallery, video clips, dozens of photos, text, and interactive flash map. Each of them is used to deliver certain information to users in form of a multimedia element [4].

A. *Interactive flash presentation and map*

Adobe flash software is a powerful environment for web developers with many useful tools. It offers many advantages but most of all are interactivity and modern graphic design production. Its popularity and usefulness is based on the ability to comprise all media forms together: text, graphics, audio, video footage and computer animation. That's why it can be used for various applications.

We used the flash technology for the photo gallery and the map showing the location of the laboratories in created Virtual tours. A classic photo gallery shows a group of photos which describes some events and places. Interactive flash photo gallery shows photos, their descriptions; it makes nice and fancy transitions between the photos; easy-to-use environment. All this is coated in a modern look animation. The software used for creating this kind of flash photo gallery was Flash Slideshow Maker [5]. It's a free licensed software with a simple interface. It offers powerful features that allow faster generation of flash applications, although with less options than the original Adobe Flash application package.

Students usually search sections that provide as much information as possible in the shortest time. That's why the virtual tour students' production team decided to create a flash [6] based photo gallery. Photos from all laboratories were ment to help students to get an idea what is done in the laboratories (Fig. 2 and Fig.3).

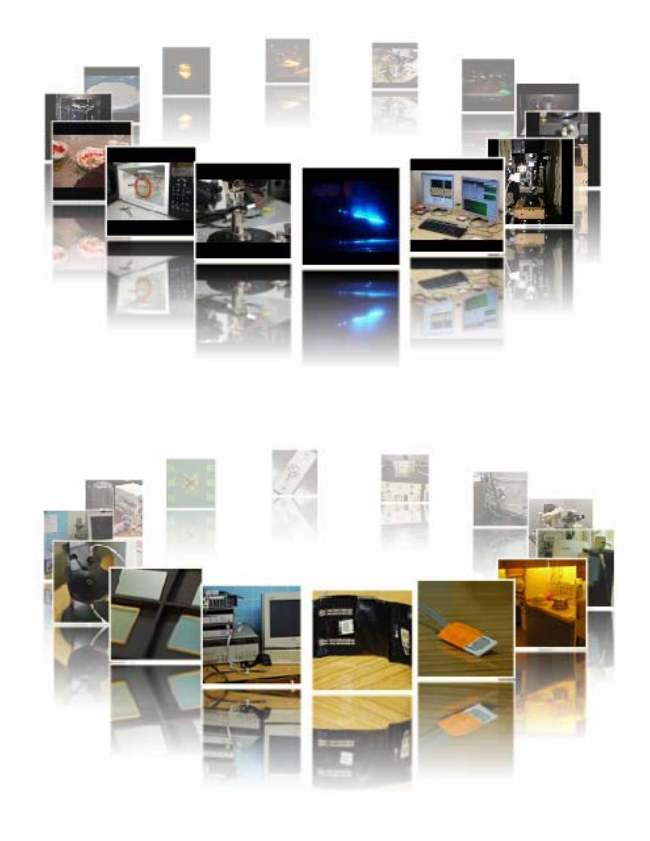

Figure 2. Interactive flash presentation in Virtual tours

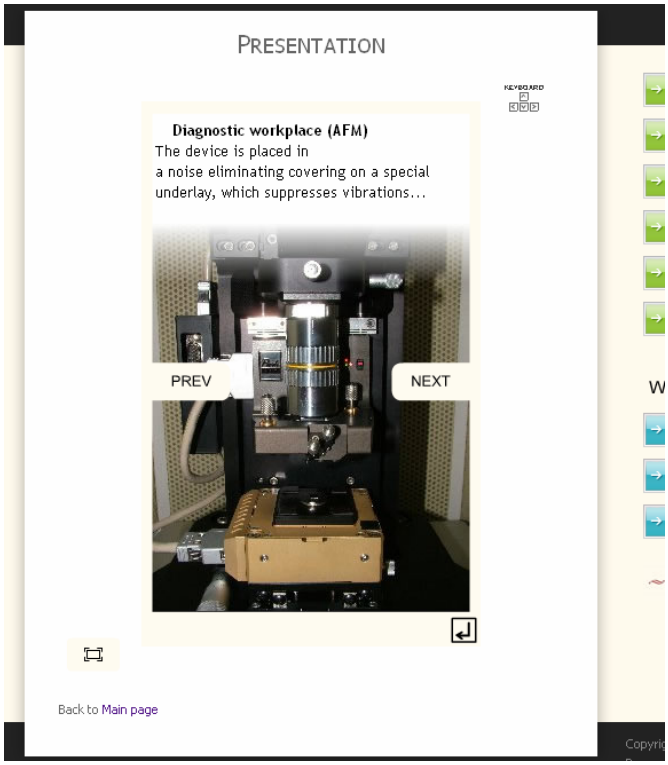

Figure 3. Photo of diagnostic workplace (AFM) in interactive flash presentation in Virtual tours of Optoelectronics laboratories

The location map of the department section is designed in flash, too. It loops zoom-in animation of the map that can be stopped/resumed, zoomed-in/zoomed-out, and observed by user. The map helps students to easily find the location.

B. *Static pictures and text*

Nowadays, a text is usually supplemented with pictures. It does not require any special skills. On the other hand, it is important to use pictures which clearly describe what is written in the text. Introduction article shortly describing the history of the Optoelectronics or Sensorics, present and future trends was created for virtual tours. All articles are supplemented with pictures, charts, and also hyperlinks, so that students interested in certain subject can find out more on other external sources.

New logos for Optoelectonics laboratories and Sensorics laboratories were designed (Fig. 4) as part of intro process of creating of virtual tours. Basic principles for logo creation were followed: simplicity, graphical unity, and easy to use in other applications (MS Word documents etc.). Logos for both virtual tours were designed in two variations (black and white) so they can be used on various backgrounds.

C. *Video clips*

A great part of both Virtual tour of Optoelectronics laboratories and Sensorics laboratories is concentrated on video documents. In cooperation with pedagogues and researchers in chosen laboratories, the students' team selected few measurements methods and production processes.

Figure 4. Logos for Virtual tour of Optoelectronics in English, Virtual tour of Sensorics in Slovak and Virtual tour of Sensorics in English

These processes were captured by camera and afterwards edited and cut in Sony Vegas Pro [7] video software. Final video footages were exported for web video flash player.

The videos demonstrate technological process of manufacturing organic electroluminescent diodes, measurement of S parameters (Fig. 5), AFM measurement, manufacturing process of thin layers on the substrate and their applications (Fig. 6), photolithography processes, and many others.

Video clips are addressed to laity, so that they can understand what optoelectronics or sensorics is in practice. Short video footage is supplemented with an audio commentary and a short article below the video.

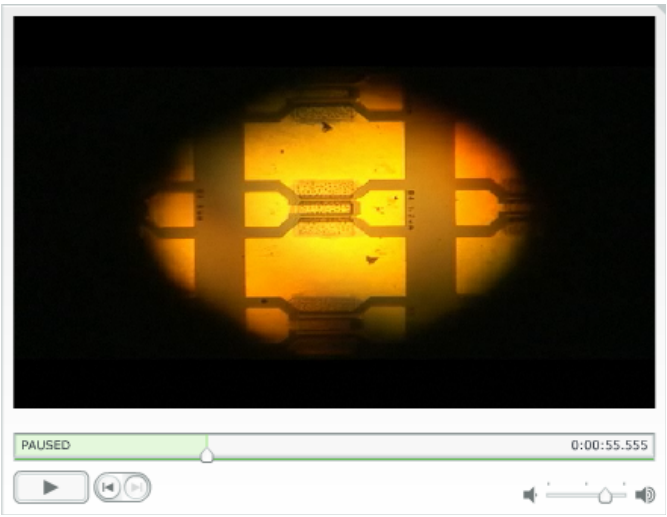

Figure 5. Video clip about measurement of S parameters

Figure 6. Video clip about thin layers preparation

III. TEAM WORK

In modern educational curriculum students are encouraged to work collaboratively on academic projects and in various competitions. Projects presented in this article aid students in developing the essential skills they will need when they enter the world of working. A team project encourages members of the team to work interdependently towards the same goal. It also leads to responsibility because every member in the group feels a sense of ownership of their role.

Behind all the students' team work there is an environment of an online course application, created on educational portal "eLearn central" and based on course management system Moodle [8]. This platform enables all team members to manage the course content, chat with each other, collaborate on the same document, and upload files. Each team member can work on his tasks whenever it is suitable for him, he can also react on posts or queries sent by other team members. Students are forced to cooperate with each other in a way to accomplish the goal of the team project. Students can use and present their skills by working on partial tasks which are from their field of interest. They are also forced to learn new information and skills on self-educational basis. The most important is that students can get a valuable experience in team work, cooperation, and advocacy of their own statements in front of other team members. From the students' point of view, team work gives them much more space for organizing their time and the way they will accomplish goals of the project. The driving force of the project was independence, new way of working together, and opportunity of teams' competition at the end of the semester.

However, very important fact is a structure of the team. Members need to be interested in the project they are going to collaborate on. The experience in organizing students' team projects on the Department of Microelectronics on Faculty of electrical engineering and information technology shows that the best way is to let students themselves choose project they will participate in. Thereby students' active approach in team project is most probable. Students' interest, activity, and motivation are very important for reaching the project goals. If properly motivated, members of the students' team project

stimulate each other in common team work. So we can see that the significant step is the proper selection of team members with complementary knowledge and abilities. In case the mentioned condition is fulfilled, the result of the students' team project can be very interesting and with a high quality.

Of course, involvement of pedagogic supervisors of team projects is obvious. Nevertheless their role in the students' team project should be to regulate and convect, not to govern and dictate the work flow of the students' team. Otherwise the main goal in the students' team project is missed and also students lose a motivation for an autonomous team work.

IV. FEEDBACK

One of the primary ideas of Virtual tours of Department of Microelectronics was to address visitors and attract them by the content of these Virtual tours. A quality feedback can show us whether we succeeded or not. In web site industry, feedback and statistics are very important. By analysing various statistic indexes and their changes it is possible to improve the content of the web site. For example by improving local hyper linking system of the web site, pages with low visit rate can be more visualized. On the other hand pages that lack visitors can be supplemented or replaced by multimedia elements, which describes the topic in a modern and fancier way.

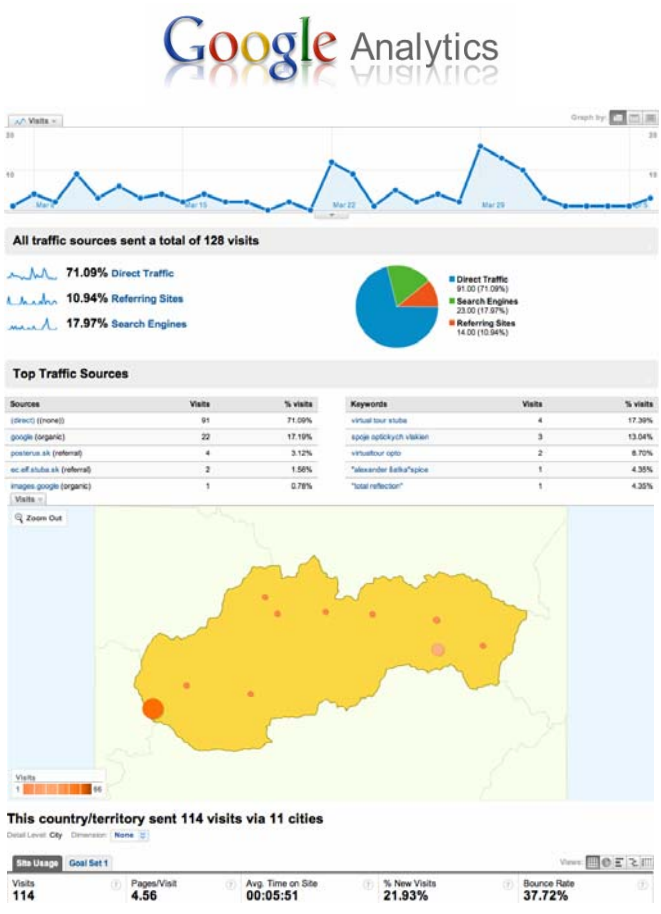

Figure 7. Logo and previews on Google Analytics statistic tool interface

Statistic tools are important in websites because they provide unprejudiced and relevant data about the website.

Both Virtual tour of Optoelectronics laboratories and Virtual tour of Sensorics laboratories use feedback system for statistic reports. Free online tool called Google Analytics (Fig. 7) is used. It provides a plenty of useful features such as visitors' localization statistics, pages' visit rate, most frequently used search engine keywords. It is a statistic tool used by professionals [9].

Virtual tour project of the whole Department of Microelectronics is still under development, although parts of it are available on the Internet. Further spreading of the project is planned and therefore more students' feedback is expected to be received. Forasmuch as these virtual tours are mainly dedicated to students, their feedback is the one that matters the most.

V. CONCLUSION

Virtual tour of Optoelectronics laboratories and Virtual tour of Sensorics laboratories were created to encourage students' interest in microelectronic education.

Very important and interesting fact is that these presentations were results of two separate students' team projects. They were created by students for students, which means that students created educational materials for themselves and their colleagues according to their own needs. Still they were supervised by experienced pedagogues and researchers.

Both students' teams worked collaboratively while gathering available information, sorting, and structuring them, creating video clips, articles, and other multimedia elements. The aim was to create an interesting presentation with useful information presented by modern multimedia elements. All virtual tours of the department of Microelectronics are accessible on http://kme.elf.stuba.sk/virtualtour/. Considering the fact that students are those who submit ideas and solutions, the virtual tour presentations are full of fresh and modern concepts and multimedia elements.

Virtual tours were created but now the public needs to be informed about existence of these free online educational materials. To address the potential students, presentations of the Virtual tours are organized for the students of secondary schools. In such a way or by other means of propagation they are informed about possibilities of their further education and importance of application in practice.

ACKNOWLEDGMENT

Authors' acknowledgment goes to all who participated on the projects of Virtual tour in Optoelectronics laboratories and Virtual tour in Sensorics laboratories. Most of all the thanks go to the members of our two teams and to mentors which have guided us throughout the projects [10]. This work was performed under the Center of Excellence CENAMOST (VVCE-0049-07) project and supported by the Slovak Scientific Grant Agency VEGA 1/0507/09, VEGA 0742/08, and by the project KEGA 3/7248/09.

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Microelectronic Education by Doing

The MPC-Group of Baden Württemberg

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In 1989, the Multi Project Chip Group (MPC) was founded by 13 Engineering Schools, now Universities of Applied Sciences of Baden Württemberg, which have electronics design in their curriculum. Emphasis of the MPC organization was to provide the Universities with software, computer equipment for microelectronic design and a path to real silicon prototypes. In the beginning there were own contracts to companies as there have been Telefunken and the IMS Stuttgart and first silicon chips were developed by students. Later the European project of EUROCHIP and the successor Europractice managed this path to prototyping, but cooperation of the UAS were established and concentrated on information exchange, software acquisition and know how in ASIC design. The MPC group, which is still active and organizes an own workshop two times a year (now we will have the 43rd WS in February 2010) developed more than 80 silicon chips, most of them designed by students, fabricated and tested since then. The range of these designs cover all actual topics of microelectronic design including processor cores, SOC designs, high level system designs, telecommunication chips, analog- and mixed signal chips, full custom design of small cores and other applications.

The presentation will give an overlook over the concept of the MPC group, their activities and achieved results in education. Typical project chips will be presented and the impact of industrial cooperation demonstrated.

I. INTRODUCTION

Electronic design today is more or less assembly of industrial designed integrated circuits on printed circuit boards. Successful design requires careful reading and understanding of complex data sheets, interfacing between different standards and adaption of programmable devices to protocol requirements. There is few circuit design left, may be a small space in high quality analog electronics with high performance requirements or with special power or environmental requirements. Assembling predefined ICs is not a very satisfying job for a creative electronic engineer, there is no real area for own concepts and improvements. Even for industry using existing chips is not enough because everybody can do it and there is no differentiation in product, performance or behavior, may be only in some software running on the system.

Real new things require the ability to design own ICs, which allow to have the required originality in performance, advantages in price, size or power consumption, which the competing company does not have, with other words: ASICs (Application Specific Integrated Circuits) are a must to differentiate and to stay in a fast moving high competitive market. It's about the same as if a car manufacturer uses only DIN-Parts to assemble a roadster. He will never sell it!
ASICs can be designed in house or under contract by a design house. Who has the knowledge and experience, what is possible with ASIC design and where are the technological and financial limits? Modern electronic education has to answer these questions during a course in modern electronics in every engineering school or university.

II. GOALS OF MICROELECTRONIC EDUCATION

A. Modern electronics teaching

Electronics is one of the fastest changing subjects in all engineering professions. To keep track teachers have to do own work in this field, by the best they should actively work in industrial design projects or work closely together with design houses. Link to industry is a must, but there are complex fields that have to be covered today:

- Analog Design on transistor level
- Digital Design on System and HDL-Level,
- Digital design on CPLD, FPGA and ASIC
- Cell based ASIC design
- Hardware/Software-co-design
- Busses and Network interfacing
- Embedded Processors, IPs, memory

There are more subjects of importance; complexity is even faster growing than the doubling of transistor numbers every two years, called the famous rule of Gordon Moore.
Classical analog circuit design is one course, same for fundamental logics, processor architectures, VHDL as a design language, may be with already first training on FPGA devices.
But teaching microelectronics must be much more. You can not be a gardener without putting your hand into the soil. So there must be a direct contact to silicon also for students, CAE

and EDA is nice and important, but without the feedback from real things build up it stays theory. You cannot teach swimming without water!

B. Learning by doing, founding the MPC-Group

Since Mead and Convey [1] in the 80th we have the concept of educational test designs on silicon, teaching students by defining a project, one student or a team of students, designing their own chip in an actual technology.
In USA the MOSIS was started in 1981, a manufacturing site, later more a broker site, to give low cost or even no cost access to silicon for universities.
In Europe, with the European Program of EUROCHIP, started in 1988, a similar approach was made. Main difference to MOSIS was that there were no own manufacturing intended; instead standard processes are offered from IC Fabs in a multi-project wafer fashion. This program is still ongoing now with Europractice, which offers several international available production processes from UMC to AMS, from AMI to very special RF-Processes, covering the actual technology scenery with a standardized administration process and reduced and affordable prices for university designs.
I have to mention the competing broker site of CMP, run by TIMA, Grenoble, also available for European universities with alternative processes down to 60 nm and below, founded at about the same time as Eurochip. CMP is now main supplier of French and non European universities, even customer from USA are common.
In this scenery, the 13 German Engineering Schools (Fachhochschulen) of Baden-Württemberg which educate in electronics formed an own organization in 1986, called the

MPC – Group

MPC stands for **M**ulti **P**roject **C**hip, Fig. 1. Our idea has been similar to the later Eurochip/Europractice-Program, but in a much smaller scale. The name was taken from the original Mead Conway MIT courses and ideas under the same acronym. We made contracts to German fabs at that time like TELEFUNKEN, AEG and other (they are all gone, why?), working in close cooperation with the Institute of Microelectronics (IMS) in Stuttgart, which was founded about the same time.
Main interest of the MPC group is until today:

- Education in Microelectronics and IC Design
- Paving away to Silicon, real ICs, real problems
- Way to actual processes and device libraries
- Working and teaching on industrial CAE Equipment
- Using actual high level Tools
- Keeping and developing technical knowledge and intercommunicating this in the group by organizing and conducting courses on IC design.
- Mutual assistance and help in running soft- and hardware
- Workshops in regular intervals, two times a year to give a forum for students for presentations.
- Proceedings of the workshop as a publication journal with official ISN registration and peer reviewed papers.

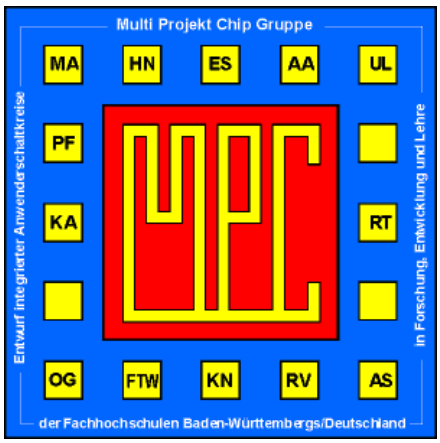

Fig.1: Logo of the MPC-Group of Universities of Applied Sciences, Baden-Württemberg founded in 1986.

III. Design Software and Computer Equipment

A. Design Software

From the beginning it was decided to use industrial grade software for IC design, although there were several no cost university programs available. At that time many teaching institutions worked on their own equipment, some even in their own technology kitchen. Because of the small time available to train the students in microelectronic subjects, it was decided, to go “fab-less”, to use the same programs which industry use, and to use the same fabs for manufacturing, which are used by industry.
This was very challenging! Not for technology, but for the amount of equipment and money which has to be acquired. The coming up of “university-programs” by companies who are interested that students are trained in their software helped a lot. A common DFG-Application with significant volume in money allowed the group in 1990, to acquire a first set of Apollo-Workstations for each school and related software Licenses from MENTOR-Graphics. This software covered

- Analog simulation with SPICE,
- Analog and full custom IC-Design with the IC-Station
- Digital design with Simulation, later also with a VHDL Compiler and Synthesis.

Further Software allowed plotting the designs, DRC and LVS and all what is needed to make a real chip.
In later years many MPC members are still going with MENTOR in education, even when there some Cadence – and Synopsys Tools are available and used.
Since Europractice started in 1996, all MPC – members are also members of europractice and most of them are using the tools which are provided from there. I have to mention that we use still about the same set of software, acquired with MPC resources and contracts. Now the europractice portfolio is

The Author is elected speaker of the MPC Group since 1998

much larger, complete and actual, which make it easier to keep actual and updated. On the other site, nearly 50% of the available resources are spent for membership fees and license costs, but it is worth while having the access to big packages of tools.

B. Computer Equipment

The decision to use commercial design software required from the beginning high level (UNIX) hardware and computer equipment, mainly so called workstations, which were very expensive at that early time (before the PC arrived). The MPC Group managed to be equipped with three generations of Hardware, starting with about 3 … 5 graphical workstations of Apollo Type per School. Later we got HP-Workstations with up to 8 places, 5 years ago the last hardware update with a modern concept of SUN-Ray graphical sites, organized around a central SUN-Server-Cluster with network based connection and more than 24 places connected. These acquisitions were possible by three DFG- reviewed projects, the last one 5 years ago with a volume of about 1.3 Million € for all the 13 now called Universities of Applied Sciences.

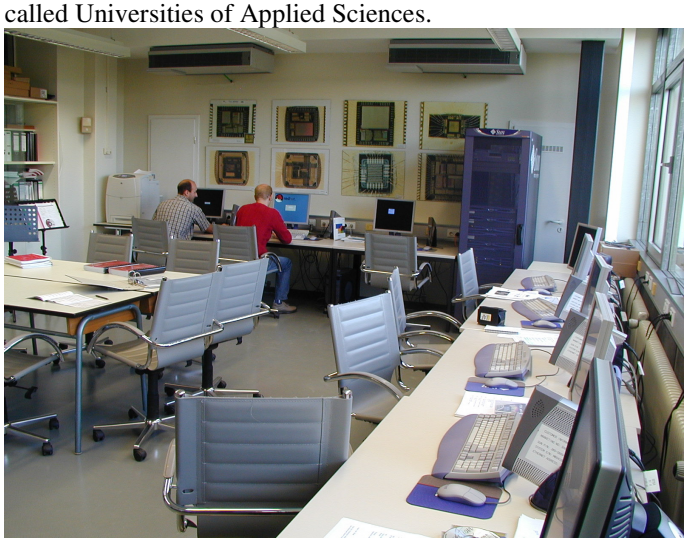

Fig 2: SUN Cluster with SUN-Ray – Terminals (Offenburg)

In addition, several high performance PCs were added and connected to the central cluster, because more and more of the commercial software is running now better on a PC than on a UNIX-Solaris system, especially the FPGA design software, often used in the training of students. So the tendency is to expand the X86 server side, which will be done soon, without scrapping the Solaris which is still good for special programs, not yet available on PC. May be there will be some way to virtualization.

Running these complex clusters, all members have grown to experts in UNIX and CAE/EDA administration. This has been a severe bottle neck in the past, because these software tools were extreme complex and required a lot of administration.

IV. COOPERATION WITH INDUSTRY

Although all members signed license agreements which reserved the use of the software for educational use, several industry projects as well as research work have been performed in the group. Fig 3 shows a map of Baden-Württemberg with the member- Universities well distributed over the region, being a natural addressee for IC related issues.

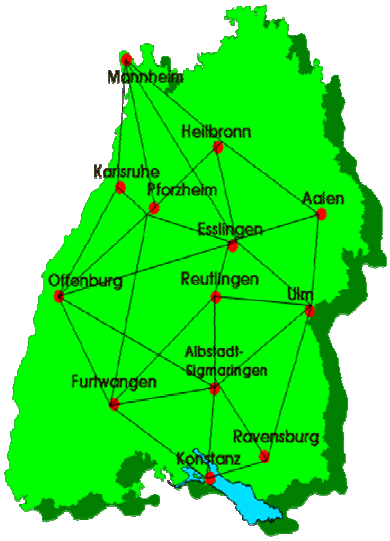

Fig 3: Map of Baden-Württemberg with MPC sites.

There is even more: depending on the personal history of the member and interest, there has been a specialization on certain subjects. So there are sites with emphasis on digital design, other sites are more full custom design or system design related. We have experts on nearly all important subjects in our MPC Group, if we our self are not able to respond, we have many connections to Universities, Fraunhofer Institutes or even international sites, where we are known and where we can ask. So every MPC site can offer the whole spectrum as a local representative. See our website

www.mpc.belwue.de

These industrial contacts are very important for teaching and the actuality of our microelectronic courses, many students found jobs in the corresponding companies, after being engaged in cooperation projects or performing Master/Bachelor thesis in these companies.

V. PROJECTS AND RESULTS

There are more than 100 Chip designs done in the MPC group since 1989, starting with analog arrays on a Telefunken Master up to now high performance CMOS ICs with processors on in a 0.18 UMC Technology.

In 2000, the educational knowledge of the group was condensed in the 744 pages book:

"Electronic Design Automation Handbook"[3]

by the author of this paper with contribution of 16 authors, mostly from the MPC group and associated partners and a foreword by Professor Gajski, UCI. The book, first edition in German language [3], was translated to English 2005 and is available until now from Springer [4]. A Chinese edition was added in 2005 and is successful sold by Publishing House of the Electronics Industry, Peking as a paperback version [5]. The book is still used in the microelectronic courses and allows an easy insight into basics of modern microelectronics, even when there are many new developments since than done.

The MPC group will have its

43. Workshop on Microelectronics

on 9th of July this year in UAS Reutlingen, with a non interrupted rhythm of twice workshops a year, from the beginning. There are no similar networks active and successful over more than 20 years as far as I know in this field.
On the 40th workshop 2008 in Constance there was a "Best Paper Edition" of papers from our proceedings journal, taken from the past 20 years [2].
Nearly every year the group organizes special courses on IC design, so "Net to Chip" in 2002 and 2006, "Analog Design with Cadence" in 2009 and this year again a SystemC-Course. These courses were taken from educational material, produced by the members and distributed in the group, as well as there are course scripts distributed, text books written by members and so on.
But the main thing is silicon, not only talking on chip design, but doing it. Here are some examples from ICs, made by students in Labs of the MPC group.

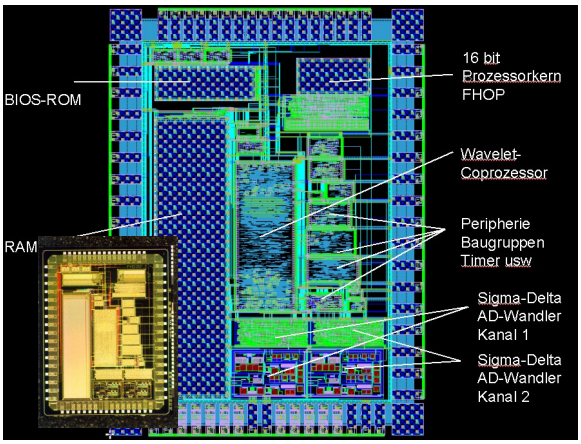

Fig. 4: DSWPC-Chip for 24 hr ECG recorder with 2 channel sigma-delta converter, 16 bit processor, wavelet coprocessor, FIR signal processing and data compression, in ES 2, 0..5µm CMOS Technology. Chip photo in the corner. The chip has a dimension of 4.9x 6.6 mm^2, designed by Wolfgang Vollmer, UAS Offenburg, 1998.

The *DSWPC Chip* was designed in 1998 for a one-chip 24 hr ECG recorder, which was later produced in series and sold with CE from 2002 on (it is still on the market). The chip contains a 16 bit processor core, already developed in Offenburg in the 90th , related RAM and ROM structures, a wavelet unit with 3 FIR Filter for data compression and the related A/D converter using the sigma/delta concept. The chip is able to process the 2..3 mV heart electrode signals directly, compress the data and store it on SD-Card or send it via a small bandwidth telephone link. The chip was used in several other medical and industrial applications and is still used in these systems.
Fig. 5 shows a 0.35 AMI CMOS design for the project ePille®, containing a 32 bit processor, PLL, temperature cell, special medical telemetry blocks and further periphery blocks forming a complete system on chip (SOC)[4-8]. The soft processor SIRIUS, developed in Offenburg in 2005 and used in several applications, is a 1 instruction per clock cycle low power design with about 120µW/MHz and an area in silicon below 1 mm^2 in 0.35 Technology. The chip photo is shown in the corner.

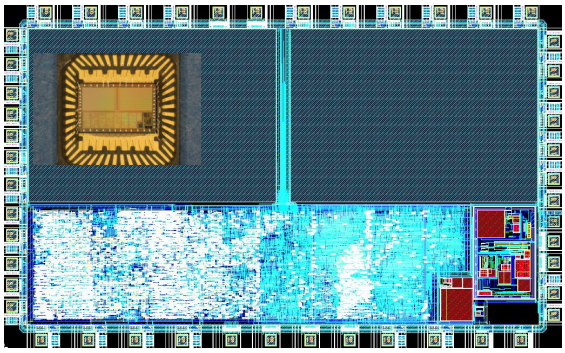

Fig. 5: Design and chip photo of the ePille® -processsor chip for a medical application. AMI 0.35 A/D Tchnology, contains a 32 bit processor, peripherie, temperature cell, PLL, wake-up and power down electronics (design NidalFawaz, Daniel Bau, UAS Offenburg 2008)

The last example is a 0.18µm Design in UMC technology, showing a 32 bit processor and related periphery for a student-PDA called studPod, with interface for external memory, an OLED display and an USB interface. This design, made in 2009 by Daniel Bau, is only 1.6 by 3.4 mm2 in size and represents a more than 4 times higher integration in comparison to the above chips. All these designs were published on international conferences and papers and are part of cooperating dissertation thesis [9].

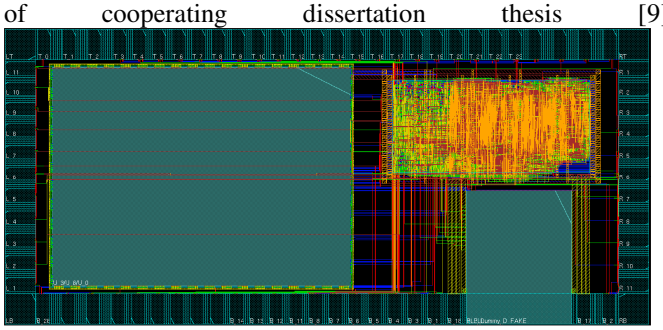

Fig. 6: 32 bit processor SIRIUS and periphery for a PDA in a 0.18 µm 6M1P A/D-CMOS technology. Chipsize is 1.6 x 3.4 mm^2. Designed by Daniel Bau, 2009, Offenburg.

There are of course many other designs from other UAS of the group, which emphasis on analog, RF-Frontend, signal processing or whatsoever. Many publications are made; some of them research papers in conjunction with PHD processes.

VI. CONCLUSION

Microelectronics education has a 22 year history and experience in the Universities of Applied Sciences of Baden-Württemberg, organized in the MPC-Group. With an average of 150 students a year, more than 3300 Students were educated and trained on IC design, with more than 80 ICs designed in student projects (52 since europractice, see annual report 2009). Complexity of actual designs covers all flavors from RF to high level SOC chips in a research adequate level. Success was gained from available full commercial tools and a paved way to silicon, using Eurochip, later Europractice as a broker. In all 13 Universities, basic IC design is part of the curriculum. All concepts are fab-less, IC-technology development is not in the focus and is not regarded as a subject of training.

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FPGA implementation of a real time multi-resolution edge detection video filter

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***Abstract*—This paper presents digital video filters labs for final year engineering students. The project deals with the implementation of Canny Deriche optimal edge detectors on a FPGA plateform. The target of these labs is to illustrate the design of integrated electronic systems and to introduce the concept of architecture/algorithm adequacy.**

***Index Terms*—Engineering student labs, embedded filters, edge detectors, real-time video processing, FPGA, SoC**

I. Introduction

This paper presents an advanced digital design project using FPGA for final year engineering students. The aim of this project is to study and to implement a real time edge detection video filter on a DE2 Altera Cyclone II Development Board [1]. This kind of project presents several pedagogic interests. Firstly, it is an opportunity for students to put into practice signal and image processing theory on a concrete example. Secondly, as shown in this paper, the relative complexity of this design project leads students to explore different architectures to choose the one which presents the better performance/complexity tradeoff. In the same line, students have to propose an efficient validation methodology suited to the project complexity. Finally, this design project covers the entire FPGA design flow, i.e. from the HDL specification to the hardware implementation.

This paper is outlined as follows : the second section presents the required background theory on the edge detection filters. Then, the hardware implementation upon which the project is based is described in the third section. The fourth section presents the design environment, and especially, the DE2 Altera Cyclone II Development board [1]. The fifth section presents an illustrative example based on the lab results, and, finally, the pedagogic interests of such design project are discussed in the sixth section.

II. Theoretical background

The principle of an edge detection filter is to locate the sharp changes in the image brightness. Two methods are commonly used: the *Laplacian*-based ones and the *Gradient*-based ones [2]. The second ones, that interest us in this paper, consist in computing the gradient magnitude and direction in order to detect local maxima of the magnitude in the direction of the gradient. These maxima correspond to the image edges. Usually, a smoothing stage is applied before the actual edge detection stage to enhance the detection quality (noise reduction). The figure 1 shows the generic architecture of such kind of edge detectors.

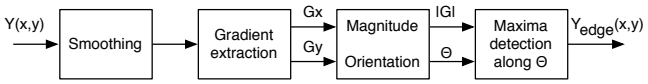


Fig. 1. Generic architecture of a Gradient-based edge detector

A. Deriche edge detection filters

Canny [3] defines three criteria of optimal edge filters: *good detection*, i.e. a low probability of failing to detect a real edge point and a low probability of falsely marking non-edge points, *good localization*, i.e. detected edges close as possible to the real edges, and a *single response* to one edge. By applying these criteria on a noisy step edge model, he demonstrates that an optimal edge detection filter can be implemented by a Gaussian filter to smooth the image followed by its derivative to extract the gradient components Gx and Gy. The size of the Gaussian filter is an important parameter as it defines the resolution/sensitivity tradeoff: smaller filters allow the detection of thin lines, while larger filters are more robust to the noise effect.

Deriche improves Canny's filter in case of digital images. He proposes to substitute the Gaussian filter with recursive filtering structure (Infinite Impulse Response filters) to reduce the computational effort required for smoothing [4], [5]. By doing so, Deriche's filter presents a fixed complexity that does not depend on the smoother coefficient. That allows multi-resolution edge detection processing.

B. Garcia-Lorca implementation

Finally, Garcia-Lorca proposes an efficient implementation of the Deriche's filter suited to FPGA architectures [6], [7]. He demonstrates that the Deriche's filter can be decomposed by four second order IIR filters to smooth the image $Y(x, y)$ (two for the horizontal smoothing and two for the vertical one), followed with two FIR Roberts filters to extract the

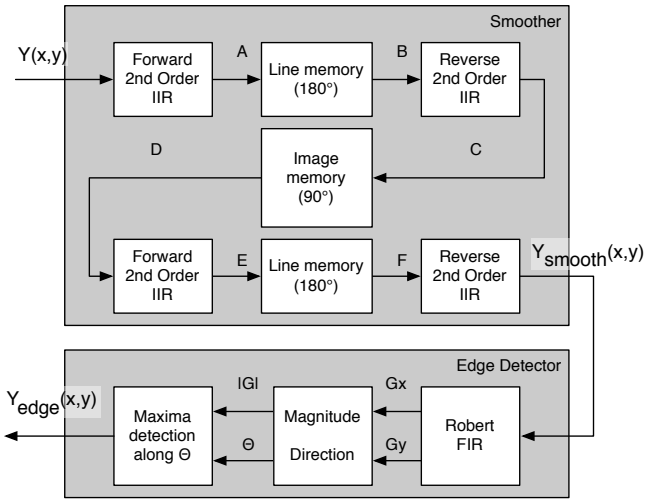


Fig. 2. Architecture of the Garcia-Lorca edge detector

gradient components (Gx and Gy). While the design project proposed in this paper relies on this implementation, we propose to detail it in the next section.

III. Edge detector architecture

The figure 2 shows the Garcia-Lorca edge detector architecture. The smoother stage is composed of four identical IIR filters, of two line memories, and of one image memory. The equation (1) represents the z transfer function of the IIR filters with γ corresponds to the smoother coefficient.

$$S_{GL}(z) = \frac{(1-\gamma)^2}{(1-\gamma z^{-1})^2} \tag{1}$$

After the first IIR filter, a line memory is used to perform the horizontal rotation of the image. The principle is to write the incoming pixels in the memory in one direction (ex. increasing addresses), and to read them in the opposite direction (ex. decreasing addresses). By doing so, the image is rotated of 180°. However, we note that this principle implies that two memory accesses are performed at each pixel cycle (one to read the pixel stored in the memory, and one to write the new incoming pixel). After this horizontal rotation, the same IIR filter can be applied to complete the horizontal smoothing. Then, the image is turned of 90° to carry out the vertical smoothing along exactly the same principle. Again, this new rotation is performed thanks to a special management of the image memory: while a pixels column previously stored is extracted from the memory, the incoming line is stored at the same memory addresses. Once again, this principle implies two memory accesses at each pixel cycle.

Possibly, additional line and image memories can be inserted between the smoother stage and the edge detector stage in order to rectify the image orientation. These optional memories are not represented on the figure 2 but have been implemented in the examples of the section V.

The edge detector stage is divided into three successive blocks. Firstly, two Robert derivative filters are applied on the filtered image $Y_{smooth}(x, y)$ to extract the horizontal and the vertical components of the gradient (eq. (2,3)). Then, the gradient magnitude and gradient direction are computed to enable the magnitude maxima detection in the direction of the gradient. These maxima correspond to the image edges. Possibly, a threshold can be added on the comparator block to mitigate the noise effect and to enhance the detection quality.

$$G_h = \begin{bmatrix} -1 & 1 \\ -1 & 1 \end{bmatrix} \tag{2}$$

$$G_v = \begin{bmatrix} 1 & 1 \\ -1 & -1 \end{bmatrix} \tag{3}$$

IV. Design environnement

A. DE2 development board

We have chosen the Altera DE2 Cyclone II Development board for the design project because it includes, among others devices, a large FPGA circuit, a SRAM suited for 512x512 image memorisation, and video In/Out devices (NTSC decoder and VGA controller) [1]. It includes also a large number of switches which can be used for debugging, and for setting the value of the smoother coefficient and the value of the detection threshold.

B. Video processing environment

Moreover, the DE2 package includes a NTSC video-to-VGA display project (DE2_TV) in which any video filter can be mapped. The figure 3 shows the DE2 video processing architecture. The video decoder block extracts YCrCb 4:2:2 (YUV) video signals from the external NTSC TV decoder. Because the NTSC video signal is interlaced, it is required to perform de-interlacing on the data source. That is done thanks to the SDRAM dual frame buffer and the field selection multiplexer controlled by the VGA controller. Finally, the edge detection filter is inserted between YUV 4:2:2 to YUV 4:4:4 converter block and YUV to RGB converter block as depicted on the figure 3. The edge detection is processed only on the Y video channel.

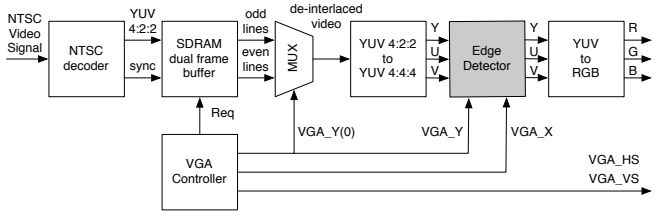
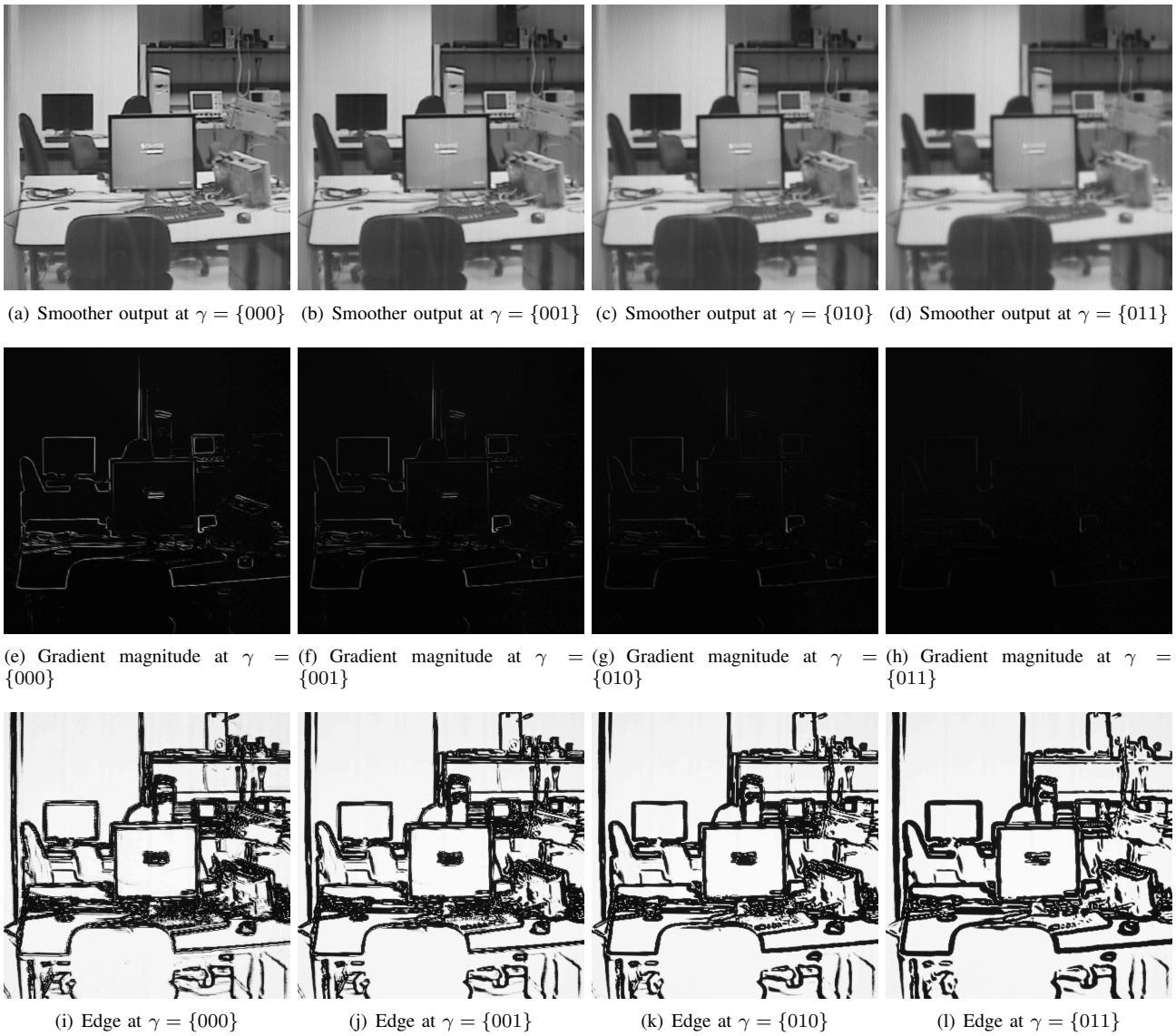


Fig. 3. DE2 video processing architecture



(a) Smoother output at $\gamma = \{000\}$ (b) Smoother output at $\gamma = \{001\}$ (c) Smoother output at $\gamma = \{010\}$ (d) Smoother output at $\gamma = \{011\}$

(e) Gradient magnitude at $\gamma = \{000\}$ (f) Gradient magnitude at $\gamma = \{001\}$ (g) Gradient magnitude at $\gamma = \{010\}$ (h) Gradient magnitude at $\gamma = \{011\}$

(i) Edge at $\gamma = \{000\}$ (j) Edge at $\gamma = \{001\}$ (k) Edge at $\gamma = \{010\}$ (l) Edge at $\gamma = \{011\}$

Fig. 4. Edge detection examples with respect to the smoothing parameter γ

We note that although the Altera DE2 Cyclone II Development board integrates a PAL TV decoder, we choose the NTSC video standard because it simplifies the clock management in the system. Indeed, NTSC systems use a refresh rate of 60 fields per second (one image composed of 2 fields), which corresponds exactly to the refresh rate of a standard VGA display (60Hz). For comparison, PAL system uses a refresh rate of 50 fields per second. The use of PAL standard would infer a resampling factor of $6/5$ which is, obviously, more complex to implement.

The video flux processed by the edge detector is clocked at 27 MHz. Because of the special memory management that requires two accesses (read and write) during one pixel cycle, the user filter and the external SRAM memory are clocked at 54 MHz.

C. EDA tools

The whole project is designed in RTL VHDL code and the functional simulations and validations are performed with *Mentor Graphics ModelSim* software. Then, the *Altera Quartus II* software is used to do the synthesis, and the place-and-route steps. Possibly, post place-and-route simulations are performed in *Modelsim* before real test on the DE2 development board.

A comprehensive example is provided to students to help them in the design. It consists in a very simple motion detector which is implemented at the same location than the edge detector (figure 3). Its principle is to compare the value of the incoming pixels with the value of the pixels of the previous image stored in the image memory so as to detect changes in the scene. Moreover, a set of VHDL test benches are

provided to simulate the operation of the DE2 video processing architecture.

V. Illustrative example

The figure 4 shows illustrative examples obtained during lab sessions on the DE2 development board. The figures 4(a), 4(a), 4(c) and 4(d) show the output of the smoothing filter for different values of the smoothing parameter γ, the images of the computed gradient magnitude are displayed on figures 4(e), 4(f), 4(g) and 4(h) as the final edge images are shown on figure 4(i), 4(j), 4(k) and 4(l). These examples illustrate the effect of the smoother coefficient as described in section II.

The table I provides a summary of the main hardware resources used by the edge detector filter and by the whole DE2 video processing architecture. We note that the memory lines are synthesised on the FPGA while the memory image used the external SRAM memory. Then, 256 Kbytes are used in the SRAM to implement the image memory of the smoother stage plus 256 Kbytes to implement the optional image memory required to rectify the image orientation.

TABLE I
Ressources Utilisation Summary - Cyclone II EP2C35F672

	LUT	Flip-Flop	RAM Bits	Multipliers
de2tv	3537 (5%)	1700 (5%)	58368 (12%)	20 (29%)
edge detector	2057	739	33792	2

VI. Educative issues

As mentioned in the introduction, this design project targets third year engineering students. For two years, it has been proposed to the students of the Phelma engineering School with the CIME Nanotech support. This experience lets think us that the project can be achieved into 7 supervised labs of 4 hours, plus several hours of personal work.

We think this design project presents several pedagogic interests. Indeed, the complexity of the signal processing algorithms implemented in this design project leads students to explore different architectures to choose the one which presents the better performance/complexity tradeoff. As an example, the IIR filter used in the smoother stage can be implemented along different architectures which lead to different performances or complexities (data precision, hardware resources, latency...). In the same way, the clock frequency constraint (54MHz in the edge detector) imposes to implement *pipeline* technic. The students have to explore different combinational partitioning solutions to chose the one which matches the clock requirements and presents the lowest latency. We think these different issues perfectly introduce the concept of the adequacy between an algorithm and its hardware implementation.

Moreover, the Garcia-Lorca implementation presents some tricky memory optimisations that seems very interesting for digital designer. From our experience, the implementation of these special memory management appears as the biggest difficulty for the students.

As well, the complexity of the project, as the fact it is carried out by groups of two or three students, leads them to propose an efficient design and validation methodology. Indeed, each student takes in charge the design and the validation of a sub-part of the project before gather together the whole project. Then, they have to clearly specify the behaviour of the different parts as well as the interfaces.

Finally, and more generally, the project covers the entire design flow of integrated electronic systems, from the architecture specification to the hardware implementation.

VII. Conclusions

This paper presents a digital design project that consists in implementing a real-time edge detection video filter on a FPGA development board. The section II introduces the edge detector theory, while the section III describes the Garcia-Lorca hardware implementation on which the project relies on. The fourth section presents the design environment and especially the video processing architecture where the edge detector is implemented. The section V provides some labs results, and the pedagogic interests of the project are discussed in the last section. To conclude, we note that the framework proposed here can be reused to implement any other kind of video filter.

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Export Mobile Device Display Content

Applications and User Interfaces for Inter-Vehicle Communication

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***Abstract*—Within the Master Project *"Wireless Mobility"* this project was offered to IT Master Students during the second and third term and ran approximately over ten months. The project team developed a demonstrator platform to export the display content from a consumer mobile phone to a larger remote display, e.g. installed in a car. The key requirement was the utilization of non-proprietary technical solutions. This constrain did not limit the scope to standardized solutions only, but proprietary solutions ought to be open source or somehow accessible for the interested community. One important goal of this project was the awareness of latest design constraints and challenges in the Embedded Systems and System on Chip (SoC) area through a Project Based Learning (PBL) strategy. In this context, the students developed personal design competence, including specification, design trade-offs, design for testability, analysis and verification, and realization.**

Keywords-Embedded System; wireless; mobility; Car PC; Project Based Learing;

I. INTRODUCTION

The Master Project *Wireless Mobility* was offered in cooperation with the company *Task9* to IT Master Students during the second and third term and ran approximately over ten months. Today mobile devices such as smart phones usually provide sufficient processing power for complex applications like street maps, internet browsers or multimedia players. In a typical scenario the consumer carries his device, e.g. a personal digital assistant (PDA), with him and has a multitude of personal data stored on the device memory like music files or podcasts. On top of these applications, one can imagine, that mobile phones can connect nearby cars to each other enabling so called consumer car communication based services.

A potential use case for communication between cars is media sharing, i.e. one car streams music that other cars in front or behind can receive. This way, the cars nearby are able to listen to music which is stored only on one car's PC. This scenario offers even more potential: Thinking of the car PC's music collection, one could imagine a kind of need-list broadcasting. The driver could provide a list of songs he would like to get from other cars in case they possess them. Thus, the car's music collection can be updated whilst stuck in traffic. As a further possibility, radio signals can be transferred between near by cars, which could obviate the need of antennas.

Figure 1. Car PC receives navigation data from a mobile device.

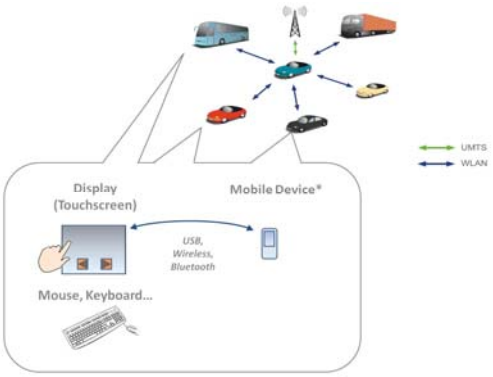

Figure 2. Internal and external car link connections [1, 2].

The mobile device provides various applications that can be controlled by the Car PC. For instance, a music collection can be stored on the mobile device and accessed by the Car PC. Another example is the use of navigation software on the device as shown in Fig. 1.

The car does not need a special navigation system any more but can rather use the mobile device in interaction with the Car PC for this very purpose. These examples demonstrate the advantages of having just one PC in a car that can be used by a variety of applications and devices such as mobile devices.

Anyhow, typical car communication has been expected to start with safety critical applications to improve traffic situation. However, from a technical point of view it is already feasible to interconnect cars via WiFi and cellular technologies by implementing their infrastructure, see Fig. 2.

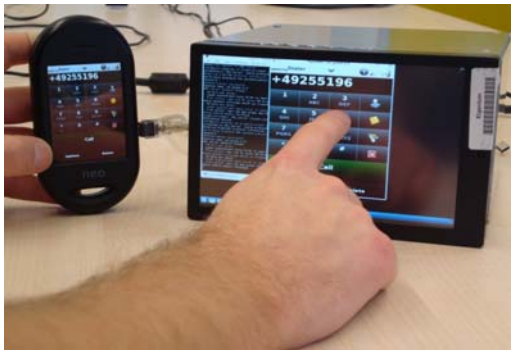

Figure 3. Dialing application forwarded to and used by Car PC.

Figure 4. The Car PC comprises off-the-shelf components only.

Additionally, this paper gives a brief introduction into a possible infrastructure scenario inside a car. Given the idea of an established connection between a mobile device inside each car and the car's infrastructure several applications become feasible. For example, it becomes possible to run a street map application on a mobile device and forward it to an in-car device. In this scenario there is no need for complex and expensive hardware inside the car. A single display with associated input devices is sufficient as all the processing is done on the mobile device. To establish the recurred link several opportunities have been examined within this project.

II. Design

To handle the mobile device appropriately while driving without violating any existing traffic law there is the need for an embedded device in the car which is easy to handle. Therefore, it is conceivable to install a display or touch screen with a minimum of processing power and software which is embedded in the dashboard of the car and connected to one or more mobile devices (see Fig. 2 and Fig. 3). Depending on the complexity of the car-display it is possible to use different standard connection types like USB, Bluetooth or even WiFi to connect these devices and transport different kinds of information like display data. With this approach it is possible to export the user interface of a single application from the mobile device to the car-display and control it remotely with the help of any input device directly connected to the car-display

As depicted in Fig. 4, we developed the so called Car PC as a test vehicle out of off-the-shelf components. To provide an easy to use interface, the PC is equipped with a touch screen display. The integrated Intel Atom Platform, a Solid State Disk and various communication components (Bluetooth-, GPS-, UMTS- and Wireless adapters, and USB 2.1) ensure high performance and widespread communication possibilities.

III. Challenges

The Car PC fits the standardized radio slot so no additional space is necessary. Common communication standards are Bluetooth, GPS, UTMS, Wireless and USB. A wireless communication is considered as the most appropriate one. The Car PC is embedded in an enclosed environment. That is why potential heat problems could occur. A possible solution for that could be heat pipes that lead the heat away from the PC's case. Feasible operating systems are Microsoft Windows and Linux. Windows provides driver support for most devices, so this would be a good choice for a smooth running PC. Using a Linux operating system like Ubuntu or Debian, on the other hand, offers more flexibility to customize the system. The demonstrator PC currently uses Ubuntu 9.10 in cooperation with the 9.04 version's kernel 2.6.28, because the 9.10 kernel tends to be problematic regarding wireless adapters. Furthermore, the calibration of the touch screen display was not supported. A Debian operating system should be given a try in a further development phase, because there might be less problems regarding the tools, specially because the current kernel 2.6.32 comes with out of the box USB touch screen support.

IV. Results

The main achievements of this project are a prototypical endpoint to receive mobile device display data and a huge technical expertise how to set up the communications and the configuration of the selected protocols. The following knowledge was gathered:

VNC transfer is straight forward to use. The advantage is platform independency. A major drawback is the poor performance caused by its frame buffer protocol implementation. Tunneling single X11 applications including window managers (e.g. KDE, gnome, wmaker) via SSH was successful with good performance. Forwarding the X11 window system was not possible with the current configuration because of the operating system used, but worked on different configurations and therefore could be a desirable goal.

V. Conclusion

The developed Car PC provides a perfect platform for further development of non-proprietary technical solutions. Connecting a mobile device to the PC and establishing a stable transfer with good performance between them still needs further development, as the available standards like X-forwarding need to be improved substantially. One could imagine a System-on-Chip solution that comprises all essential components of the Car PC and integrates them into a single chip. In addition, the costs of such a SoC solution could be reduced.

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Synopsys' Interoperable Process Design Kit

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Abstract

An Interoperable Process Design Kit (PDK) for a 90nm custom design flow, including all the necessary design rules, models, technology files, verification and extraction command decks, scripts, symbol libraries, and Parameterized Cells (PCells) is described. The components of the PDK augment all types of custom design for educational and research purposes. Although the PDK does not contain any foundry information, it allows close to real 90nm technology with high accuracy to be implemented in the designs.

1. Introduction

In the age of nanometer technologies, universities strive to provide the most modern and high quality studies in IC design. In addition to Electronic Design Automation (EDA) tools and Educational Design Kits (EDKs [1]) from leading companies, Process Design Kits (PDKs) for different IC fabrication technologies are also necessary. But the creation of such PDKs is met with numerous difficulties such as labor-intensive development and considerable complexity of verification. The most important challenge is the intellectual property (IP) restrictions imposed by IC fabrication foundries that do not allow universities to copy their technology into PDKs. To overcome this challenge, Synopsys created a PDK that has characteristics very close to real foundry design kits but does not contain confidential information from foundries that restricts its use.

2. Overview of the PDK

Synopsys created an interoperable PDK that is free from intellectual property restrictions and is targeted for educational and research purposes. It is aimed at programs for training highly qualified specialists in the area of microelectronics at universities, research centers and professional training facilities. The PDK enables students to master today's advanced design methodologies and the capabilities of Synopsys' state-of-the-art custom implementation IC design tools. It allows students to design different analog ICs and IPs using 90nm technology and Synopsys' EDA tools.

The Synopsys PDK contains the following: technology files: physical verification files, parasitic extraction files, Spice models, schematic symbols, PCells, and scripts.

For the PDK's development, an abstract 90nm technology was used. While the PDK does not contain actual foundry data, which is confidential information from foundries, it is very close to real 90nm technology. Using abstract technology allowed Synopsys to create an interoperable PDK that can be used for study and research of real 90nm design characteristics.

3. Description of the PDK components

3.1. Technology Files

The technology files provide technology-specific information, such as the names and physical characteristics of each metal layer and the routing design rules. Technology files include technology, display resource and mapping files:

1. Technology file contains layer information, design rule definitions, and associations with packets defined in the Display Resource file.
2. Display Resource file (DRF) contains the colors, fills and stipples, as well as packets, which are combinations of each. These packets are later used by the layout tool to show layers that are associated with a specific packet.
3. Mapping file maps the OpenAccess (OA) layer names to the GDSII layer numbers and data types. It is used during importing and exporting designs in GDSII format.

3.2. Physical verification files

Physical verification files include Hercules runset files for Design Rule Check (DRC) and Layout vs. Schematic (LVS) checks. DRC checks compliance of physical structures to design rules. LVS performs a comparison process that verifies whether the geometric or layout implementation of a circuit matches the schematic representation. Runset files are needed to instruct the tool on the operations performed.

1. DRC runset file is used by the DRC software program that analyzes the data in the layout and calculates its interaction (spacing and overlaps) to other layers.
2. LVS runset file is used by the LVS software program that extracts the intended devices and their parameters to compare with schematic netlists.

3.3. Parasitic extraction files

Parasitic extraction files are used by the parasitic extraction software program that extracts parasitic capacitance, resistance and/or inductance from circuit layout. StarRC, the parasitic extraction tool from Synopsys, uses the Interconnect Technology File (ITF), TLUPlus models (TLU+) as well as mapping and command files as its input. ITF defines a cross section profile of the process. TLUPlus models are a set of models containing advanced process effects that can be used by the parasitic extractors in place-and-route tools for modeling. The Mapping file maps layers in the technology file to the layers defined in ITF. The command file is used to instruct the tool on the extraction process.

3.4. Spice Models

The generic Spice model library is based on the Predictive Technology Model [2] and contains the following devices:

- transistors
  - 2.5V devices: thick oxide MOSFETs
  - 1.2V devices: thin oxide MOSFETs with typical, high, and low threshold voltages.

    For these devices five corners were created depending on the performance of NMOS and PMOS transistors (fast, slow or typical) with varying threshold voltage and gate oxide thickness: TT - both typical; FF - both fast; SS - both slow; SF – slow nmos/fast pmos; FS – slow pmos/fast nmos.
- diodes
- unsalicided and salicided poly resistors, P+ resistor
- varactors
- inductors
- capacitors
- BJTs

In order to estimate the accuracy of the SPICE models, the models' parameters were scaled to 0.25um technology to compare them with the characteristics of known 0.25um models (Figure 1). A set of DC transfer curves was obtained and the middle curve from the set was chosen as a typical corner for 2.5V devices, thereby assuring that it is close to a real foundry process.

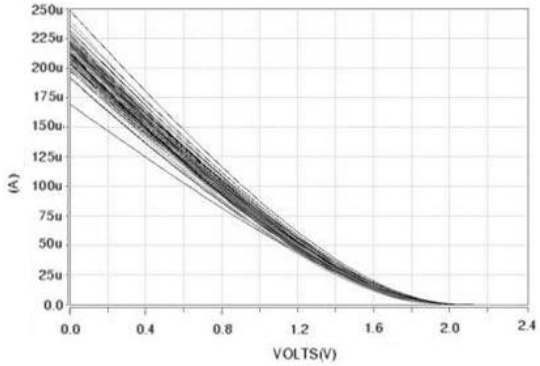


Figure 1. Set of .25um Transfer Curves

FF, SS, SF and FS corner models were formed by changing the threshold voltage (v_{th0}) and oxide thickness (tox) in the range of +/-5%. Figure 2 shows the transfer curves for TT, FF and SS corners of a thick oxide NMOS model.

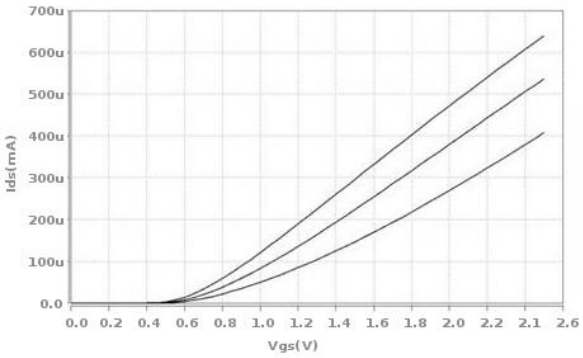


Figure 2. TT, FF and SS corners of 2.5V thick oxide NMOS

3.5. Schematic Symbols

The interoperable PDK includes an OA library that contains schematic symbols for devices such as MOS transistors, resistors, BJTs, diodes, varactor, inductor, and capacitor. The symbols were developed to work in any OA compatible [3] tool so the 90nm PDK is interoperable. The Synopsys OA compatible tool is Custom Designer.

3.6. PCells

A parameterized cell (PCell) is a layout cell generator programmed with a scripting language. Each PCell has a pre-defined set of parameters that can be strings, boolean, or numeric values. After execution of code by an interpreter it generates a cell view in an OA database. PCells included in the interoperable PDK are written in Python, which enables use of object-oriented techniques. The full advantages of object-oriented methodologies are applied to the creation of PCells. They can be used to reuse the code by defining well formed inheritance trees thereby reducing development time.

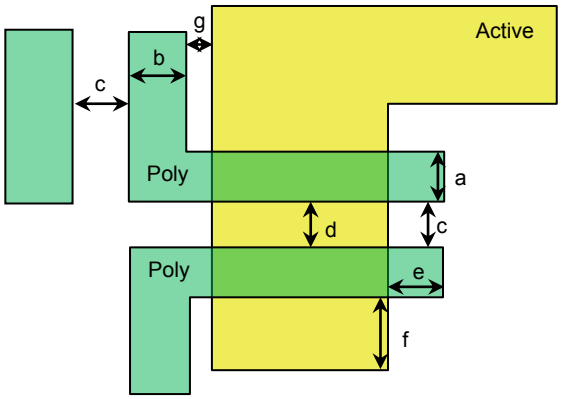
3.7. Scripts

Scripts are commonly used to do various functions in an OA compatible editor while using symbols and PCells. The common uses of scripts are: LVS, DRC and Extraction setup, invalid input checks, integer checks for parameters (m, nf, series, parallel, etc.), min/max checks and off-grid checks for non-variable inputs. Scripts can throw warning/error messages or even change parameters if the change is unambiguous. The scripts that perform checks are callback scripts tied between the Schematic or Layout editor's graphical interface and the PDK. This approach enables users to fully integrate the PDK components into the editor allowing the user to work with the PDK in a familiar

environment. These scripts, though invisible to the user, provide a means to work with device parameters in the editor's native dialog boxes. They also perform checks, report errors and calculate device electrical parameters based on the physical dimensions and vice-versa. For example, callback scripts for resistor can calculate resistance if the user provides the dimensions, and can calculate dimensions for the needed resistance value.

3.8. Design Rules

These rules were created by using the MOSIS Scalable CMOS (SCMOS) design rules. They provide greater portability of designs than if 90nm rules were developed because the sizes in 90nm rules can be larger by 5-20% than those in real foundry processes. An example design rule is illustrated in Figure 3.



a=0.1, b=0.3, c=0.18, d=0.2, e=0.18, f=0.16, g=0.05um

Figure 3. Example Design Rule

Also design rules contain a GDSII Layer Map. It maps layer names to the corresponding GDSII layer numbers used in the 90nm process. Some layers such as dummy, marking, and text, have been added to the MOSIS layer map. A sample of the layer map is shown in Table 1.

Table 1. Sample of Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in TechMap File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	NWELL	NWELLi	NWELL i	NWELL
2	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL

…

4. PDK's deployment

Currently the PDK is in use for both educational and research purposes by students in microelectronics area at a number of universities: State Engineering University of Armenia, Yerevan State University, Russian-Armenian Slavonic University, Moscow Institute of Electronic Technology, etc. Use of the PDK is highlighted in several courses: RF IC Design, Analog IC Design, Mixed-Signal IC Design, etc. The PDK is used in these courses for implementing both laboratory works and course projects by students. For example, in the Analog IC Design course, the laboratory works cover all the schematics that are taught during the course and students implement them using devices included in the 90nm PDK. Additionally, the course project is based on designing different operational amplifier schematics using the 90nm PDK and extracting various characteristics. Results show that using the 90nm PDK in course projects and laboratory works is more effective than relying on generic PDKs because they lack the necessary technology-specific effects. As the field of microelectronics constantly evolves, students need to be able to study as much real effects as possible to become competitive. Also schematics in such courses as RF IC Design or Mixed-Signal IC Design usually include devices like resistors, capacitors and inductors that have complex layouts. The presence of PCells for these devices not only enables students to easily design large circuits, but also lets students learn their complex structure. Although foundry-specific design rules are not included in the PDK it does not impact the educational process because most of the real effects are included.

5. Future PDK development

To keep pace with industry advancements and to support smaller process technology nodes, new PDKs may be created. Development to support new device structures in the 90nm Interoperable PDK is ongoing.

6. Conclusion

An interoperable Process Design Kit (iPDK) was created for educational and research purposes. It is free from intellectual property restrictions and is representative of industrial design kits. It can be used in a wide range of design flows for digital, analog and mixed-signal designs using Synopsys' EDA tools.

7. References

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[3] OpenAccess Documentation (http://www.si2.org/?page=621)

Integrating Microelectronics Into A Distance Learning Course

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***Synopsis*— The implementation of a M.Sc.-course in electrical engineering at the Hochschule Darmstadt [2] is outlined. The curriculum and in particular the microelectronics content is discussed. The mixture between hands-on skills and distance learning is not straightforward and has to be balanced for an optimum outcome for the students. Microelectronics is seen as a basic technology which broad applicability and hence is embedded in a more general curriculum, which cover non technical subjects as verbal communication in a professional environment and economics as well as technical subjects from automation and software engineering.**

Keywords- Distance learning, microelectronics and automation education, teaching strategies, course set up

I. General Description of the M.Sc.-Course

Postgraduate education and life long learning is of central focus in the Bologna process and in the rapidly changing world of the electrical and the electronic industry. Therefore ongoing education parallel to the professional career has to be provided by the universities and this not only in business administration but in technical subjects as well. This was the motivation for our institution to develop a distance learning course in Electrical Engineering leading to a Master of Science (M.Sc.) degree. The course duration is 6 semesters part time which is equivalent to a four semester full time program equivalent to 120 credit points in the ECTS system. The development started in 2004. The course setting including curriculum, examination and teaching procedures passed the senate of the University in 2006, was accredited by the accreditation board of the agency ZeVA in 2007 and the first students entered in spring 2007.

Postgraduate further education in German universities has to be financed entirely from tuition fees. Therefore it was a prerequisite for a successful program that a substantial number of potential students can be addressed. Though microelectronics is of central importance in many fields of the industry, a program resting solely on this field would not sustain a self financed degree program. Since the number of engineers working directly in microelectronics manufacturing sites is limited, it was important to offer an interesting curriculum for a broad range of engineers in the field of electrical engineering.

To do so we developed a curriculum consisting of a blend of non-technical subjects (economics, soft-skills), general engineering subjects (simulation, signal conversion, control theory, embedded systems, and software development) and advanced technical subjects. In depth studies are offered in two potential fields of specialization: microelectronics und automation. An extension to electric energy as third field is in preparation. Students select one of these subjects as the central topic of their studies.

The first students started their studies three years ago and more than 50% of them chose microelectronics as their specialization. At the moment 81 students are enrolled. The annual fees are 4400€.

II. Cooparation and Costs

Since up-to-date laboratory equipment is very expensive and top-notch electronic teaching expertise is rare we started this course in cooperation with the University of Applied Science in Aschaffenburg [3]. Here colleagues focus on Chip-Testing and Electromagnetic Compatibility and as a newly founded institution Aschaffenburg offers first class technical equipment. Roughly 20% of the teaching load was taken over by professors of this institution. The cooperation also facilitates access to a broader range of alumni.

As there was no particular know how in administration of distance learning courses available at our institution we linked our new post graduate course with the framework of the ZFH in Koblenz, Germany. The ZFH (*Zentralstelle für Fernstudien an Fachhochschulen*, Centre for Distance Teaching and Learning at Universities of Applied Science) is a scientific institution funded by the states of Hesse, Rhineland Palatina and Saar. There are some 20 distance learning courses available in the ZFH-framework, mostly in social sciences and economics, both on the graduate and on the postgraduate level. The M.Sc. in Electrical Engineering is the first technical course. The ZFH supplies valuable organizational support. All students apply for the course at the ZFH. This institution checks the qualification and submits the data to the Student Service Centre of the Hochschule Darmstadt. Student fees are also collected by the ZFH and assistance is given for marketing, press/media-relations and advertisement.

Since each postgraduate further education course has to be financed without university money, the ZFH provided an initial loan (400,000€), which covered the start-up cost for the course. The main cost factors are the wages for a scientific assistant and a secretary. The development of the course material was costly as well (150,000€). This loan will be fully paid back

The development of the course was sponsored by the Hessian Minister of Science and Arts and by the Zentralstelle für Fernstudien an Fachhochschulen (ZFH) [1] a scientific institution of the states of Hesse, Rhineland Palatina, and Saarland.

during 2010 at the end of the year the course will generate a small profit, which will be used for extensions, improvement, and adaptations of the program.

III. COURSE STRUCTURE AND CONTENT

The course is organized in modules, which in general have a workload of 10 ECTS credit points (CPs). The curriculum is organized in 4 sections (the total number of CPs is noted in brackets)

- A1, A2, A3: General technical and non technical skills (30)
- B: Specialization (30)
  - BA1, BA2: Automation
  - BM1, BM2: Microelectronics
  - B3: Optional subjects
- C: System development and Team-Project (30)
- D: Master Thesis (9 month: 30 CPs)

The curriculum is organized in parallel to the semesters of the university. Students may start in winter or in summer. In general 2 modules are covered by the students in each semester. The thesis project is scheduled for duration of 9 months.

In general we provide 4 sets of printed lecture notes in form of booklets per module. Each booklet (see Fig.1) has approximately 100 pages and it is associated with a workload of 2.5 CPs. Each lecture note is backed up by online material distributed with the e-learning software platform Moodle.

For every module we offer four mandatory classes (4x10 hours) at the university on weekends (Friday and Saturday). During these contact hours we have additional lectures, solve theoretical problems and work with the students extensively in the laboratories. The students take two modules per semester which corresponds to 4 contact weekends per semester. Exams have to be cleared in 180-minutes assessments for each module. Exams are written at the university at the end of the semester break giving the opportunity of an extensive preparation phase. Figure 2 shows a typical semester time table. The course material is sent out in three batches so that it is available four weeks ahead of the corresponding contact weekend.

Figure 1. Sample study booklets

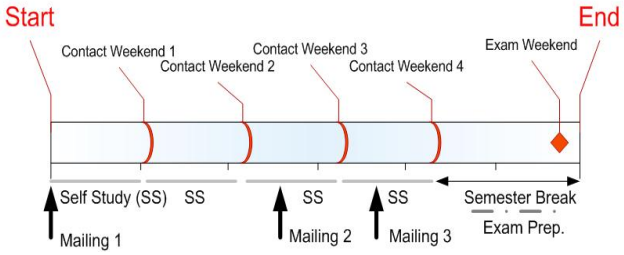

Figure 2. Semester timetable: 4 contact weekends and 3 mailings of course material. The semester break is reserved for repetition and exam preparation. Just before the start of the next semesters we have the examanition weekend with 2 module exams (duration: 180 minutes each)

In summary the theoretical electrical engineering content is 60 ECTS-points. 20 ECTS-points are obtained from non-technical subjects, and 10 credits are obtained from a successful completion of a team project in section C.

The following list shows the topics of the different modules (for details see [4]):

A1 Communication
- Verbal communication I
- Verbal communication II
- Presentation and moderation
- Leading by communication

A2 System-Design and Objects
- Hardware Description using VHDL and VHDL-AMS

Object-oriented Programming
- Part I (JAVA)
- Part II (JAVA)
- Part III (UML)

A3 Signals, Systems, Simulation
- Signal conversion (ADC, DAC, Sigma-Delta-Modulation)
- Signal processing: analog-, discrete time- und digital signal processing
- System theory: mathematical methods, test functions, stability and transfer functions
- Simulation: continuous simulation in time and amplitude, time and value discrete simulation, statistical simulation using Monte Carlo techniques

BA1 Control Theory
- Control systems I
- Control systems II
- Identification of dynamical systems
- Adaptive and learning control systems

BA2 Automation
- Automation-systems
- Sensors and actuators
- Bus systems and process automation
- Visualization of industrial processes

BM1 Design methodology
- CMOS Analogue Circuits: OpAmp-Design
- Digital Systems: Error correction, arithmetic

structures, filters
- Testing and Verification: Design verification strategies, chip testing and ATPG
- Low Power Design: design measures for reducing dynamic power consumption

BM2 Technology
- Reconfigurable Hardware: CPLD, FPGA and SOPC
- Semiconductor memories: DRAM, SRAM, Flash
- CMOS production technology: from mask making to wafer production
- Low Power Technology: Reducing static power consumption in nanometric CMOS-processes

B3 Optional subjects (Chose 4 out of 8)
- ASIC-prototyping
- Automotive microelectronics
- Mixed Signal Chip Design with TannerTools
- RFID
- LabView
- Process- and factory automation
- Robotics
- Image processing

C1 System development by Software- and Hardware-Engineering
- Software-Engineering I
- Software-Engineering II
- Embedded Systems I
- Embedded Systems II

C2 Team-Project and Project Management
- Project management in theory (2,5 CPs)
- Project: Planning and realization of a technical project in a team (7.5 CPs, 36 contact hours, 150 hours self directed project work)

C3 Economics
- Foundations of Economics
- Business administration and entrepreneurship
- Marketing and Management
- Information management using enterprise resource planning tools (ERP)

D: Master-project, thesis and viva voce: thesis topic from industry or university, 9 month duration, 30 CP

This general overview shows that microelectronics is part of a more general engineering environment. The modules in the microelectronics specialization are focused on industrial electronics. Here circuit design with field programmable devices, power reduction and development methodologies are of central importance. Testing and verification is covered as well. In order to understand the limits and possibilities of system integration foundation lectures on CMOS-technology are given. Facultative subjects which may be selected contain lectures on ASIC-prototyping, automotive electronics and mixed signal chip-design.

The total amount of electronic-related subjects is 30 ECTS credit points, which correspond to a workload of 900 hours or roughly one third of the taught contents in the master course. As Fig. 3 shows the specialization phase is in the second and third semester, where the students either select the modules BM1 and BM2 for microelectronics or BA1 and BA2 for in depth training in automation.

Note that the 8 optional sub-modules (B3) are either related to automation and microelectronics, but more general topics of current interest maybe chosen as well (LabView, RFID, Smart grids).

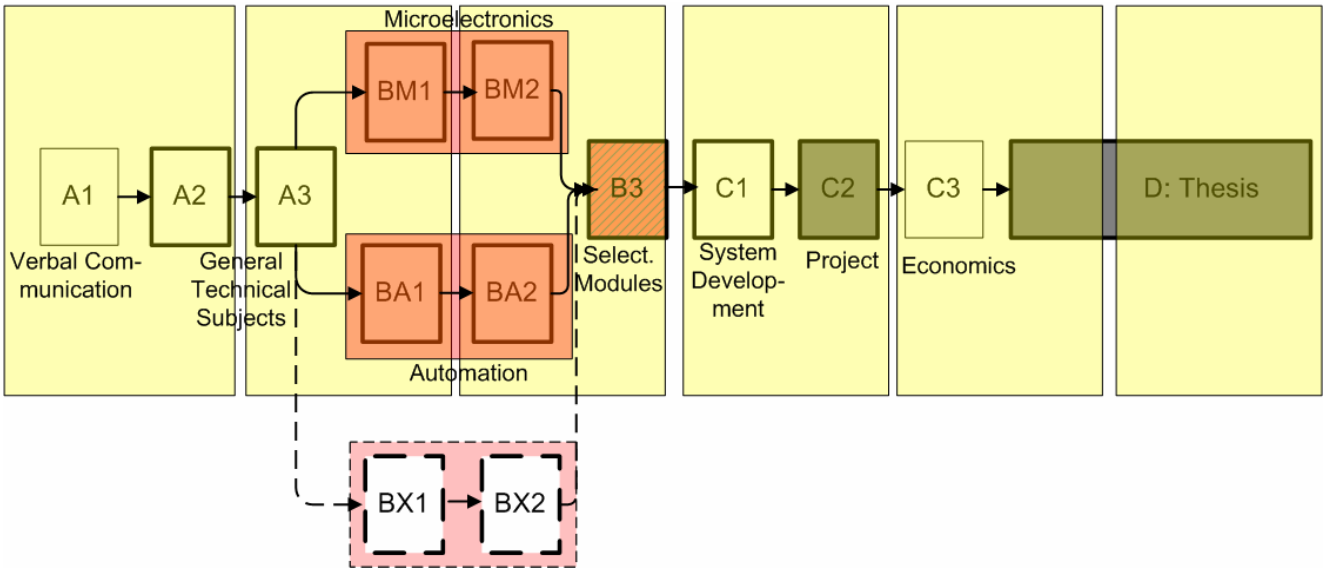

Figure 3. Course organization, semesterwise: 20 CP workload (i.e. two modules per semester). Students start with the general subjects A1 to A3, then they split up into 2 batches for automation and microelectronics respectively, select their topics of special interest in B3 and then come together for the software and poject modules (C1 and C2). Economics (C3) is the last theory module.The thesis (D) completes the studies. Potential extemsion of the programm with other fields of specialisation (BX1, BX2) are indicated by figures with dashed lines at the bottom of the graph.

IV. TEACHING AND LABORATORY WORK

Distance learning has its own challenges. In microelectronics tool usage and hands-on laboratory work is of special importance for the applicability of the knowledge gained in postgraduate education. In order to train these particular skills, we included practical exercises during contact hours at the weekends. EDA-tools are rather complex to handle. Since contact time is limited, this has to be made efficient by offering training during the learning and preparation phases of the students. So we provide students with instructions to use freeware or commercial tools for which student or trial versions are available. Hence the students can work at home on particular design problems in preparation of the contact periods.

In particular we supply a full commercial student version of MATLAB. MATLAB is the standard computer tool for automation and the student version covers all relevant toolboxes for this field. We use SystemVision from Mentor Graphics for VHDL, VHDL-AMS and SPICE modeling and simulation. Recently we recommend using the free version of Smash Dolphin since there are some problems with the current SystemVision trial version. For all these simulation tools we have full versions in our laboratories available. Chip-layout can performed at home with Microwind in order to introduce students into concepts and methodologies of the subject and in order to prepare exercises with professional tools at the university. In our labs we use the Tanner-Tools for Schematic Entry, SPICE-simulations and Layout exercises. For Logic Synthesis the ISE-Tools of Xilinx were found appropriate. ISE is available free of charge and includes a customized version of the HDL-simulator Modelsim which maybe used for VHDL-modeling. In the lab-sections during contact phases we also employ the EDA-toolset from Synopsys. In particular for testing we use ATPG generation and the ASIC-testing facilities of our partner university in Aschaffenburg.

V. LEARNING ORGANIZATION

To organize the studies we apply a blended learning concept with a strong emphasis on face to face teaching in weekend sessions. The reason for this approach is that in general students quit distance learning courses with a relatively high probability. Drop outs of 50% of each student batch over the program duration are not exceptional. If one investigates the structure and teaching concepts commonly used in other (commercial) distance learning courses, we see that for cost reasons and for reducing the organizational overhead most of the course work is done online and remote. Students are isolated and do not share and solve their problems and difficulties with others in a student team. We think that the standard remedy for such problems is an enhanced percentage of classroom teaching and laboratory work. This brings the students into classroom situations, which they are familiar with from their previous studies and solutions and assistance develop almost automatically. Internet platforms like Moodle, which we also use extensively for supporting the printed material, do not provide a similar open and interactive atmosphere, as nonverbal communication is suppressed by technicalities. Moreover after knowing each other personally from the contact phases the students find it easier to keep in electronic contact (chat rooms, e-mail) between the contact weekends. As we start with a soft skills module A1 where communication methods are discussed, the process of team formation is fostered by lots of practical exercises.

Figure 4. Students and staff in a classroom situation

VI. THESIS

Presently the first batch of students has passed the theoretical subjects and is in the concluding phase of their thesis project. It was found remarkable that only 40% of the students were offered a topic from their company. This is very untypical for universities of applied sciences, where almost every thesis (Bachelor-, Diploma-, or Master-Thesis) is performed in an industrial environment under mostly local supervision. In the distance learning course students had problems to allocate thesis topics in their company, as their department quite often had too much work to let an engineer work mainly on his thesis over a longer period. Research for other departments even in the same company was also not possible for various reasons.

So the university had to supply interesting and challenging research projects. This was done successfully as papers submitted to conferences and patent applications indicate.

However the thesis phase was found by the students to be the hardest part of the course. Continuous work on the project was found nearly impossible, since company requirements and commitments had to be met and also private life could not be disrupted for a nine month period. So the academic supervisors had to closely check for meeting the agreed schedules. Finally, all students submitted their thesis in time and at present the marking and the viva voce presentations take place.

VII. FURTHER DEVELOPMENTS

A distance learning course is never static but develops in order to keep up the interest of potential students. At present we work in two directions. As mentioned above we develop a third area of special interest, Electric Energy. There will be two new modules in part B (BE1 and BE2) focusing on Energy Conversion and production and on energy distribution and

storage. These two modules will replace BA1,2 and BM1,2 for a third batch of students in the second and third semester. Optional sub-modules for B3with focusing on issues of electric energy will be developed as well.

The second way of addressing new students is the usage of the modules or parts of them as separate training modules for engineers, who do not want to go through the complete program, but need training in special fields of engineering or want to improve their non technical knowledge. This activity will be launched this summer by special marketing events and advertisements on the internet or technical journals. Each training is completed by an examination and hence individual training units may be granted later if the student wants to go for the Masters degree.

VIII. Summary and Conclusions

We presented the course structure and the course content of a distance learning part-time Master of Science course in electrical Engineering, which started three years ago at the Hochschule Darmstadt in cooperation with the partners: ZFH for organizational issues, Hochschule Aschaffenburg, and Hochschule Darmstadt for providing content. The program runs for six semesters and has 120 CPs as workload and hence is equivalent to a full time program in 4 semesters. Specialization is possible in either automation or microelectronics. At the moment 81 students are enrolled. The first bath of students (11) handed in their thesis recently and will leave the university in May.

It is noteworthy that only 4 students out of eighty left the program without a degree, which is an excellent figure for a distance learning course. Part time studies are very challenging, in respect of balancing the competing requirements of professional work, private life and the workload of a master's course. It is found interesting that most of the topics for thesis research are not related to the company which employs the students but focus on ongoing research in Aschaffenburg and Darmstadt.

It should be noted as well that 30% of the students are financed in full by their employer and most of the students are supported financially or by adapted working hours by their company. So we are convinced that this course meets not only the demands of postgraduate education but also these of the professional community. We will continue to add additional subjects to the curriculum. Presently, as a third specialization, Electrical Energy is in preparation.

What is new in our concept? Firstly, the inclusion of a substantial amount of contact phases at the university to avoid student isolation and in order to integrate laboratory work in a distance learning environment. For all the computer labs we provide free software versions of our commercial tools for the students to train themselves at home in order to be effective in the limited time frame available in the laboratories. Secondly, the inclusion of a larger amount soft skills and economics to balance the advanced technical content with subjects of immediate applicability in the professional environment. Thirdly, the modular structure allows for easy extensions to new technical fields if required, e.g. electrical energy.

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Analog and Mixed-Signal Modeling with VHDL-AMS

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***Abstract*—This paper describes a compact tutorial on VHDL-AMS. Besides presenting its basic concepts, the tutorial highlights a top-down design approach using this language and details its model execution. The tutorial is intended for instructors with previous knowledge on VHDL and looking for a concise way to introduce VHDL-AMS on a pedagogical basis.**

I. Introduction

Since its standardization in 1999 [1], VHDL-AMS gained in importance increasingly. This language enables the modeling and simulation of analog and mixed-signal systems operating in different physical domains such as electrical, mechanical, and thermal domains. In contrast to VHDL, which received considerable educational attention at an early stage, see e.g. [2]–[4], contributions on teaching VHDL-AMS are rather rare.

Based on our long-time experience on its teaching at the Technische Universität Darmstadt and at the Baden-Württemberg Cooperative State University Stuttgart, this paper describes a compact tutorial on VHDL-AMS. To make the tutorial reusable and extendable for educators, we pay a special attention to pedagogical aspects. This includes –besides a thorough investigation of the VHDL-AMS concepts- a clear definition of the learning outcomes of the tutorial and provides a content structure according to these learning outcomes.

The remainder of the paper is structured as follows. Section II defines the learning outcomes and the structure of our tutorial. Section III details the tutorial content. Section IV presents the assessment and the evaluation. Section V concludes the paper.

II. Learning Outcomes and Tutorial Structure

In the style of constructive alignment [5] we formulate the learning outcomes of our tutorial as follows:

1) Identify the limitations of VHDL in modeling mixed-signal and mixed-domain systems and describe how VHDL-AMS covers these limitations.
2) Understand and apply a top-down design approach for analog systems using VHDL-AMS.
3) Model mixed-signal systems in VHDL-AMS.
4) Model mixed-domain systems in VHDL-AMS.
5) Understand and apply modeling in the frequency domain in VHDL-AMS.
6) Explain the model execution in VHDL-AMS.

While all the learning outcomes aim at widening the declarative knowledge of students, learning outcomes 2, 3, 4, and 5 also tend to deepen the functioning knowledge by applying the learnt theory to model and simulate practical examples using commercial tools. According to these learning outcomes our tutorial is structured in 7 units as depicted in Table I. An hour in this table is a 45-min lecture hour.

TABLE I: Tutorial Structure and Content

Unit	Subject	Form and Hours
1	Review of VHDL	Lecture (5h)
2	Introduction into VHDL-AMS	Lecture (2h) + Lab (3h)
3	Signal-flow and physical modeling	Lecture (2h) + Lab (3h)
4	Mixed-signal modeling	Lecture (2h) + Lab (3h)
5	Mixed-domain modeling	Lecture (2h) + Lab (3h)
6	Modeling in frequency domain	Lecture (2h) + Lab (3h)
7	Model execution	Lecture (3h)

III. Unit Content

A. Unit 1: Review of VHDL

As our tutorial is visited by students from different disciplines we consider precognition in VHDL as desired but not as a prerequisite. For students without any experience in VHDL, Unit 1 gives a concise introduction. A useful method to introduce VHDL relies on answering two general questions: What is hardware and how does VHDL describe it? The answers to these questions are outlined in Fig. 1 and Fig. 2.

According to Fig. 1, a hardware unit has an interface and an internal architecture. The architecture can be described by its structure as a connection of smaller components or by the function it realizes. A hardware function relates to processing signals by applying some operations to these signals and

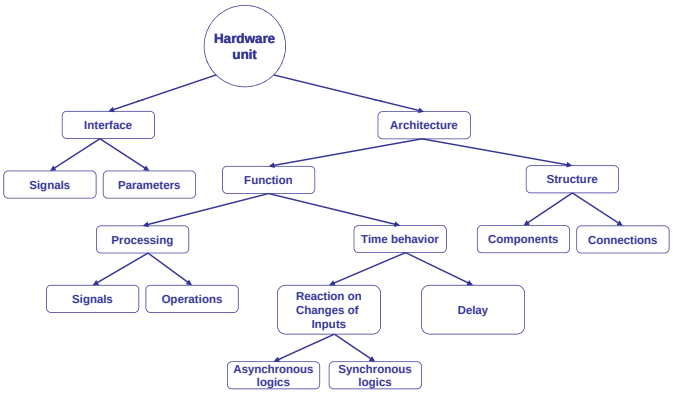

Fig. 1: General Description of a Hardware Module

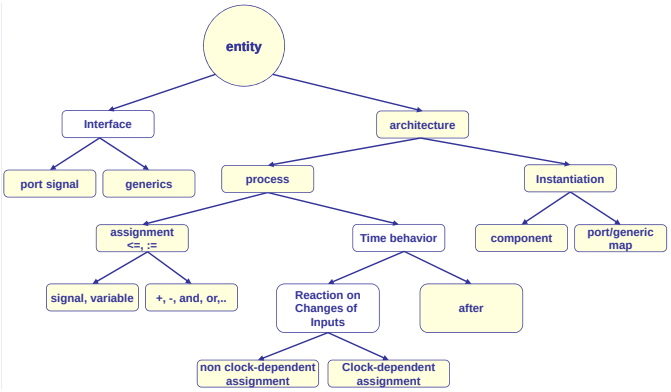

Fig. 2: General View on how VHDL Describes Hardware

producing other signals. Timing behavior of hardware can be specified by the processing delay, on the one hand, and by the speed of hardware reaction to changes of input signals, on the other. Asynchronous logic is specified by immediate reaction. Synchronous logic, in contrast, only reacts after a clock edge.

Fig. 2 outlines how VHDL reflects the hardware properties pointed out in Fig. 1. Based on this outline, we present in Unit 1 small VHDL examples, which illustrate the different language constructs. After that, more detailed aspects in VHDL are treated such as sequential versus concurrent statements, signal versus variables, and multiple-valued logic. In a next phase, the bit-accurate modeling and the cycle-accurate modeling in VHDL are treated.Bit-accurate modeling is important to building efficient data paths. The necessity of bit-accurate modeling can be demonstrated by using the integer type to model an 8-bit adder. The synthesis of this model will result in a 32-bit adder, which is highly inefficient. Cycle-accurate modeling corresponds to hardware description on the register transfer level (RTL), which is supported by most commercial synthesis tools. The advantage of cycle-accurate modeling can be demonstrated by writing a behavior model and an RTL model for a simple system, and by synthesizing them and showing which maximal clock frequency each model achieves. Other important topics in this lecture are parallelism, pipelining and finite state machines.

B. Unit 2: Introduction into VHDL-AMS

The purpose of this unit is to learn the essential concepts of VHDL-AMS including quantities, branch quantities, terminals, natures and simultaneous statements. An appropriate educational way for that is to show why VHDL fails to describe analog systems. In fact, VHDL is able to model an analog system, however, not in all the details required on the physical level. On this level, analog systems are characterized by the following three properties:

1) Value and time continuity
2) Acausality
3) Physical nature

The restrictions of VHDL to reflect the first property can be demonstrated by attempting to model a simple sinusoidal signal source as depicted in Listing 1. The problem of this model is the tricky way of generating a time-dependent

Listing 1: A Signal Source VHDL Model

```
1  entity SOURCE is
2    generic (AMP: real; FREQ: real);
3    port (signal SOURCE_SIGNAL: out real);
4  end entity source;
5  architecture BEHAVIOR of SOURCE is
6  signal CLK: std_logic:= '0';
7  begin
8    process (CLK)
9      variable V : real :=0.0;
10   begin
11     if (CLK'event and CLK= '1') then
12       SOURCE_SIGNAL <= AMP*sin(2.0*MATH_PI*
             FREQ*V);
13       V := V + 20.0e-6;
14       CLK <= not CLK after 10 us;
15     end if;
16   end process;
17 end architecture BEHAVIOR;
```

sinusoidal function. The function SIN defined in the package IEEE.MATH_REAL accepts only real values, while the time in VHDL is of discrete type. Note that the signal SOURCE_SIGNAL is a real signal, i.e. value-continuous, but still time-discrete which does not correspond to the physical case. To solve this problem VHDL must be enhanced by a new object class which represents value- and time continuous objects. This object class is denoted as *quantity* in VHDL-AMS. Additionally, a new time type must be defined, which allows this continuity. Therefore, VHDL-AMS provides a universal time type, which supports both time-discrete signals and variables, on the one hand, and time-continuous quantities, on the other. Modeling SOURCE_SIGNAL as a quantity can be seen in Listing 2. Note that the function ***now*** in VHDL-AMS is of the type floating-point, in contrast to the discrete type in VHDL.

To discuss the acausality property of analog systems consider Listing 3, which shows a possible VHDL model for a resistor. The problem of this model is considering the voltage as an input and the current as an output. In particular, physical systems are acausal, which means that not only the resistor voltage affects its current, but the opposite is true, too: The higher the resistor current, the more power is dissipated in other circuit elements and, thus, the lower is the resistor voltage. This acausality is attributed to the exchange of charge and energy with the environment and to the conservation laws ruling this exchange. To model these aspects new objects are required, which have no in/out mode, on the one hand, and

Listing 2: A Signal Source VHDL Model

```
1  ...
2  architecture BEHAVIOR of SOURCE  is
3  quantity SOURCE_SIGNAL: real;
4  begin
5    SOURCE_SIGNAL == AMP*sin(2.0*MATH_PI*FREQ*
         now);
6  end architecture BEHAVIOR;
```

Listing 3: A Resistor VHDL Model

```
1 entity RESISTOR is
2   generic (R: real);
3   port (signal V: in real;
4         signal I: out real);
5 end entity RESISTOR ;
6 architecture BEHAVIOR of RESISTOR is
7 begin
8   I <= V/R;
9 end architecture BEHAVIOR;
```

are subject to conservation laws, on the other. This object is denoted as *branch quantity* in VHDL-AMS and can either be a potential quantity (*across*) or a flow quantity (*through*). Note that a potential and a flow quantity are always needed to reflect the conservation of energy and charge. Listing 4 shows the VHDL-AMS model of the resistor.

Listing 4 also addresses the third property of analog systems. As a real system may operate in several physical domains, each branch quantity describing this system must be assigned to the domain it operates in. This aspect is essential to model the energy exchange between different physical domains and the associated energy conversion, e.g., from thermal to electrical form. A physical domain is modeled in VHDL-AMS as a *nature*. Assigning a branch quantity to some nature is accomplished by defining it between two access points of this nature. Such access points are referred to as *terminals* in VHDL-AMS.

Besides these essential concepts Unit 2 also treats:

1) The different types of simultaneous statements: simple, if, case, null, and procedural statements.
2) Model solvability rules
3) Tolerance groups and the attribute *tolerance*
4) The predefined attributes *dot* and *integ*

In the lab students model and simulate several electrical circuits including passive elements and analyze several aspects such as the resonance behavior of an RLC circuit.

C. Unit 3: Signal-flow and Physical Modeling

This unit introduces a highly important aspect of VHDL-AMS, which is the description of analog systems on different abstraction levels. This aspect distinguishes VHDL-AMS from other languages and tools, which only support signal-flow models such as MATLAB or circuit-level models such as

Listing 4: A Resistor VHDL-AMS Model

```
1 entity RESISTOR is
2   generic (R: real);
3   port (terminal P1, P2: ELECTRICAL);
4 end entity RESISTOR ;
5 architecture BEHAVIOR of RESISTOR is
6 quantity V across I through P1 to P2;
7 begin
8   V == I*R; -- or I == V/R;
9 end architecture BEHAVIOR;
```

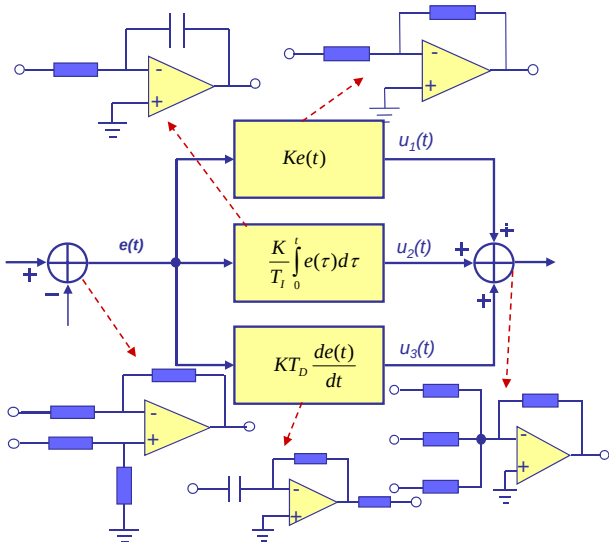

Fig. 3: A PID Controller: From Signal-Flow to Implementation

SPICE. *Free quantities* and *port quantities*, which are essential concepts for writing signal-flow models, are learnt in this unit. For a complete understanding of the top-down design approach we first describe a PID controller as a signal-flow model and write a testbench to simulate it. In the next phase, which is a lab session, each block is successively replaced by its implementation model using operational amplifiers as depicted in Fig. 3. The refined models are simulated using the same testbench used to simulate the signal-flow model.

D. Unit 4: Mixed-signal Modeling

In this unit three aspects of mixed-signal modeling in VHDL-AMS are learnt. These are:

1) How to convert a digital signal into an analog quantity using the attributes *ramp* and *slew*?
2) How do digital events affect the operation conditions of the analog system using *break* statement?
3) How does the analog part release digital events using the attribute *above*?

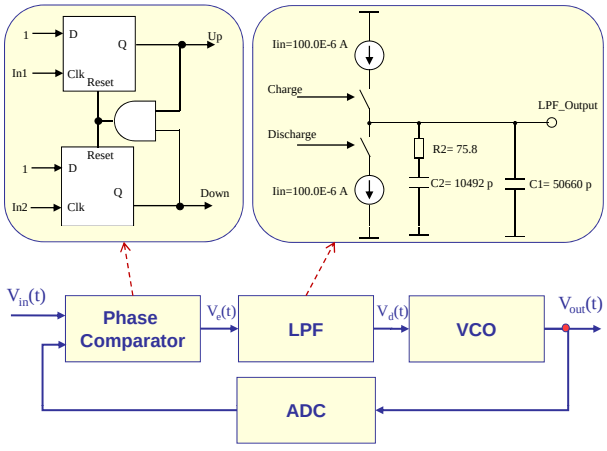

Fig. 4: A Digital PLL as a Mixed-Signal System

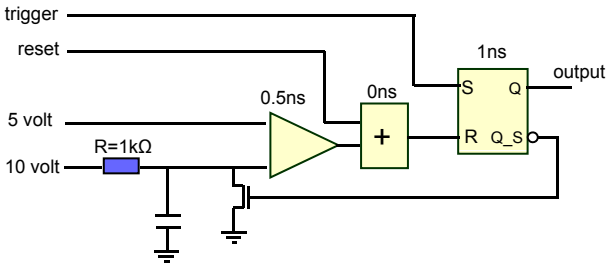

Fig. 5: A Simple Timer for Illustrating Model Execution

Several examples such as AD converters, DA converters, and switch transistors are represented. In the lab a digital phase-locked loop is modeled and simulated, see Fig. 4. A digital PLL is a suitable case study for mixed-signal modeling as it includes both a digital-analog interface (charge-pumb LPF) and an analog-digital interface (ADC). In a further step, the PLL is extended to a frequency synthesizer using a counter.

E. Unit 5: Mixed-domain Modeling

In this unit the following topics are treated:

1) Understanding the IEEE standard packages describing the different physical natures
2) Declaration of own natures
3) Modeling of non-electrical systems
4) Modeling of heterogeneous systems

In the lab students model a gearbox, a DC motor, and a self-heating diode.

F. Unit 6: Modeling in Frequency Domain

In this unit the following points are discussed:

1) The predefined enumeration *domain_type*, which has the values *quiescent_domain*, *time_domain*, and *frequency_domain*.
2) The predefined signal *domain* of the type *domain_type*, which is used by the simulator to determine the simulation mode. At the beginning of simulation, *domain* is always set to *quiescent_domain* to determine the operation point of the system. After that, *domain* is either set to *time_domain* for transient simulation or to *frequency_domain* for frequency simulation. In the latter case a small-signal model is created.
3) *Source quantity* used for the frequency analysis.
4) The attribute *ltf*, which defines the Laplace transfer function for some quantity.

The topics of this unit are illustrated using filter circuits and different transfer functions.

In the lab a stability analysis of the PID controller studied in Unit 3 is performed.

G. Unit 7: Model Execution

The last unit treats the execution of a mixed-signal model in VHDL-AMS, which proceeds in three phases: analysis, elaboration, and execution. Fig. 5 shows a mixed-signal circuit which we use to illustrate the topics of this unit. Note that the timer includes analog components (R and C) and digital components (flipflop and OR-gate), as well as an analog-digital component (comparator) and a digital-analog component (MOS). The topics treated here are:

1) The elaboration of the analog part of a model. This results in the structural equation set describing the conservation equations, e.g., the mesh and node equations.
2) The elaboration of the digital part of a model. This results in a set of processes communicating through nets.
3) The VHDL-AMS simulation cycle which is an extension of the VHDL simulation cycle and includes the analog simulation between two digital events.
4) The interaction between the digital kernel and the analog solver. This interaction occurs when a break statement is executed by the digital kernel or when some threshold defined by the *above* attribute is exceeded during analog simulation.

IV. Assessment and Evaluation

The assessment for our course can be described both as formative and summative, according to [5]. In the formative assessment, which is usually applied in the lab, students perform the design assignments described above to deepen the functioning knowledge. In the lab, students have the possibility to ask questions and get feedback about their design and reached results. Lab assignments are not graded. In this way, we intend that students feel relaxed in accomplishing the assignments, which is essential for success. The summative assessment is performed in form of a written 90-minute exam to see whether and how well students acquired the intended functioning and declarative knowledge. In 2008 the exam was written by 29 students and passed by 24 of them, which corresponds to the general experience with this course.

On their part, students evaluate our course every year anonymously by filling out forms with questions about the technical and didactical aspects of the course. Fortunately, our course has always got above-average marks. This was confirmed by the student council, which awarded it twice as the best course in our department in 2005 and 2007.

V. Conclusion

A compact tutorial on VHDL-AMS was presented to help instructors with planning similar courses on modeling mixed-signal and mixed-domain systems.

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A Platform for VHDL Visualization

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***Abstract*—This paper presents a new platform for VHDL visualization to support undergraduates in learning this hardware description language. The presented platform, denoted as VISUAL-VHDL, enables students to enter their own VHDL code and control an animation process, which shows step-by-step how the different language constructs are treated to synthesize a complete digital circuit. Furthermore, VISUAL-VHDL enables the visualization of the Quine-McCluskey algorithm, which is embedded in our tools to optimize the circuit resulting from synthesizing the VHDL code.**

I. Introduction

VHDL is a well-established language for hardware description in industry and research and has gained considerable attention in education [1]–[3]. An efficient learning of VHDL relies on understanding it as a hardware description language and on a clear differentiation between this language and traditional programming languages such as C.

In particular, writing a software program mainly consists of understanding the problem, translating the specification into the language syntax, and testing the written program. Questions relating to resource allocation, mapping of tasks to resources, or scheduling are out of interest, as a rule. This is attributed to the fact that most computer systems today still include only one central processing unit —although two or more cores are common in current computers— which makes the problems of resource allocation and task mapping irrelevant during software programming. Due to the sequential operation of these CPUs, furthermore, the scheduling task is also trivial.

Using VHDL to model digital systems, in contrast, is highly different. Besides understanding the system specification, knowing the language syntax, and the need to test models by simulation, VHDL designers are responsible for solving all the above problems of allocation, mapping, and scheduling, along the way—or perhaps essentially. Understanding VHDL relies on the awareness that writing any VHDL statement may be associated with allocating a new hardware resource, mapping some task of the system specification to this resource, and scheduling the execution of this task at a specific time point or in a specific clock cycle.

To make students familiar with its basic concepts, we created a visualization and animation platform for VHDL. With the aid of these tools, denoted as VISUAL-VHDL, students can enter small VHDL codes and control an animation process to see how this code is processed to set up the corresponding digital circuit compounded of basic logical elements such as gates, flip-flops and multiplexers.

TABLE I
Commercial Schematic Viewers vs. VISUAL-VHDL

Commercial Schematic Viewers	VISUAL-VHDL
Schematic is generated after completing the synthesis process which often takes a considerable amount of time.	Schematic is generated on the fly.
Schematic is output all at once. Understanding which VHDL statements were mapped to which schematic elements often demands an accurate investigation of the schematic and the VHDL code.	Schematic is generated dynamically in an interactive mode. During this animation, relating VHDL statements and schematic elements are highlighted using colors.
Investigation of relation between the VHDL code and the schematic often demands a switching between the windows of the VHDL editor and the schematic viewer.	Both the VHDL code and the schematic are displayed on one window which considerably facilitates analysis.
Code optimization may hinder the understanding of the mapping process of the VHDL code to hardware elements.	Code optimization is done on demand. User can switch on or off the optimization option.
Code optimization is performed in the background.	Code optimization can be visualized in an auxiliary window.

VISUAL-VHDL differs from schematic viewers embedded in most commercial synthesis programs in several points, which spring from the educational merit of VISUAL-VHDL, as shown in Table I.

Animation platforms for data structures and algorithms in terms of pseudo code or software programs have long been used for educational purposes and evaluated for effectiveness [4], [5]. To our knowledge, neither VHDL nor other hardware description languages were addressed in the scope of such visualization environments, so far. VISUAL-VHDL is a first step in this direction.

The remainder of the paper is structured as follows. Section II provides a brief introduction into ANIMAL, which our platform is based on. Section III details VISUAL-VHDL. Section IV concludes the paper with a summary and an outlook.

II. ANIMAL

VISUAL-VHDL is a plug-in for ANIMAL, which in turn is a Java-based environment for algorithm visualization [6]. The animation is created by applying appropriate effects to pre-defined graphical primitives such as points, polylines,

Listing 1. Example for ANIMALSCRIPT

```
1 triangle ''d1'' (25,100) (25,110) (55,110)
2 polyline ''p0'' (35,0) (35,20) (85,20)
      (85,90) hidden
3 move ''d1'' via ''p0'' within 3000 ms
```

polygons, arcs and texts. For each primitive, several specific properties such as the size and the color may be defined. The animation effects include display, timed display, hiding, color change, movement and rotation. Animations are displayed with video player-like functionality including play, pause and a direct jump to a given step. ANIMAL takes as input a special ASCII-based script denoted as ANIMALSCRIPT, which defines the animation content in a flexible way [7]. Each line in ANIMALSCRIPT can represent a command compounded of a keyword and a number of parameters. Listing 1 depicts a section of an ANIMALSCRIPT file. In this section, a triangle is first displayed. Then a hidden polyline is specified. The triangle is finally moved along the polyline during 3 seconds.

III. VISUAL-VHDL

VISUAL-VHDL extends both the graphical library of ANIMAL and ANIMALSCRIPT. Figure 1 shows the general flow for generating an appropriate animation for a given VHDL code. During its analysis, the VHDL code can optionally be optimized on the Boolean level based on the Quine-McCluskey algorithm [8]. If desired, this optimization process can also be visualized step-by-step.

The next task is to generate an *extended netlist*, which is a structural description of the digital circuit enhanced with visualization and animation information. This information is generated in the style of ANIMALSCRIPT, so that it can be treated by ANIMAL. The circuit primitives of the extended netlist are selected from a graphical library, which was extended with new classes to support digital logic schematic. Besides the automatic approach, VISUAL-VHDL allows the generation of an extended netlist from a schematic editor.

The core functionality of VISUAL-VHDL consists in interpreting the extended netlist and constructing an animation

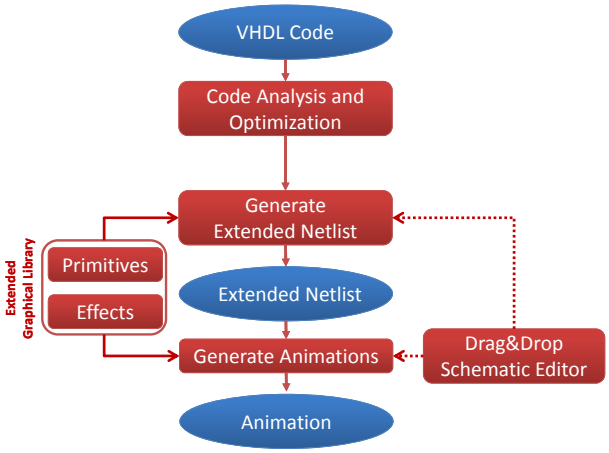

Fig. 1. Generation of an Animation for VHDL Models

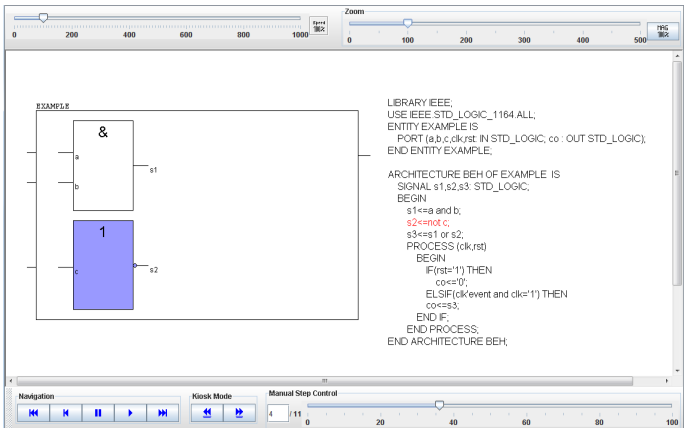

Fig. 2. Example for VHDL Animation, Processing the Assignment of the Signal S2

that can be viewed inside ANIMAL, utilizing the Java Swing library. This animation program can then be executed under user interaction to generate the circuit schematic corresponding to the analyzed VHDL code step by step. The user interaction is performed within the animation window with video player-like controls.

Figure 2 presents a screenshot of the animation window in an early step of the visualization process. Note how VISUAL-VHDL highlights the code row ($s2 <= not\ c$), which relates to the currently visualized digital inverter. In the final step, the animation window appears as shown in Figure 3.

The extended graphical library is based on the graphical library of ANIMAL and supplements it with new primitives to display logical gates, flip-flops, multiplexers, entities etc. The new special class *Wire* in VISUAL-VHDL is used to connect the terminals of different primitives.

In the following, we describe some important aspects of VISUAL-VHDL in more detail.

A. Code Analysis and Optimization

In its current prototype, VISUAL-VHDL supports the following VHDL language constructs: entities, ports, signals,

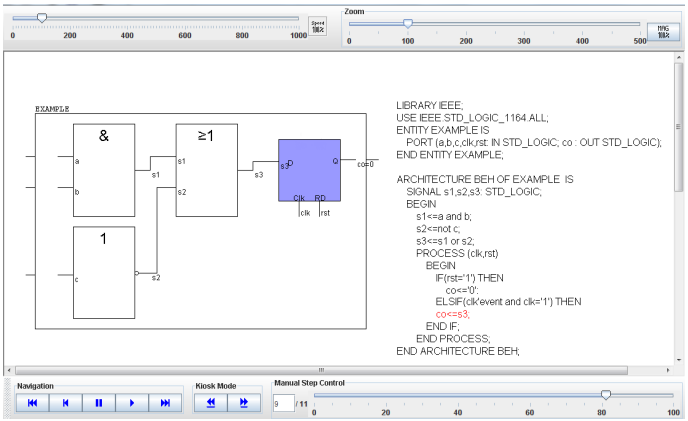

Fig. 3. Example for VHDL Animation (Last Animation Step)

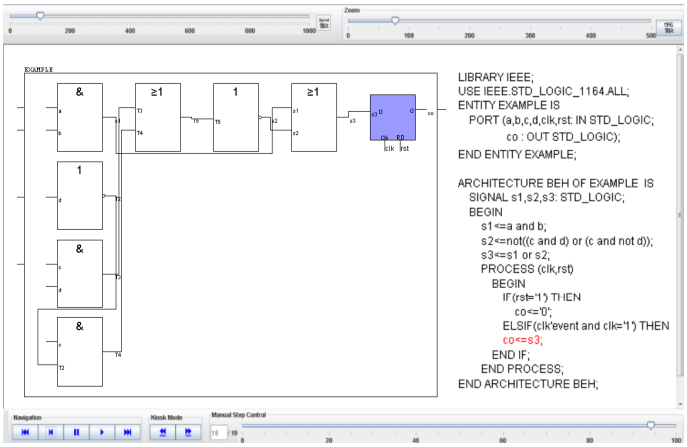

Fig. 4. Example for VHDL Animation (without Optimization)

architectures, processes, concurrent and sequential signal assignments, variables and variable assignments, conditional assignments, component declarations and instantiations.

From a design perspective, VISUAL-VHDL allows the visualization of VHDL models which presents behavioral, structural, and mixed models, i.e., models with both behavioral statements and component instantiation. Regarding behavioral models, both combinatorial and sequential logic are supported, so that a description on the register transfer level (RTL) is allowed. Description on the RTL level is the most well-known approach to specify hardware in commercial design flows. On this level, the designer takes the responsibility for bit-accurate resource allocation, task mapping, and cycle-accurate scheduling. Thus, with the aid of VISUAL-VHDL, students do not only learn VHDL and digital logic, but the de facto standard design approach on the RTL level.

Upon parsing and analyzing the VHDL model, VISUAL-VHDL offers an optimization of this model. VISUAL-VHDL currently uses the Quine-McCluskey algorithm [8] to find the minimal form of the Boolean function represented by the VHDL model. Students can switch the optimization process on and off to learn the effect of optimization on the synthesis result. Figure 4, for instance, visualizes the synthesis result of a given VHDL code without optimization. Investigating the code shows that the signal $s2$ can simply be determined by inverting the signal c as $c.d + c\bar{d} = c$. Thus, if the same code is visualized with optimization, the synthesis result would appear as given in Figure 3.

The Quine-McCluskey algorithm relies on finding prime implicants, which is an NP-hard problem. This algorithm is taught in many courses on logic design. Besides its usage during synthesizing the VHDL code, VISUAL-VHDL provides the possibility to visualize the proceeding of this algorithm. By this means, students learn about processes running in the background of the synthesis task.

B. Extended netlist

The extended netlist includes all the information needed for the dynamic visualization of the digital circuit. An extended netlist extends ANIMALSCRIPT with several primitives to visualize circuit symbols. During the animation process, an extended netlist is processed sequentially from top to bottom. Listing 2 shows the section of the extended netlist responsible for visualizing the flip-flop and its connection with the OR-gate according to Figure 3. In particular, this script section contains two animation steps parenthesized with curly bracket {}:

Listing 2. An Extended Netlist Section Relating to Figure 3

```
1 {color ''or1'' type ''fillColor'' none
2  d ''d1'' (421,117) (571,267) input ''s3''
       output''co'' clock''clk'' reset''rst''
       color black fillColor (153,153,255)
       depth 50
3  unhighlightCode on ''codeSource'' line 16
4  highlightCode on ''codeSource'' line 17
5 }
6 {wire wire_or1-0->d1-0 (404,192) (404,178)
      (421,178)
7 }
```

1) The first step performs the following four actions simultaneously. (1) The fillcolor of the OR-gate is removed. (2) A D-flipflop is visualized, with upper-left and lower-right corners at the position (421,117) and (571,267), respectively. Note that the y-axis in VISUAL-VHDL is directed downwards. The names of the inputs and outputs of the flip-flop are specified. The attribute *color* specifies the color of the flip-flop frame and the signal names. The flip-flop is finally highlighted by a fillcolor. (3) Line 16 in the VHDL code, which was highlighted in the previous animation step, is unhighlighted. (4) Line 17 ($c0 <= s3$) is highlighted.
2) In the second step, a wire from the output of the OR-gate to the input of the D-flipflop is visualized. Note that this wire is specified by three points, as depicted in Figure 5 schematically. See Figure 3 for comparison.

The automatic generation of an extended netlist for a given VHDL code is a highly complex task, which includes the following subtasks:

1) Determining the optimal placement of the logical elements.
2) Determining the optimal routing.
3) Determining the optimal animation.

The execution of the first two subtasks results among others in the (x, y) position data for all the elements and wires of the circuit. These data are supplied as parameters in the extended

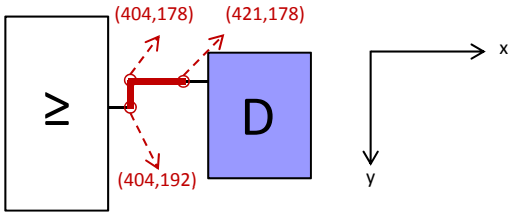

Fig. 5. Illustrating the Wire Dimensioning in the Extended

netlist, see Listing 2.

As mentioned in Section III, an extended netlist is generated at the end of the analysis and optimization phase. For this purpose, each element is specified by an attribute, which gives the number of the VHDL code line relating to that element. This attribute is required during the construction of the extended netlist to highlight the VHDL lines and the corresponding circuit elements synchronously.

For an appropriate display of the digital circuit, the animation field of the animation window is organized as a grid of numbered cells and channels. Logical elements are placed into cells, while wires are laid within the channels.

The grid size in terms of cell number and size is automatically adjusted according to the netlist content. Some rules are defined for simplifying the placement process. One rule relates to the placement of the circuit elements having external interface. Elements with external input signals, for instance, are placed in the leftmost grid column as far as possible. In contrast, elements with external output signals are placed in the rightmost grid column.

Visualizing wires in VISUAL-VHDL is a sophisticated task for the following reasons:

1) Wires should be as short as possible.
2) Wire segments can be only horizontal or vertical, not diagonal.
3) Suitable inflection points should be found.
4) Intersections should be minimal.
5) Wires should expand from the output of an element to the input of another. The expansion velocity should be adjustable.

To provide this flexibility, our *Wire* object is realized as a set of points. To visualize a wire consisting of several segments, the start points of each segment and the end point of the last segment are provided as parameters, see Figure 5.

C. Schematic Editor

The schematic editor as shown in Figure 6 is an extension of the graphic editor of ANIMAL. The new digital toolbar at the right includes symbols for 15 element types including gates, flip-flops, multiplexers and demultiplexers. Upon dragging and dropping a symbol, several parameters can be set, such as the name and the color. The number and the names of inputs can be entered for each gate. For a multiplexer, for instance, the user may set the number of the data inputs. The number of the control signals is then determined internally to avoid errors. A D-flipflop can optionally be provided with set, reset and/or clock-enable signals.

In addition to plotting, the schematic editor enables the simulation of simple combinatorial circuits. For this purpose, students can define the digital value for each input of the plotted elements. The simulation core determines the output values and visualizes them automatically.

IV. CONCLUSION

VISUAL-VHDL is a visualization platform for VHDL. It enables entering VHDL code and an interactive production of circuit schematic. By this means, students can learn the effect

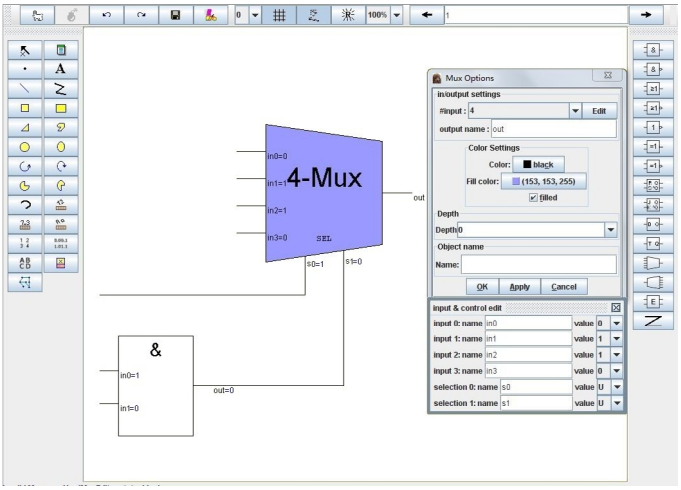

Fig. 6. VISUAL-VHDL Schematic Editor

of the versatile language constructs on the resource allocation, task mapping and scheduling in the target system. Educators may also take advantage of this tool to verify their models or to quickly generate circuit schematics using the drag&drop toolbar of the schematic editor.

VISUAL-VHDL is the first step toward a sophisticated system to support the learning process in many subjects of computer and electrical engineering. Currently we are developing a web interface for VISUAL-VHDL. Besides facilitating the usage of our tools the web interface includes a feedback system enabling students to evaluate these tools, so that we can prove their effectiveness in the near future. Furthermore, our platform will be completed and developed to support further features of VHDL and its event-driven simulation process. Other hardware description languages, such as Verilog, will also be considered.

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Implementing Constructive Alignment in a CDIO-oriented Master's Program in Integrated Electronic System Design

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Abstract *- This presentation reports on the design and implementation of a Master's program in Integrated Electronic System Design at Chalmers University of Technology from the perspectives of CDIO and constructive alignment. CDIO is an innovative educational concept originating from Massachusetts Institute of Technology (MIT) in which engineering fundamentals are stressed in terms of a* Conceive, Design, Implement*, and* Operate *process. Constructive alignment is a concept for creating an integrated learning environment where the teaching and learning activities are aligned with the assessment tasks to ensure that the achieved learning outcomes will correspond to the intended learning outcomes. In a process based on these two concepts, we have built a Master´s program that not only offers the basic theoretical background but also gives the student an opportunity to become competent in the skills that industry needs. Program focus is on the engineering process, on the technology platforms, and on the design tools and methodologies needed by the engineer to be able to contribute to the development of complex electronic systems and products while working in an engineering team.*

1. Introduction

Today, renewal of technical education of engineers at Chalmers University of Technology, and in Sweden at large, is most often discussed in terms of a Conceive-Design-Implement-Operate[1] (CDIO) process and in terms of constructive alignment. However, even though these concepts have been around for some time we believe that they are still new to many microelectronics education communities at universities around Europe. Therefore, we would like to describe our efforts to design and implement a new Master´s program in integrated electronic system design in terms of these two concepts.

In 2007, Chalmers University of Technology implemented a 3+2 two-tier Bachelor/Master's educational model, thereby abandoning its traditional one-tier integrated engineering education. The first three years of the new engineering programs are still taught in Swedish, and after having successfully completed these three years of study the student obtains a "Teknologie kandidat" degree, equivalent to the Bachelor's degree. From 2007 the two senior years are offered as advanced Master's programs and taught in English to stimulate EU student mobility and to provide opportunities for international students. The Electrical Engineering program offers six Master's specializations, one of these being the one in Integrated Electronic System Design (IESD) to be discussed here.

Already before 2007 Chalmers had some experience of international Master's programs from some one-year programs offered in English for international students. Two such examples are the Communication Engineering and the Power Engineering programs. However, these programs were given in parallel to the engineering specializations offered in Swedish for domestic students. Electronics design was one of the specializations offered in Swedish only. After 2007 all advanced specializations are offered in English only, in the form of integrated Master's programs.

While the predecessor specialization of electronics design was more or less an *ad hoc* collection of courses, the new IESD program has been carefully planned in detail. The program content and its learning outcomes have been presented before [1], but here we would like to focus on the planning and implementation processes in terms of CDIO [2, 3] and in terms of constructive alignment [4].

2. The Planning Process

Planning of the new Master's programs started already in 2006. In this process, we spontaneously formed an academic team that with enthusiasm and dedication set out to plan and implement the new program in Integrated Electronic System Design (IESD). During the planning process, the academic team was not fully aware of the CDIO concept. Nor were we then aware of the fact that Chalmers and two other Swedish universities actually were among the first universities in the world to become MIT partners in promoting the CDIO concept. Today the CDIO concept is widely accepted at Chalmers and future reforms of the Bachelor's programs are discussed in terms of CDIO. Also, the Ministry of Education plans to evaluate the education offered by Swedish universities in terms of CDIO and constructive alignment.

Nevertheless, when we now observe in retrospect the pedagogical ideas behind the IESD program and the program development process, we find many similarities with the processes for initiating CDIO that we can now read about on the web pages of the MIT Aeronautics and Astronautics Department [5]. Of course, these similarities are not there by sheer coincidence. Even though the CDIO concept was never explicitly spelled out, as far as we can remember, the instructions from Chalmers' university administration were quite clear that the new Master's programs were to be based on learning outcomes rather than on taught content.

In the planning process, the members of the academic team worked tightly together to formulate relevant learning outcomes based on the academic and industrial skills that we believed were needed by the graduating students to become productive and innovative engineers. A list of abilities was compiled and, for reference, these abilities were discussed with an informal group of industry representatives. Also, a matrix was formed in which the intended learning outcomes were mapped to the outcomes of the individual courses to ensure that these would reflect the overall learning outcomes of the program.

[1] CDIO is an innovative educational concept originating from MIT (Massachusetts Institute of Technology) stressing engineering fundamentals in terms of process steps that engineers use when creating complex systems and products, see http://www.cdio.org/.

The next step was to modify, remove and add courses in the existing electronics specialization to meet the new learning outcomes. Just as described on the MIT web page, we changed the sequence and manner in which the courses were taught as well as their content. However, what took precedence over all other issues was the need to include a comprehensive design project. For CDIO-based learning, design projects and laboratories are key elements.

The final, and still ongoing, process is the process of aligning the teaching and learning activities with the assessment tasks of the individual courses in such a way that the *achieved* learning outcomes correspond to the *intended* learning outcomes.

In the next section the program planning and implementation process is discussed in more detail from the perspectives of CDIO and constructive alignment.

3. Engineering Skills and Learning Outcomes

The process of formulating intended learning outcomes has served as a major stepping stone in a university-wide process of replacing the traditional lecture-based teaching focus with a student-oriented learning perspective. This is a necessary step to take at any university if CDIO is to be successfully implemented. As far as the intended learning outcomes of the IESD program are concerned, we believe that they reflect the broad engineering skills required from an electronic system designer. The key goals of this program are to educate IESD graduates that are able to work as productive engineers in an industrial team designing and building electronics products, and qualified enough to undertake graduate studies leading to a doctorate in the field of electronic system design. In particular this means that our graduates should be

- proficient in the basic trade of *conceiving, designing, implementing, and verifying complex electronic systems*; a trade ranging from software for embedded electronic systems to analog transistor circuits
- proficient in the use of various computer-aided design tools used in industry
- aware of *the fundamental limitations of both the design tools and methodologies, and the technology platforms* that represent current best practice
- able to analyze new technical challenges and to generate technical advancements at either the electronic system level or at the device and circuit level
- able to carry out qualified industrial tasks within given constraints by applying *suitable methods*, also when in an industrial context technical aspects might be secondary to constraints associated with economy and environment
- able to critically, independently and creatively identify, formulate and solve complex problems in the field of integrated electronic system design
- able to critically and systematically integrate knowledge, to model, simulate, predict and evaluate behavior and events, also with limited or incomplete information.
- able to clearly and unambiguously communicate their conclusions, and the knowledge and rationale underpinning these conclusions

4. Program Structure and Curriculum

The next step in the process was to outline the overall structure of the Master's program. Once the overall program structure was determined, existing courses were modified or removed, and new courses were added to meet the new intended learning goals, see Table 1. In accordance with the CDIO concept it was decided already at an early stage of the planning process to include a first-year spring design project with the obvious goal to enhance student learning by doing and to develop their engineering skills by working in teams on realistic design project specifications. This decision came to have an important impact on most of the curriculum, since the fall courses in year 1 were planned to prepare the students with the skills and knowledge needed in the spring project.

The first year has a set of mandatory courses with a fall semester of introductory courses and a spring semester dominated by the design project. The second year has a fall semester with elective courses and a spring semester with a final individual Master's thesis project. This mandatory/ elective structure keeps the class together during the first year, while the second year is dominated by individual specializations.

<table>
<tr><th colspan="2">Fall semester, year 1</th><th colspan="2">Spring semester, year 1</th></tr>
<tr><th>1st quarter</th><th>2nd quarter</th><th>3rd quarter</th><th>4th quarter</th></tr>
<tr><td rowspan="3">Introduction to Electronic System Design</td><td>Computer Architecture</td><td colspan="2" rowspan="3">Electronic System Design Project</td></tr>
<tr><td>OR</td></tr>
<tr><td>Analog Integrated Circuit Design</td></tr>
<tr><td>Digital Integrated Circuit Design</td><td>Methods for Electronic System Design and Verification</td><td>Elective course, e.g. Data Conversion Techniques</td><td>Elective course, e.g. Hardware Description and Verification</td></tr>
<tr><th colspan="2">Fall semester, year 2</th><th colspan="2">Spring semester, year 2</th></tr>
<tr><td colspan="2">Topics in Electronic System Design</td><td colspan="2" rowspan="2">Master thesis project</td></tr>
<tr><td>Elective courses</td><td>Elective courses</td></tr>
</table>

Table 1. Outline of IESD program curriculum.

The program learning outcomes helped us identify courses that were vital to the program. For example, the first-year spring project was immediately assigned a dominating role in the curriculum: Skills like "*conceiving, designing, implementing, and verifying complex integrated electronic systems*" using "*suitable methods*" based on the awareness of "*the fundamental limitations of both the design tools and methodologies, and the technology platforms*" can only be acquired in a project, working as a member of a team. Obviously, this concept is at the very heart of the *Conceive, Design, Implement*, and *Operate* (CDIO) concept.

We were convinced that the project should not be just *any* course, but that it should be *the unifying course* of the program; a program with a wide technical scope[2] promoting engineering and project-management skills on top of a thorough theoretical training. A design and implementation project like ours supports active modes of hands-on learning including experimentation, social interaction, team building, and team activity. Already in place at Chalmers

[2] Embedded software, computer architecture, principles of EDA tools, digital circuit design, and analog circuit design.

were facilities for computer-aided design of integrated electronic systems, license agreements with Cadence, Mentor Graphics, and Synopsys for access to industrial software tools, access to silicon through multi-project chip fabrication via Europractice and CMP, and a laboratory with test equipment to operate the implemented systems.

Existing courses were modified so that their learning outcomes reflected the learning outcomes of the program, and two new courses were developed to fill up gaps in the curriculum: *Introduction to electronic system design* takes a top-down view to practical system design and trains the student in hardware description and verification in an FPGA context. *Methods for electronic system design and verification* focuses on principles behind EDA tools and trains students in ASIC synthesis and verification tools from register-transfer to layout level.

5. CONSTRUCTIVE ALIGNMENT

Constructive alignment represents a marriage between a constructivist understanding of the nature of learning, and an aligned design for outcome-based teaching education [6]. There are two parts to constructive alignment:

- Students construct meaning from what they do to learn.
- The teacher aligns the planned learning activities with the intended learning outcomes.

The Swedish translation of constructive alignment is *lärcentrerad undervisningsplanering*[3]. Real learning can only be managed by the students [7], and what we can do as teachers is to provide a learning environment that the student finds stimulating enough to spend the time and effort to meet the intended learning outcomes. Then we must also align the assessment methods and criteria for giving feedback on outcome fulfillment, to the suggested learning activities, see Fig. 1.

Figure 1. Aligning learning outcomes, learning and teaching activities and the assessment. From [7].

We have implemented constructive alignment at two different levels: First, courses have been aligned at the program level to provide for student progression. As already mentioned, first-year fall courses are aligned to prepare students for the spring project. Secondly, learning activities like lectures, home assignments, and laboratory exercises are aligned at the course level to support student progression towards achieving the intended learning outcomes at the end of the course. In the following, we will discuss in more detail constructive alignment at the course level by providing a summary of how it has been implemented in some of the courses in the program.

Introduction to Electronic System Design – The main intended learning outcome of this course is that the students should obtain a strong proficiency in design at the gate and register-transfer levels, using VHDL as hardware description language. VHDL proficiency is assessed by lab exercise reports submitted throughout the course; these are enough to earn a passing grade.

The IESD program has a wide technical scope and, thus, our students have very different backgrounds, ranging from analog circuits to computer systems. Making sure that all students have a certain core competence is important for succeeding courses, and this course ensures that all students are proficient in VHDL. The course also introduces a number of system design issues, offers a chance to work with FPGAs, and, via the VHDL exercises, revisits a selected number of signal processing applications. In addition, a lecture series gives a top-level overview of electronic system design. A written exam on the topics of this series is offered for students who desire higher grades.

Digital Integrated Circuit Design – The intended learning outcome of this course is twofold: After the course the student should be able to

- design basic combinatorial logic gates, clock trees, and adders and to optimize these for speed using paper and pen and some basic design and optimization principles
- validate these implementations by using advanced computer-assisted design (CAD) tools for schematic capture, circuit simulation, layout, design rule checking, layout vs. schematic etc.

A CAD design environment is set up using wide-spread industrial design tools. Lectures, home assignments and the hands-on lab series are aligned to take the students from simple concepts to more advanced implementations as the performance specifications are gradually tightened to meet stricter timing constraints.

Analog Integrated Circuit Design – The major intended learning outcome is to make students able to design a known circuit topology to a given specification using hand calculations for prediction and circuit simulations for verification as their tools.

The learning process is centered on five labs that use pre-lab hand calculations for prediction, the Cadence design suite in lab (for verification of the hand calculations), and post-lab reports for documentation and reflection. The class-room teaching is mainly viewed as a support for what is done in the lab and the topics covered are centered on those that are useful in this context. Two of the labs are "real" designs where the students design op amps to a given specification. Feedback from the teachers is given on the student designs before coming to the in-lab session so as to make the most of the time spent in the lab and increase the learning. The examination for passing the course requires that all prelabs and lab reports are satisfactorily carried through. An optional written exam is used only for assigning higher grades.

Methods for Electronic System Design and Verification – Here the emphasis of learning outcomes is on the *methodology* skills that are required for complex digital system design. For five (out of seven) course weeks, the students are active in a lab series that makes use of the Cadence Encounter system. The series is cohesive in the sense that the *same* digital block is considered throughout all labs; starting from block specification, via logic verification and timing- and power-driven implementation, ending with place and route. During the lab series there are number of hand ins, which forces the students to plan the

[3] *Learning-centered education planning*

work so that several critical deadlines are met, see Results and Discussion for more details.

The other important learning outcome relates to "softer" skills, in this case to critically and systematically assimilate new knowledge and to communicate this new understanding in a clear and unambiguous manner. To this end, the course includes a term paper assignment that allows the students to focus on a design and verification related topic.

Electronic System Design Project – The learning outcomes of the design project focus on the project approach and on the design process. Design, tool, and method skills taught in the fall semester are applied to solve a system design problem of modest complexity, going from a terse specification to a complete implementation. The system is chosen to offer design tasks spanning the range of sub-disciplines covered in the program (analog and digital circuit design; FPGA and monolithic implementation; processor-based and HDL-based behavior; etc). Thus, the course approximates a real-world design project, with extra emphasis on reflection on the process.

Students work in small teams which plan their work independently. Plans and results are documented in written reports and through oral presentations according to a prescribed project model. Project plans are continuously revised to handle inaccurate estimates of effort needed for certain tasks. Importantly, students are called upon to initially assess the collective team skills and to set aside resources to acquire additional skills by independent study. Progression in more general skills is provided by a "team roles" exercise carried out prior to a reshuffle of the team member responsibilities halfway through the project.

Examination is based mainly on the documents produced as part of the project work, and also on mandatory individual web log books kept by the students. The design task is the same for all teams and thus friendly competition is encouraged. The best design is a candidate for chip fabrication following a final design review.

In 2008 and 2009, the students designed the vital parts of a speed and distance measurement system; from refinement of the system specification to tape-out of a digital 130-nm ASIC. In 2010, the design task is a complete digital hearing aid in a 130-nm process.

6. RESULTS AND DISCUSSION

In this section we would like to share and discuss some of the experiences that we have gained in the process of planning, starting up, and running a new master´s program for three years. An attempt will also be made to quantify the results of our efforts.

In the Chalmers' IMPACT report [8] the Dean of education wrote: "In January 2006 the largest re-organisation of the education system in Chalmers' history was initiated. The goal was to start forty-four new Master's programmes in the autumn of 2007, and Chalmers would be one of the first universities in Europe to fully adopt the so-called Bologna structure. Existing final year programmes, international Master's programmes and about twenty new programmes would be integrated into the Chalmers' programme structure. This endeavour was monumental; however with fantastic support from Chalmers Foundation, the departments and many dedicated teachers; we can look back today, and realise that we have achieved a fantastic result with forty-nine well operating Master's programmes and many satisfied students. The latter was clearly confirmed in an evaluation which was conducted by the Quality Committee and IMPACT during spring 2009."

First of all, we are proud and happy to have developed a Master's program taught in English that we can offer to domestic and international students; a program that we consider up-to-date and well organized. This is in itself a major achievement starting from the *ad hoc* specialization offered in Swedish for domestic students only. The program has been running for three years now with 41, 46 and 28 participants, respectively. The fraction of international students has been 17%, 76%, and 61%. So far the program has been offered to all students free of charge, but from 2011 a tuition fee will be charged to all non-EU students.

A clear group identity: One good feeling that we have about our program, even though it is difficult to quantify, is that we now appear to have a group of students with a well-defined identity as a group. Before the start of the Master's program our impression was that of individual students taking one or many of our courses on an *ad hoc* basis.

One of the reasons for this improvement is that the provided learning activities have stimulated students to cooperate. For the mandatory lab courses we enforce an assignment of students into groups to provide for a well-balanced mixture of domestic and international students. Also, for the spring project, which is a major unifying undertaking in the program, we have tried to form as multi-national groups as possible. The effect of these efforts can also be seen in that working groups spontaneously formed by students for solving some assignment problems often are multinational.

The positive effect of a clear identity, associated to the profession of electronic system design, lingers throughout the program. In contrast to the time period before the Master's programs, many of our students today are integrated in the research work of the groups. To reinforce this trend, a new elective course *Topics in Electronic System Design* was introduced in the fall of 2009. Here a limited number of students (15 at most) can participate in smaller research-oriented projects, as a precursor to research-oriented Master thesis work and, later, PhD studies. In the first installment of the Topics course, twelve students participated. The projects carried out were mainly in one of three different categories; seven students made evaluations of new EDA tools and/or new technology platforms, three students made in-depth studies of their favorite topics, and two students contributed to on-going research projects. The latter cases both led to conference paper submissions.

What about improved examination results? One important question that has been raised is whether the course examination rates have improved. Has student performance improved in the new learning environment, and if so, by how much? For many reasons this question is a bit difficult to answer. One reason for this is that many courses were so heavily revised that examination results are not comparable; another reason is that some of the courses are totally new. One of the courses where comparisons are most easy to make is the Digital integrated circuit design course, a course that essentially follows the same main outline as before the Master's program was started. The examination results from this course are shown in Fig. 2.

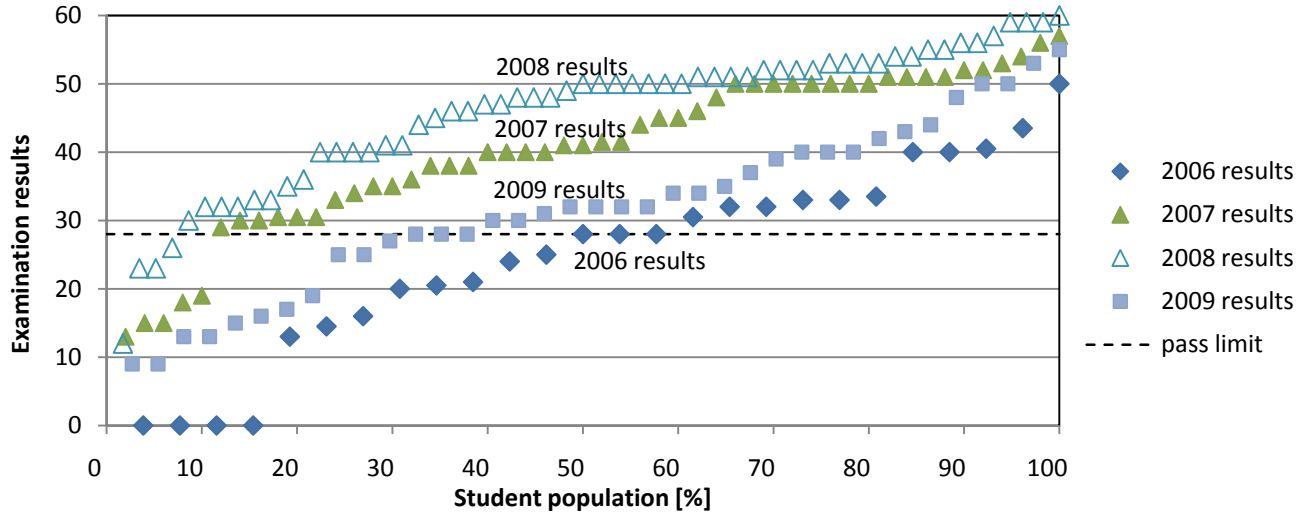

Figure 2. Examination results for the Digital integrated circuit design course 2006-2009.

In this diagram each marker represents the result of one student in the final written examination. The 2006 results are from the academic year before the course revision in connection to the start of the international Master's program. The cumulative diagram shows that 46% of the students (12 out of 26 students) failed in reaching the written examination pass limit.

The results from 2007 and 2008 indicate a considerable improvement as a result of introducing the new learning environment influenced by CDIO and by constructive alignment. During these two years only five and four Master's students, respectively, failed in the written examinations corresponding to as low as seven to ten per cent failure rates. We believe this is a result of the introduction of a set of home assignments that were well aligned to the lecture schedule and to the laboratory assignments. Hence, the students could constructively take advantage of the provided learning activities to ensure a good result in the written examination as they were already well aware of the intended learning outcomes.

Unfortunately, the 2009 results indicate a considerable set-back as the failure rate suddenly increased to almost 30% (11 out of 37 students). We do not know for sure whether this is a result of a more difficult written test or a result of a parallel course consuming too much student effort. Also, there are some indications that students paid less attention to the home assignments in 2009 since they might have heard from second-year students that these were not graded. Also, they were essentially the same assignments as in 2007 and 2008. Renewal and constant change appears to be one key to improved student performance.

Other courses are either new or so heavily revised that direct comparisons in examination rates cannot be made between the situations before and after the start of the Master's program. The discussion should rather focus on the improvement in the learning outcomes that we believe that we achieve. The main point is not the increase in examination rates per se, but rather that we have a much better control of the learning outcomes that we achieve. Also, due to the much better defined intended learning outcomes and the improved assessment, we as teachers have a much better picture of the differences between the achieved and the intended learning outcomes. Therefore, today we have a rather good idea of how we could work for continuous improvements.

As an example of new approaches to assessment, *Methods for electronic system design and verification* exposes the students to an applied design methodology. The student's progress in learning methodology is hard to assess by, for example, using traditional written examination, so we have been trying a different approach, which impacts both grading and feedback. The core lab series contain three deadlines pertaining to specification, implementation and verification, and for each deadline the students are required to hand in documents and(or register-transfer level (RTL) code. To make it possible for the students themselves to do an assessment of whether they fulfill the learning objectives or not, the lab memo details the intended learning outcomes for each of the four labs. The teachers assess several parts of the laboratory work, including the initial specification of the digital block and the verification testbench, the actual RTL code and the final report.

Training students in methodology by using practical projects and labs makes much of the teaching student-team oriented. This is both good and bad. Practicing team work is important as the skills acquired while working in a team are applicable to the engineering role. However, it is hard for the teachers to assess individual efforts. In the first installments of the course, the ambition was to assess actual work in the lab halls to gather information on the work of the each student. For several reasons, this proved to be a challenge.

Beside the problem of finding a uniform way to assess students when several teaching assistants are involved, such a continuous and informal assessment makes the student feel they have limited time for their own exploration. For example, a student may think that asking a question, and thus acknowledging missing knowledge, may reflect badly on the grade. The collected experience from dealing with methodology training is that there must be several assessments during the course, however, the rules and timing of assessment must be clear, and the exploration time in between assessment must be generous enough to allow students to reflect and explore "what if" questions.

The spring design project replaced a set of incoherent small design projects. New intended learning outcomes were formulated, focusing not only on technical aspects but also on aspects of working as a member in a project team. We have opted to use a common project model with a small number of mandatory deliverables and presentations. The first deliverable is the initial time plan for the complete project. In most cases, this first time plan will be unrealistic; teachers will however point out only mistakes deemed potentially fatal. Students are encouraged to regularly adjust the time plan and to redistribute the work within the group as necessary.

What about student workload? In the design project course, students are required to keep individual log books of their efforts, detailing the number of hours spent on different tasks. Stopping short of time sheets, the log books still facilitate periodic follow-up of the time plan devised by the students at project start; additionally, it lets teaching staff assess student workload. As the log books were not used previously, they provide no definite data of how workload has changed; still, we believe the average level of effort spent has increased somewhat and that the minimum level has increased significantly.

What about staff work load? Staff work load has definitely increased. Other shortcomings notwithstanding, the traditional course organization with lectures and a written exam is quite efficient in terms of teacher workload. Thus, our improved achieved learning outcomes and examination results have come at a cost. It is difficult to quantify the load increase; but quality individual feedback for home works and for pre- and post-lab reports would be difficult to provide with a class larger than the present ones, whereas "traditional" courses are routinely taught to classes of 100 students and more.

What about e-learning? Practical computer-based work forms a large part of most of our courses. Our use of industry-standard tools means that many tasks can be carried out at a distance thanks to the network transparency of the X Window System [9]. Still, most laboratory moments require presence in the lab hall for examination: we find that especially the weaker students benefit enormously from the presence of a tutor who will not let them pass a certain checkpoint until they are ready for it. In addition, Chalmers uses the Ping Pong Learning Management System [10], which provides tools for web-based collaboration, group submissions, polls, etc. Our use of these tools can undoubtedly still be improved.

7. CONCLUSION

By using constructive alignment in a CDIO environment, a Master's program has been designed where the suggested learning activities are aligned with the intended learning outcomes and where assessment is aligned for checking whether the achieved learning outcomes coincide with the intended. An integrated learning environment has been created where students are stimulated to progress to take on more and more challenging design tasks, while in this process acquiring the skills necessary to become productive engineers. A variety of examination methods are used to assess different skills. In conclusion, building a Master's program and creating its learning environment is an ongoing process constantly subject to improvement.

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Initiation of a course package based on the Bologna process with support of the department of educational development

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Abstract— **In this contribution, we present a teaching-learning-concept which enriches the education in the department of electrical engineering and information technology by the following three points: the course works with an intensive integration and matching of the elements lecture, exercise course and laboratory; new teaching and learning forms are used; and it is complemented by an intensive assistance by the department of educational development. The aim of this concept is to establish a more student centered teaching and learning in order to help the students to develop their skills and knowledge.**

Bologna Process; course package; Information Technology; teaching techniques; educational assistance

I. INTRODUCTION

Based on the Bologna process, the Institute for Information Processing Technology (ITIV) decided to request for counseling by the educational development department of the Karlsruhe Institute of Technology (KIT - back then: Universität Karlsruhe (TH)) - in order to develop a new bachelor course of studies. The aim was not to just rename the intermediate diploma as bachelor degree, but to construct a course of studies with intertwining and up-building parts and arrangements.

The direct result of this counseling was the decision not to work on the meso level of the whole institute, but to choose one lecture as an exemplary arrangement on the micro level. In this context, the course 'Information Technology' - abbreviated IT - was chosen. This course consists of a lecture with the basic theories, an exercise course to work with these theories, and a project based laboratory where the students have to train their expertise. It is aimed at the bachelor students of the second semester and has no prerequisites. The working team all around IT comprises a professor holding lectures, two supervisors holding exercise sessions and supervising student tutors (20 students), who are supervising the teamwork during the laboratory and assisting the students during the preparatory learning sessions in computer pools. Detailed information about the IT course will be depicted in the following section.

II. PACKAGE INFORMATION TECHNOLOGY

A. *Structure of the course IT*

The IT package consists of three parts: lecture, exercise course and a project-based laboratory. All parts are strongly intertwined with each other in terms of contents and time as well [1].

The lecture counts three ECTS and thus goes over fourteen teaching sessions spread over the whole semester. The main teaching methods, which are adopted, are lecturing with the help of power point slides due to the number of the students (around 300 students) attending the course and the big lecture-hall. Nevertheless, other media like blackboard and overhead projector are occasionally used to practically show how theoretical content really works.

The lecture deals with different topics like algorithms, computer architecture and programming languages and is a kind of insight in the world of informatics for the electrical engineering students. It also gives a detailed introduction to the project of the laboratory, which helps the students to better understand the underlying theory. Due to the fact that the lecture is strongly coupled with the exercise and laboratory sessions in terms of contents and time as well, the planning of the lecture was done, unlike usual, according to some chronological and content related constraints. This came up after planning the laboratory in a first step and the exercise in a second step. This was very challenging and a tight plan was conceived. This scheduling was also adjusted during the semester. This flexibility in the course scheduling allows, unlike in traditional diploma courses, to adjust the content according to the development of the students' skills and needs over the semester.

The exercise course counts 1.5 ECTS and is held in a big lecture hall and runs over the whole semester as well. In the beginning, there is an introduction to the programming language C++. The content is coordinated with tutorials and the chapters in an additional C++ compendium, which explains the discussed C++ material with more details and further

examples. In the second part of the semester, more complex tasks are solved, which is a good preparation for the project to be implemented in the laboratory.

During the exercise, different teaching methods are used. The main medium for explanation, graphical visualization and showing practical examples are power point-slides, because of the big lecture-hall and the large number of students. Nevertheless, other methods are used according to the situation. Some questions are solved step by step with the assistance of the students using the overhead projector or the blackboard to better explain complex solutions. Programming tasks are solved in an integrated development environment via live demonstrations. This offers better insight in practical programming since the students use the same IDE later during their project. To illustrate flows in programs, especially concerning algorithms, graphical simulations are shown.

In order to reach as many individual learning styles and paces as possible, various media is used during lecture and exercise. In this way, several learner types can be reached, mainly the aural and the visual types [2]. By using active learning techniques [2],[3] like "Think-Pair-Share", a better and deeper understanding and reflection of the course material is achieved for those who prefer to learn by doing exercises themselves and by explaining to others. Such techniques keep a higher attention level of the students during the teaching session (see Figure 1) and enhance critical thinking about the contents by the students. Also, a variation of the social forms enhances the learning progress, because on the one hand there is room for those who prefer to learn alone, on the other hand there are also time slots where group learners are supported. This strategy of adopting various teaching techniques, which address different learning styles, represents an innovation in course conception and additionally enhances student centered teaching.

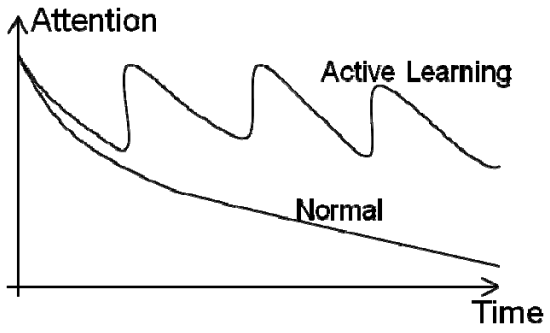

Figure 1. Influence of active learning techniques on the attention level in comparison to the classical teaching methods [4],[5],[6]

The practical laboratory counts three ECTS and includes thus seven sessions of three hours in a computer pool. In this lab, a small tool for timing analysis of synchronous logic systems is to be programmed in C++, thoroughly tested and documented in small teams of four to five students. For that purpose, the students receive handouts from the beginning of the semester which contain a detailed specification of the tool to be implemented. In addition, a project plan is suggested. During the lab sessions, three to four teams are supervised and supported by a student tutor.

The seven sessions of the laboratory take place in the second half of the semester out of two reasons. First, is needs some time until the content about the programming languages in the lecture and the concrete teaching of C++ in the exercises are finished. Second, an introductory phase in the first six weeks of the semester before the official start of the laboratory is offered. In that time, students, especially those with minimal or none previous knowledge in the world of programming, have the chance to learn the basics of C++ step by step with the help of the provided compendium and the recommended text books. Additionally student tutors offer their help in the computer pools at predefined time slots. During the offered tutorial sessions, the complexity factor rises to build up well-founded knowledge and have an easy start with the project, where the students' competences are further enhanced. Only then all students can accelerate their learning process of the programming language and have the chance to successfully complete the main project.

The following figure shows the time scheduling of the different parts of the course package over the whole semester.

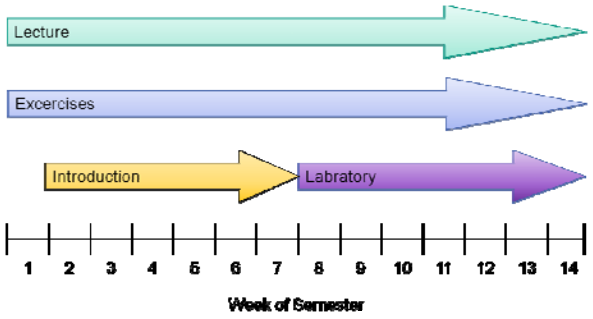

Figure 2. Time scheduling of the IT course package

The whole course material is published using a central electronic teaching platform, which is based on the open source project "Moodle" [7]. Besides the material, the platform also offers a forum which the students can use to discuss certain topics or ask questions. The latter are answered by other students, the student tutors or the supervisors. They can even be used by the supervisors while planning the next exercise sessions, since the supervisors can reproduce what the students understood and where they need more help and information. Besides, special forum areas on the central teaching platform can be used by students of the same group to discuss arising problems in the practical laboratory.

In the end of the semester, a two hours written examination is used to check the student competences, skills and knowledge concerning lecture, exercise course and laboratory. Especially skills concerning problem solving, algorithms and programming are tested. Beforehand, the project based

laboratory has to be successfully completed. For that, the students need to systematically solve a problem in groups with rules of project management (planning, tasks distribution, coordination, cooperation, documentation, etc.). At the end of the project work, the students have to present their results to their supervising student tutor and need to submit their code and documentation on the teaching platform.

B. Monitoring by educational development

The aim of the arrangement of lecture, exercise courses and – especially – the project based laboratory is not only to train the student's expertise, but also to advance their soft skills regarding e.g. competences in team work and project management. To achieve this, it is necessary that the teachers and the student tutors are able to teach, to live and to reflect these skills and competences.

Therefore, a continuing process of further education and educational development accompanies the parts of the package. This is occurring on several levels: The supervisors of the exercise courses are attending courses of the educational development and aim for reaching a certificate of the state ("Baden-Württemberg-Zertifikat für Hochschuldidaktik"). The „Baden-Württemberg-Zertifikat" is awarded by the centre for educational development (HDZ) of the universities of the state of Baden-Württemberg in Germany. It attests the successful completion of a program in higher education pedagogy. The objective of the HDZ is to improve the quality of academic teaching at all universities in Baden-Württemberg.

The HDZ also conducts tailored projects designed to improve teaching conditions directly at the institutes.

To achieve the certificate, the participants have to acquire three modules: in Module I, they learn about the basics of teaching and learning in higher education with attending two workshops (two days each), a couple of cooperative counseling sessions, a cooperative in-class observation and supervision and a written pedagogical reflection and documentation.

In Module II, the participants are requested to deepen their knowledge and skills by attending workshops in four different topics relevant for teaching in a university context. The topics can be chosen out of seven subject areas such as 'teaching and learning in alternative frames', 'new forms of teaching and learning', 'planning of courses', 'accomplishing courses', 'evaluating courses', 'counseling students' and 'conception of examinations'. The HDZ provides a large range of different workshops for each topic and subject area.

To successfully achieve the third Module, the participants work on an individual project which corresponds to their individual teaching situation. During the project, they work on optimizing their teaching and improving the learning effects of the students. Thereby they are assisted and counseled by the HDZ. The project has to be reflected and documented in written form, as well as the once more the whole own learning process.

Module I	**Module II**	**Module III**
60 academic units[1] The basics of teaching in higher education	60 academic units[1] Specialization in four of seven topics relating to higher education	80 academic units[1] Selection of individual topics

Figure 3. Curriculum of the „Baden-Württemberg-Zertifikat"

The development of the IT package was based on a project with the aim of assisting ITIV in the development of a bachelor course of studies. It was chosen as an exemplary arrangement for the institute. The exercise supervisors prepared themselves for their various duties and responsibilities in the exercise course and the laboratory by attending the certificate program, choosing courses which fit the requirements of the IT package (e.g. 'Basics of teaching and learning', 'Developing practical trainings', 'Active learning with Large Groups of Students', 'Performance Training' etc.) and regular counseling by members of the HDZ. Due to the requirements of the certificate, the development process of the supervisors as well as of the IT package is therefore well reflected and documented with a didactic perspective.

To further enhance the student centered learning, tutorials are offered during the project based laboratory. For that reason, several student tutors have to be employed. These undertake as well a special program: "Educational development for student teachers - basic level". It is oriented on the above described certificate-program, but aligned to the needs of student tutors and their work. In this program, they receive basics of didactics and specific topics relevant for their work on the laboratory project, e.g. team processes, basics on project management etc. The attendance of the program is obligatory. The students have to attend four days of workshops; they additionally counsel each other on teaching concerns and interchange feedback on how they teach. At the end of the program, they have to write a reflection about this process. The accomplished training can even be accredited as a key competences course with three ECTS in the Bachelor degree.

III. RESULTS

The feedback by the students on the new organization of the IT package has been very positive so far. In the annual evaluations, rated by the students, the main internal quality guidelines concerning structure, clearness, mentoring and the overall mark have been rated positively. Very positive elements in the laboratory are project-design, teamwork and the practical problem, which has to be solved. Concerning the exercise, the different methods and the interactive learning breaks are seen positively.

[1] One academic unit = 45 minutes

The package ran the second time in 2009. In comparison with the pilot project in 2008, a significant improvement could be seen as well. In fact, a higher motivation, enthusiasm and engagement from the students during the course could be observed. This resulted in a higher success rate in the exams.

Most student tutors of the summer semester 2009 felt well prepared for their responsibilities in the project based laboratory. They were e.g. able to structure their tutorials, and started to reflect on their behavior and the consequences out of it. Other student tutors were especially interested in the group processes and reflected this: Some found the part about group processes very interesting because theses processes are really good to observe if one pays attention to it. With the knowledge gained during the program, one has valuable indications for dealing with groups; usually one would act the wrong way by intuition. Other student tutors appreciated the possibility to share opinions, found the mutual help between the tutors a great enrichment and came to the outcome that, besides all what they have learned in the tutorials, their own private learning was also increased efficiently.

IV. OUTLOOK

It is planned to further optimize the package and to relieve all participants from the pressure of the strong intertwining – which leads to negative consequences by rather small changes (e.g. after having to cancel a lecture session). To overcome this lack of flexibility and avoid a potential disequilibrium between the different components of the course, the practical laboratory is being shifted to the third semester, meaning one semester after the lecture and the related exercises. This way, the coupling between the lecture and the exercises offers more flexibility and the students have more time to learn the new programming language.

The development and enhancement of the course IT over the time was an exemplary process for the institute ITIV. Nevertheless, the competences and skills of the different parties all around the IT package (the professor, the supervisors, the student tutors and the students) should be further enhanced.

Based on the experiences of the planning and the realization, it is now time to move from this micro level to the meso level of the institute with its various teaching arrangements. The aim for 2010 is to use the reflected experiences and establish a revised concept for the lectures in the master course of studies.

Then it might be possible to step even further and move this way of “packing packages” to the macro level of the faculty.

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The Dangers of simple usage of Microwave Software

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Introduction:

We have seen many dissertations about the implementation of microwave circuits, where a student has built an oscillator or another circuit, measured it, ran a simulation, obtained different answers and then tried to explain the reasons. Actually there are two main sources of inaccuracy, one being the measurements and the other the simulation. In the case of an oscillator the important parameters are output power, harmonic content and, most important, phase noise.

These three critical parameters are determined under large-signal conditions. Using CAD introduces automatically two weaknesses. The device used for the application needs to be characterized, many times by curve fitting, and needs to match a model of the simulator which itself is mostly an analytical model rather than physics based.

In a simple oscillator case we would like to show that using a rigorous mathematical model the educational benefit outweighs the simplicity of a CAD analysis and subsequent optimization.

The two test cases are a Driscoll oscillator with the crystal resonator in the emitter, which was taken from the literature and the design could have never worked because of errors in the publication data. A CAD tool would not have found the problem but an understanding of the operation allows to find the correction. The next case is the Colpitts oscillator, which offers many choices of design but only the large signal approach will work. This is more analytical rather than trial and error.

This effort is based on using Bessel functions and a calculation in the time and frequency domain. The added benefit is that all physics-based noise models will be used and therefore the student gains much more insight in all the concurrencies. Once the basic set of equations is derived, the first derivative of the feedback components vs. phase noise allows exact optimization.

This type of circuit analysis, which can be applied to many other designs such as amplifiers and mixers, give the best insight into the functionality of circuits in the time domain where we discover such new things like time average loaded Q and noisy feedback or noise-contributing support circuits.

In this paper we will use a simple but in the end highly non-linear circuit, where we will demonstrate the accuracy of our approach using simulations, sets of analytical time domain equations and of course accurate measurements using test equipment from two established manufacturers, Agilent and R&S. Each step of this design provides much better insight in the functionality than the standard teaching approach of this topic resorting to too much CAD. In the following we will show three cases, which will highlight the problems.

Case study of a: Twin T-oscillator using an Infineon BFR93aw, microwave transistor, showing that the linear and the non-linear analysis for the resonant frequency gives a significant different results [1], a analysis of a Driscoll oscillator where the Cad prediction is far too optimistic because it does not have good data for the flicker corner frequency [not provided by the manufacturer] and flicker noise contribution of the crystal and finally the third case is the mathematical analysis of the Colpitts oscillator using the large signal parameter and the Bessel function to get a very close result to both the measured and the CAD simulation [2].

Case 1:

In general and until recently transistor simulations used linear analysis, which turns out to give fairly inaccurate results. To show the base line, here is the example using a RC example. It is based on [1] and operates at 1.6MHz. Figure 1 shows the actual circuit diagram.

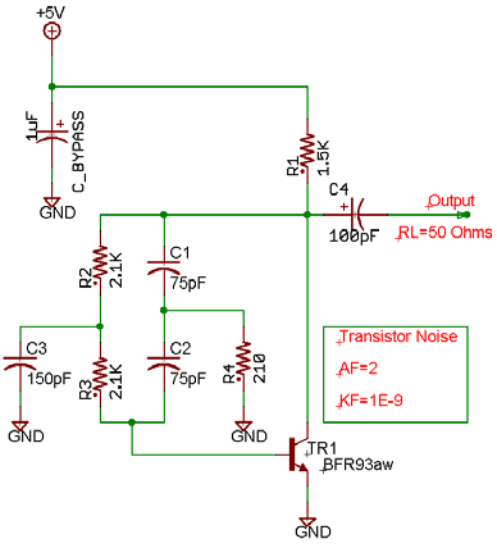


Figure 1: the actual circuit diagrams for 1.6MHz

The literature is full of RC oscillators but very little information is available on its phase noise and the difference between the linear and the non-linear operation. So we analyzed [Figure 1] this oscillator and scaled it to about 1MHz and using a linear simulation determined the following resonance frequency.

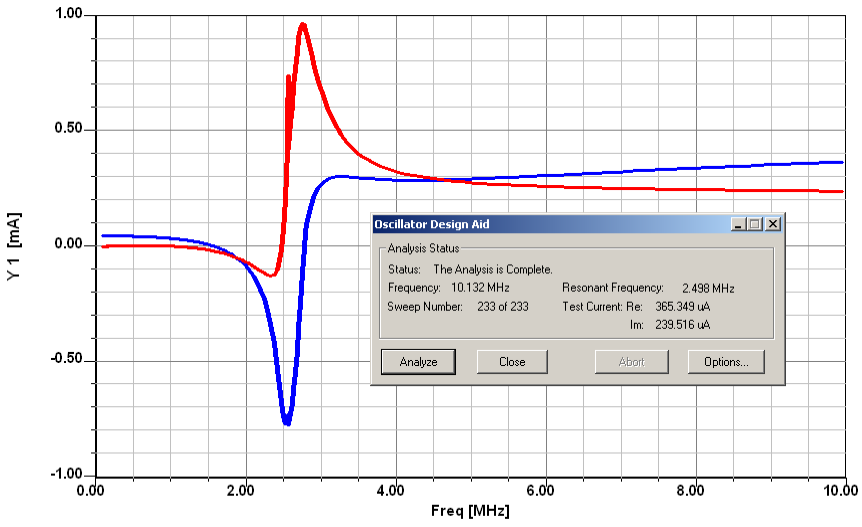


Figure 2: Linear simulation result of the schematic in figure 1.

The linear case indicates the resonance frequency around 2.5GHz. The Y-axis is the RF current in milliamps at the junction between the two resistors, 2.1Kohms and the 150pF capacitors to the ground. This assumes a total linear system and the purpose of this example is to show that the linear simulator can mislead you totally. After this result we used the Ansoft serenade harmonic

balance simulator 8.7V and a validated model for the siemens transistor BFR93aw. The initial DC analysis provides the operating point.

Bias Point Values

Voltage	Current
Vp() = -0.232686 uV	Ip() = 0 A
Vbe(_lib1) = 0.734765 V	Ib(_lib1) = 36.3168 uA
Vce(_lib1) = 0.862989 V	Ic(_lib1) = 2.70409 mA

The results are 2.7mA for 0.86V V_{ce}. The output waveform is slightly distorted and shown in figure 3. Figure 4 shows the harmonic contents. The output frequency as seen in figure 4 is different from the linear prediction and is 1.6MHz. The harmonic suppression is about 14dB. The loaded output terminated into 50 ohms is –19dBm.

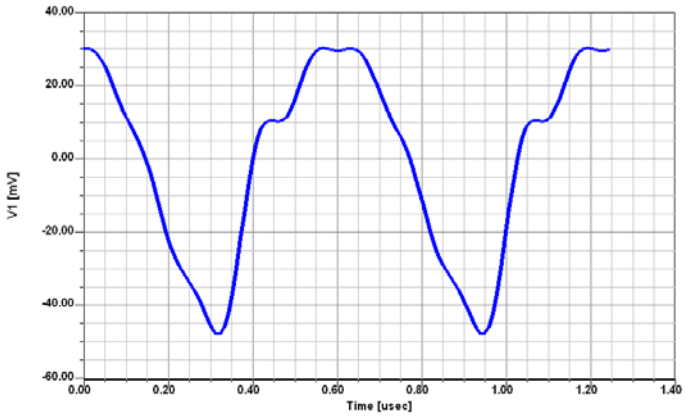


Figure 3: Simulated output waveform.

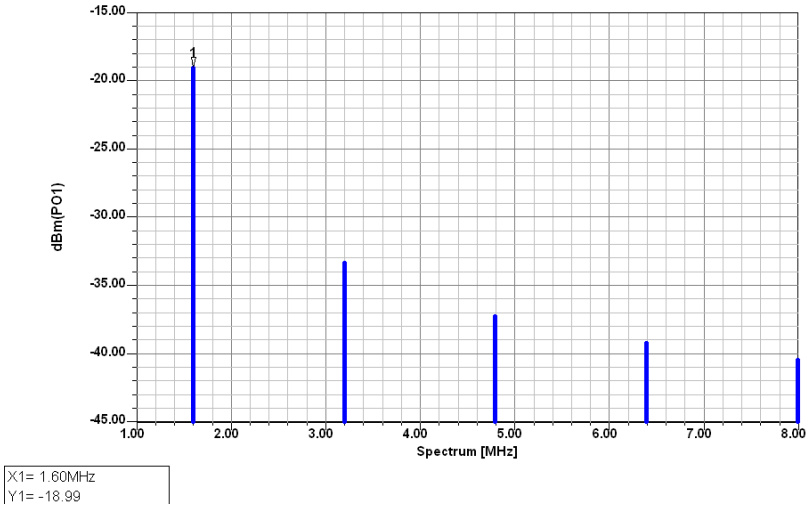


Figure 4: Simulated output power for the schematic in figure 1

We must keep in mind that this is a RC oscillator consisting of a notch filter and does not have a Q in the traditional sense. These types of oscillators typically do not operate into 50 ohms but into some CMOS gates, which are voltage and not power driven. IF we assume that the practical load is 9Kohms then the voltage swing at the output increase to ±900mV, this is 1.8Vp-p at the end to drive the gate.

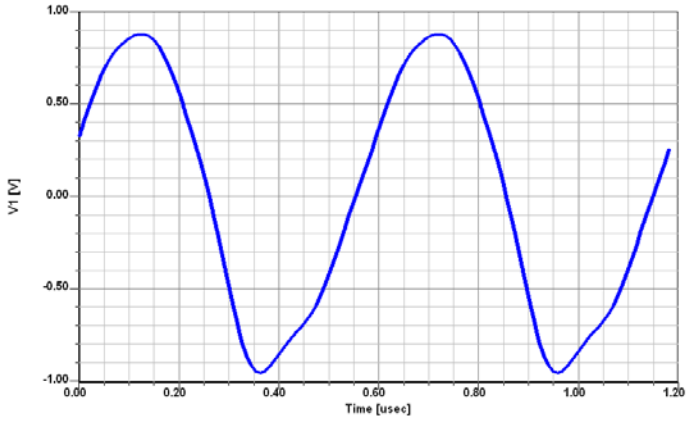


Figure 5: Simulated output waveform with a high impedance termination of 9Kohms.

Now to our surprise the resonant frequency is 1.679MHz a huge difference from the linear approximation. So far we have shown output power harmonic contents and now how about the phase noise.

This information is rarely found in the literature, but here it is shown in figure 6.

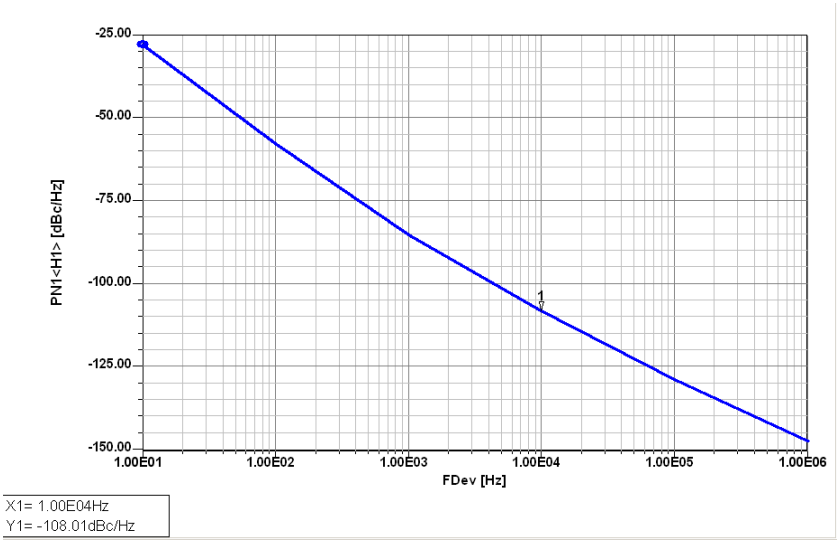


Figure 6: Predicted phase noise in dBc/Hz offset from the carrier frequency ranging from 10Hz to 1MHz of this RC oscillator.

By itself it is not overwhelming but if it is used as a part of the synthesizer loop divided down by the 100 a 40dB improvement, then it looks much better. The 10 KHz offset would be at –148dBc/Hz. It is mixed into a synthesizer it is a good performer.

Again why is this barely found in literature?

1: Most of the CAD tools cannot analyze this accurately. An important test is to validate the existence of the flicker corner frequency. In our case it is at 1 kHz. This is typical for a microwave transistor at this DC current, an audio type transistor or a FET to show much smaller number.

2: Majority of phase noise setups does not operate below 10MHz; Measurements of 5MHz are typically done using a diode multiplier at higher frequency.

Case 2:

One of the promising oscillator is the circuit discover by Driscoll; Its schematic shown in the figure 7.

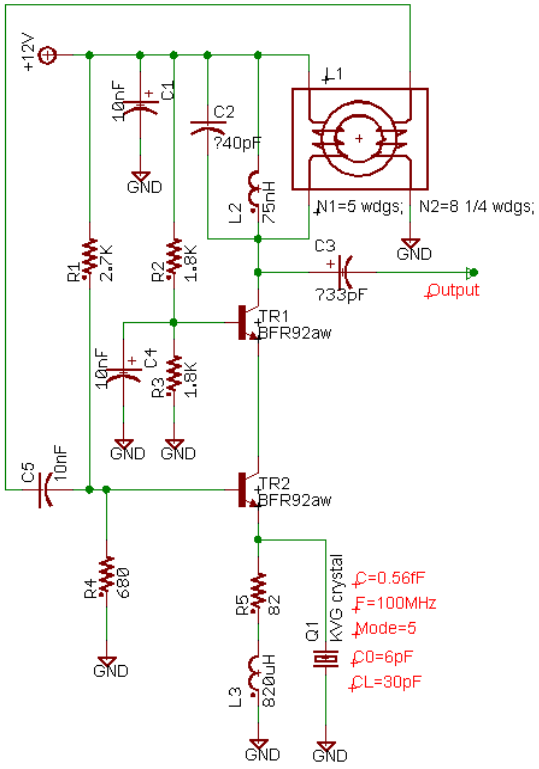


Figure 7: 100MHz crystal oscillator using the Driscoll Schematic.

Essentially it is a cascode amplifier where the output from the second transistor is inverted by 180 degrees and drives the lower transistor. At its resonance frequency the Crystal, grounds the emitter via a small resistor (C of the crystal) and the oscillations starts.

The measured results first. They were obtained using the FSUP.

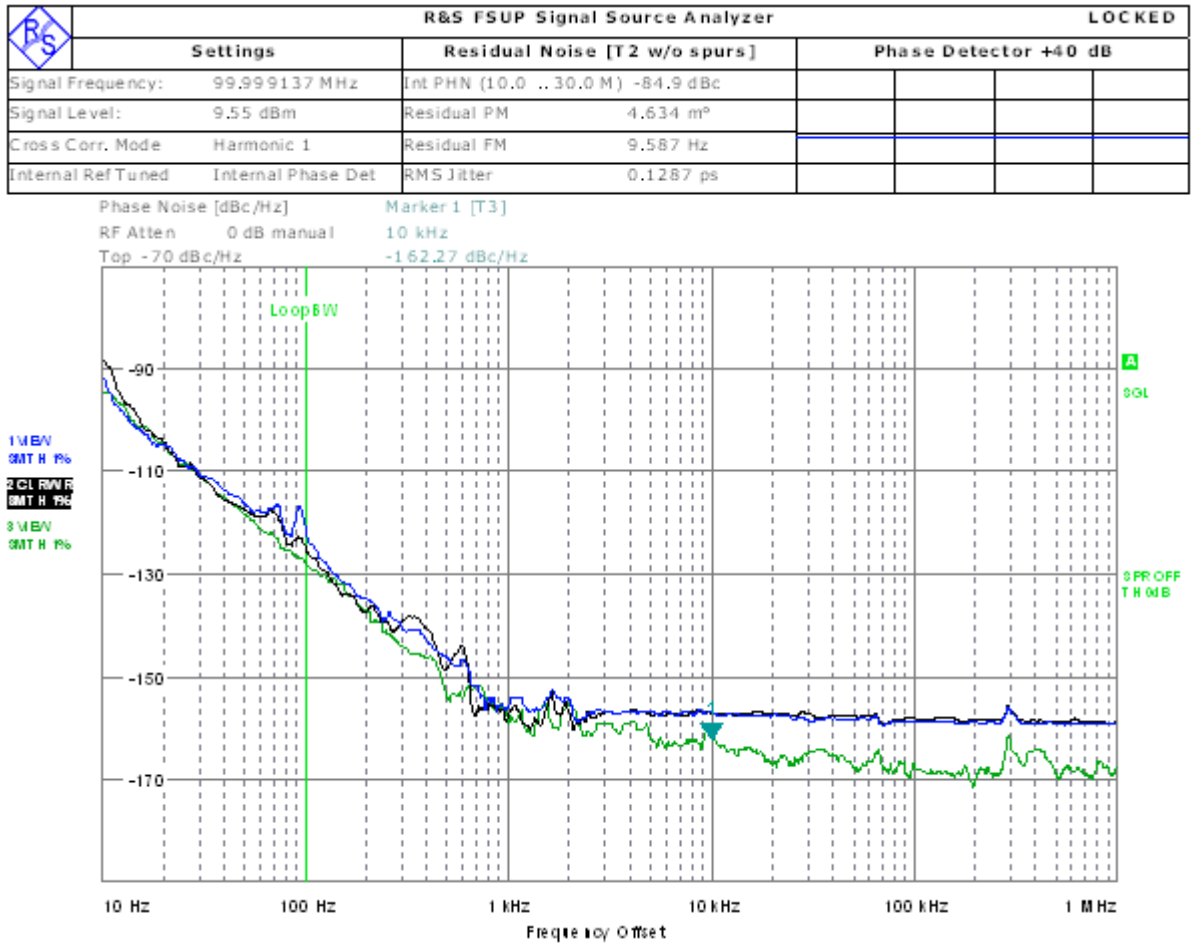


Figure 8: measured result for the 100MHz Crystal oscillator.

The difference between the blue and the green curve is the measurement taken without the buffer (green) and with the buffer amplifier, BGA614, dual Darlington amplifiers (blue curve). We really would like to point out that choice of right buffers is extra ordinarily important and the CAD tools may not give the right answer.

Now let's do the simulation.

The linear simulation tells us 99.998MHz. Because this is a very high Q device and it also maintains its high Q we can expect the circuit simulator to give a similar answer in the nonlinear mode.

The transistor cascode is operated at 17.4mA. The lower transistor TR2, model BFR92aw, has a V_{ce} of 3.46V and the upper transistor TR1 same model has the V_{ce} of 6.94V. The output power is 9.58dBm with the predicted harmonic suppression of 22 dB. The output waveform is shown in the figure 10 and it shows on the upper right corner the harmonic contents.

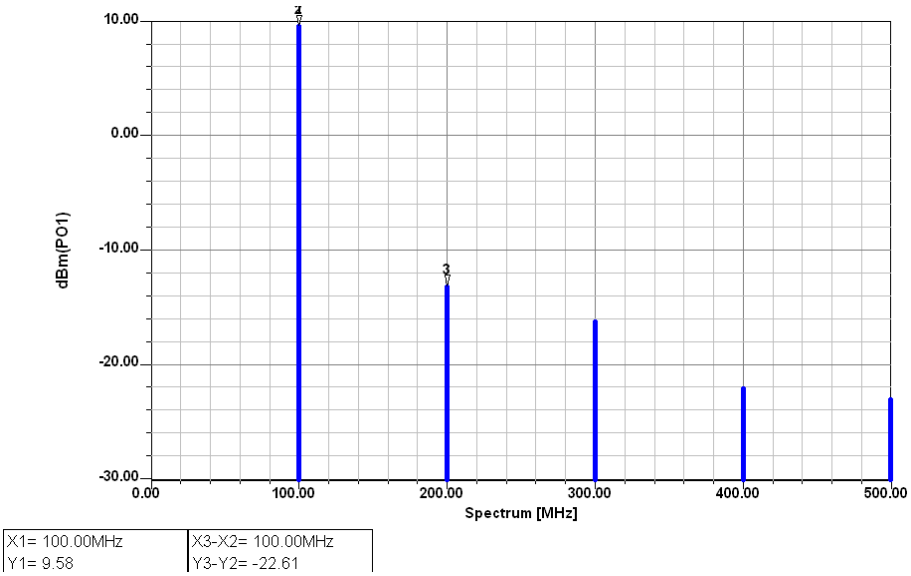


Figure 9 Predicted harmonic contents of the schematic in figure 7.

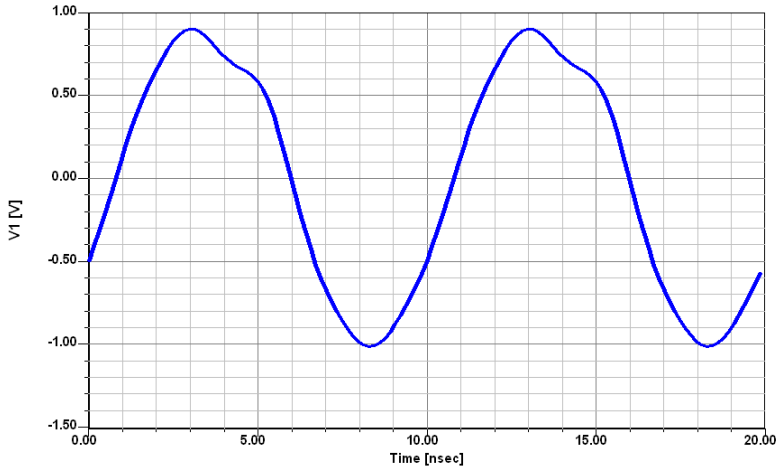


Figure 10: The estimated output waveform for 100MHz crystal oscillator

Now we are curious what the phase noise simulation tells us compared to the measured results.

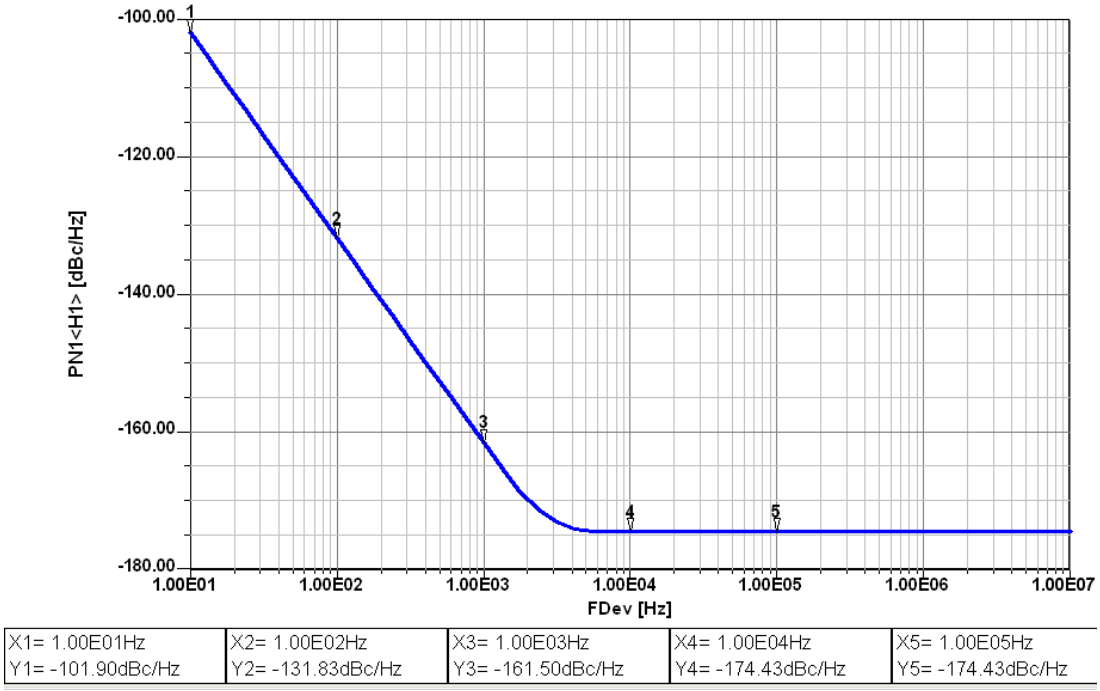


Figure 11: Predicted phase of the 100MHz crystal oscillator from Driscoll.

As we had already anticipated the CAD solution is somewhat erroneous. Since this is a crystal oscillator or a frequency reference it cannot be phase locked easily and there is no easy way to improve it. Here are the results and their deviations.

Frequency offset	10Hz	100Hz	1KHz	10KHz	100Khz
Simulation result	-102dBc	-132dBc	-161.5dBc	-174dBc	-174dBc
Measurement result	-90dBc	-125dBc	-155dBc	-162dBc	-170dBc

Having spent $50,000 for the simulator and $80,000 for the test equipment the simulator is too optimistic. The reason for this lays in the uncertainty of the flicker frequency which none of the manufacturers are willing to give guarantee for, and a type of flicker noise that the crystal has itself. The standard crystal models are not sufficiently accurate for the good modeling.

In case three we like to develop an analytic formula, which greatly eliminates the CAD cost, and its problems and yet gives results were calculations, not simulation agrees with the measurement.

Case 3:

A colpitts oscillator is an attractive oscillator, as it uses the capacitive divider and is essentially an emitter follower, which results in phase shift in transistor much less than a grounded emitter circuit has. For further details on Colpitts oscillator see reference [2].

The colpitts oscillator schematic is as shown below:

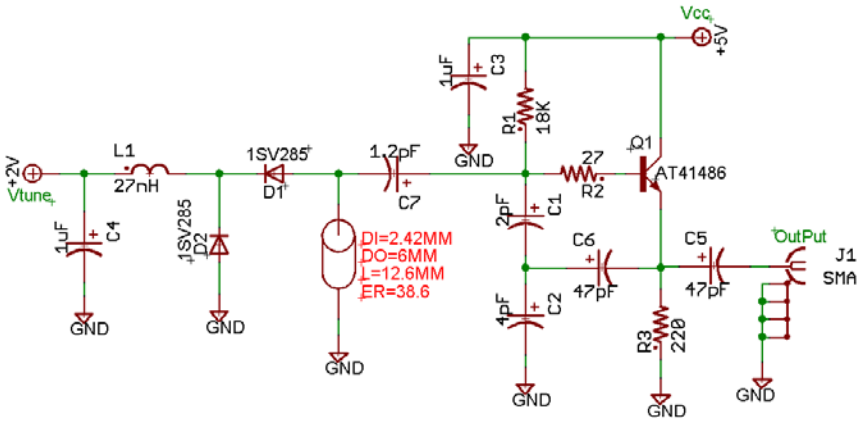


Figure 12: Colpitts oscillator design for 800-900MHz

What we is a voltage controlled oscillator with Toshiba's 1Sv285 varactor. This fulfills the requirement the author notes for the tuning diodes, page (314) [1]. The simulated results in the book strongly disagree with the simulation [1, page 315 figure 7.19]

Frequency offset	100Hz	1KHz	10KHz	100Khz	1Mhz
Simulation result with diode	-22dBc	-52dBc	-82dBc	-111dBc	-136dBc
Simulation result without diode	-51.5dBc	-81dBc	-110dBc	-137dBc	-158dBc

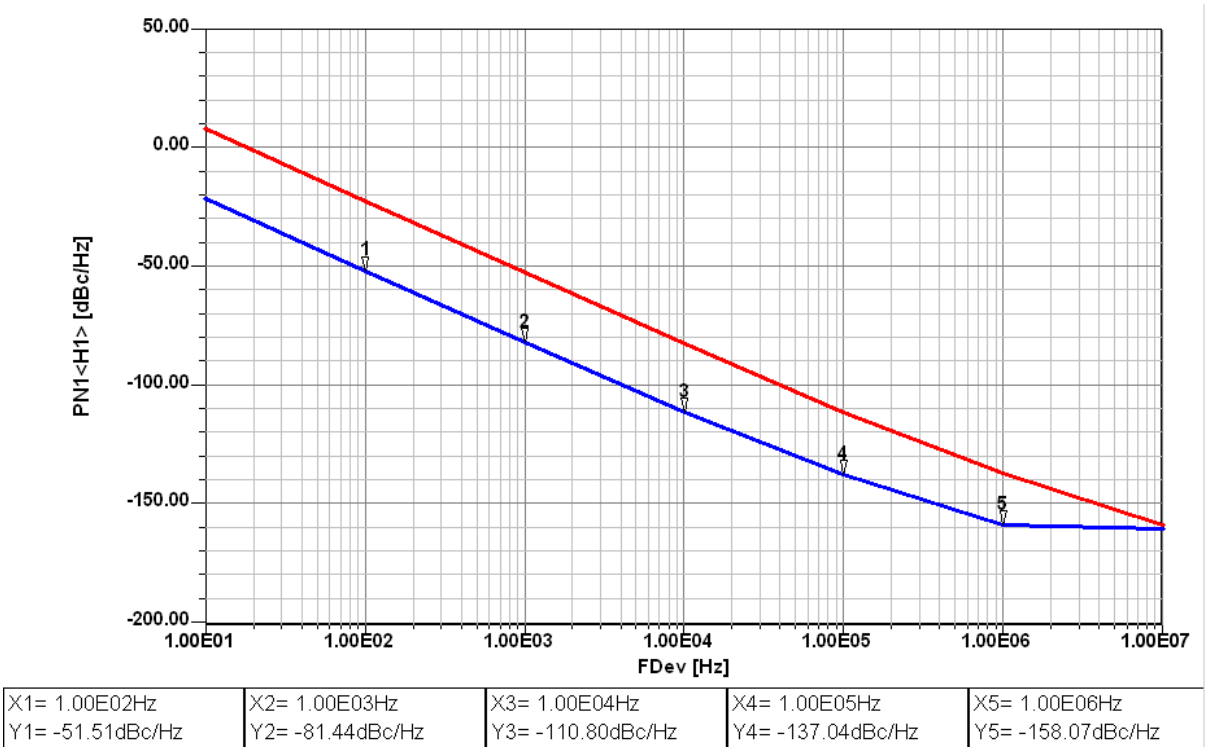


Figure 13: Predicted phase noise of the schematic in figure 12. The blue curve is with fixed capacitors, and the red curve is the phase noise with diodes.

As stated in the beginning a correct analysis of the oscillator, which is a transistor operating in the large signal stage, requires large signal parameters. The amplifier circuit applies enough negative feedback, to compensate the losses of the tuned circuit and the parasitic elements. Figure 14 shows the typical block diagram of conventional feedback oscillator circuit.

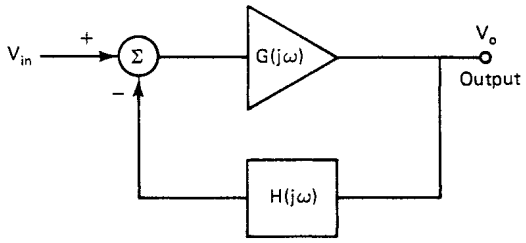


Figure14: A typical block diagram of feedback oscillator circuit [2]

Barkausen in 1935 was the first to state that for this case the product of forward voltage gain and the feedback voltage gain had to be > 1.

$$\frac{V_o}{V_{in}} = \frac{\mu}{1-\mu\beta} > 1 \qquad (1)$$

In recent years engineers used a linear approach and stipulated that the positive loss resistance and to be compensated by a parallel or series negative resistance.

Figure 15 shows a Colpitts oscillator, its input impedance with the feedback capacitors C1 and C2 connected, is calculated and to be seen later.

In the practical case, the device parasitics and loss resistance of the resonator will play an important role in the oscillator design. Figure 15 incorporates the base lead-inductance L_p and the package-capacitance C_p.

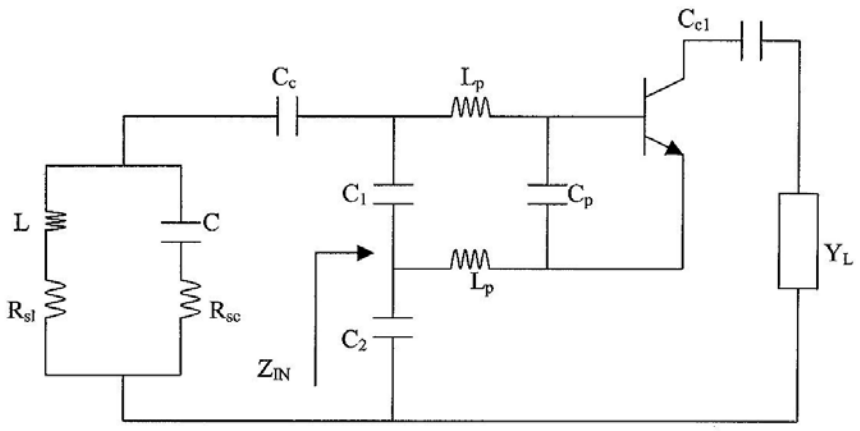


Figure 15: Colpitts oscillator with base-lead inductances and package capacitance. C_C is neglected.

The expression of input impedance is given as [2]

$$Z_{IN}\big|_{pacakage} = -\left[\frac{Y_{21}}{\omega^2(C_1+C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1+C_P+C_2)}{\omega(C_1+C_P)C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega(C_1+C_P)C_2}\right] \quad (2)$$

$$Z_{IN}\big|_{without-pacakage} = -\left[\frac{Y_{21}}{\omega^2 C_1 C_2}\right] - j\left[\frac{(C_1+C_2)}{\omega C_1 C_2}\right] \quad (3)$$

Where L_p is the base-lead inductance of the bipolar transistor and C_p is base-emitter package capacitance. All further circuits are based on this model. From the expression above, it is obvious that the base lead-inductance makes the input capacitance appear larger and the negative resistance appears smaller.

The equivalent negative resistance and capacitance can be defined as [2]

$$R_{NEQ} = \frac{R_N}{(1+\omega^2 Y_{21}^2 L_p^2)} \qquad (4)$$

The assumptions in the past were if R_{NEQ} was sufficiently negative then stable oscillation occurs. However the oscillator is inherently a linearized non-linear circuit and the assumption that this R_{NEQ} was sufficient was not always correct.

The value of R_{NEQ} is the starting value before oscillation, and as the large signal condition takes over, Y21 decreases!

This large signal effect will be analyzed and will become part of the noise analysis und large signal condition.

Large Signal Analysis:

In order to better understand the noise generation in an oscillator, we need to first leave the traditional small signal analysis and consider the actual large signals conditions. So instead of using the familiar linear S parameter, we now resort to their large signal equivalent,

Large Signal *S*-Parameter Measurements

Assume S_{11} and S_{21} are functions only of incident power at port 1 and S_{22} and S_{12} are functions only of incident power at port 2. Note: the plus (+) sign indicates the forward wave (voltage) and the minus (-) sign would be the reflected wave (voltage).

$$S_{11} = S_{11}\left(\left|V_1^+\right|\right) \quad S_{12} = S_{12}\left(\left|V_2^+\right|\right) \qquad (5)$$

$$S_{21} = S_{21}\left(\left|V_1^+\right|\right) \quad S_{22} = S_{22}\left(\left|V_2^+\right|\right) \qquad (6)$$

The relationship between the traveling waves now becomes

$$V_1^- = S_{11}(V_1^+)V_1^+ + S_{12}(V_2^+)V_2^+ \qquad (7)$$

$$V_2^- = S_{21}(V_1^+)V_1^+ + S_{22}(V_2^+)V_2^+ \qquad (8)$$

Measurement is possible if V_1^+ is set to zero,

$$S_{12}(V_2^+) = \frac{V_1^-(V_2^+)}{V_2^+} \qquad (9)$$

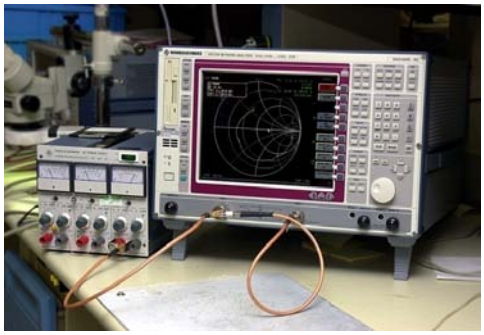
Check the assumption by simultaneous application of V_1^+ and V_2^+

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} F_1(V_1^+, V_2^+) \\ F_2(V_1^+, V_2^+) \end{bmatrix} \qquad (10)$$

If harmonics are neglected, a general decomposition is

$$\begin{bmatrix} V_1^-(V_1^+, V_2^+) \\ V_2^-(V_1^+, V_2^+) \end{bmatrix} = \begin{bmatrix} S_{11}(V_1^+, V_2^+) & S_{12}(V_1^+, V_2^+) \\ S_{21}(V_1^+, V_2^+) & S_{22}(V_1^+, V_2^+) \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \qquad (11)$$

Figure 16 shows the R&S vector analyzer and the test fixture for the transistor of choice.



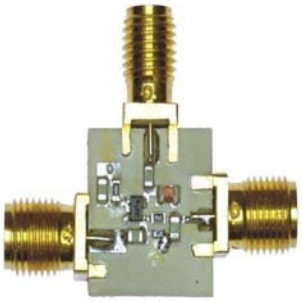


Figure 16: Typical measurement setup for evaluation of large signal parameters (R&S vector analyzer and the test fixture for the transistor of choice)

The bias, drive level, and frequency dependent S parameters are then obtained for practical use. Since we did not have an access to AT41486, we used the infineon transistor BFP520 as an example.

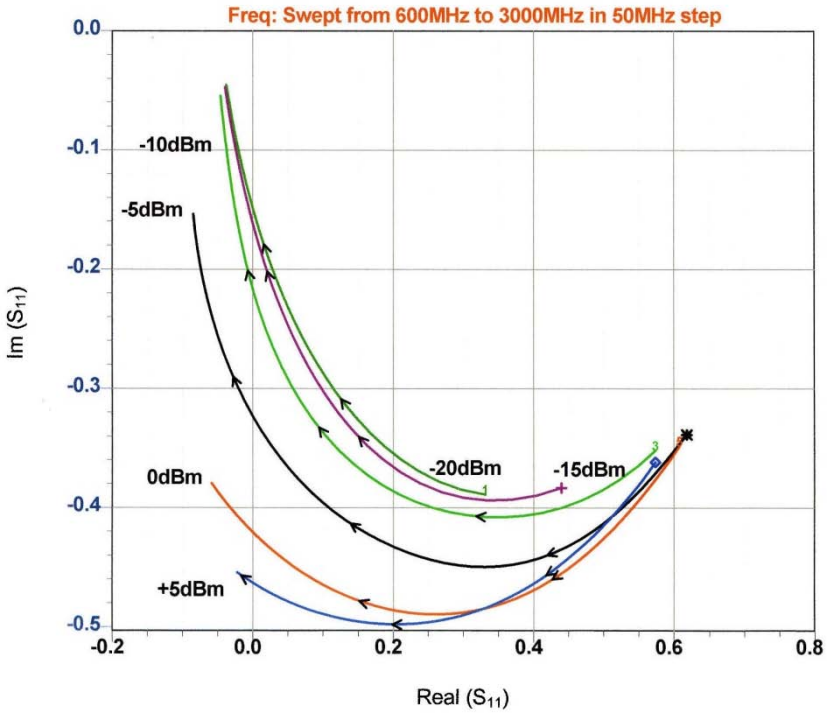


Figure 17: Measured large-signal S_{11} of the BFP520 [2, pp. 68].

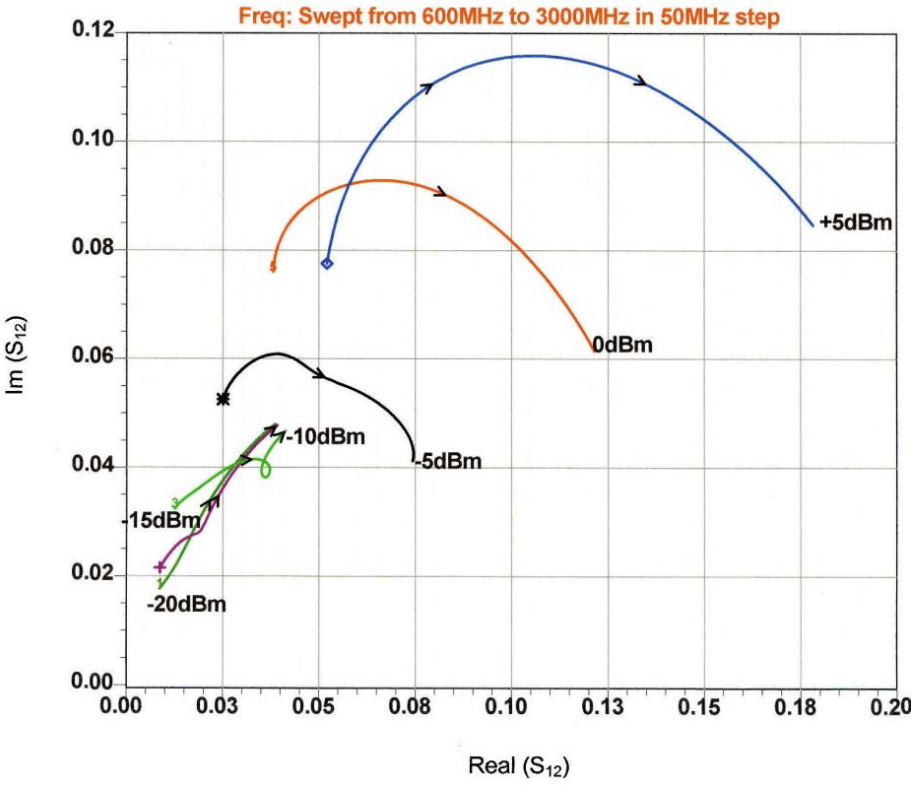


Figure 18: Measured large-signal S_{12} of the BFP520 [2, pp. 68]

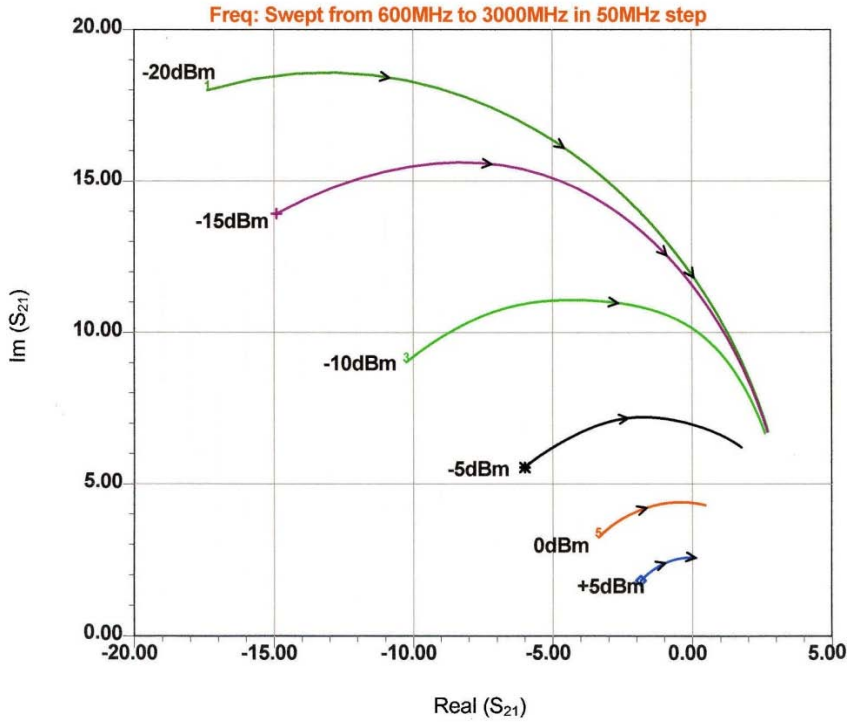


Figure 19: Measured large-signal S_{21} of the BFP520 [2, pp. 69].

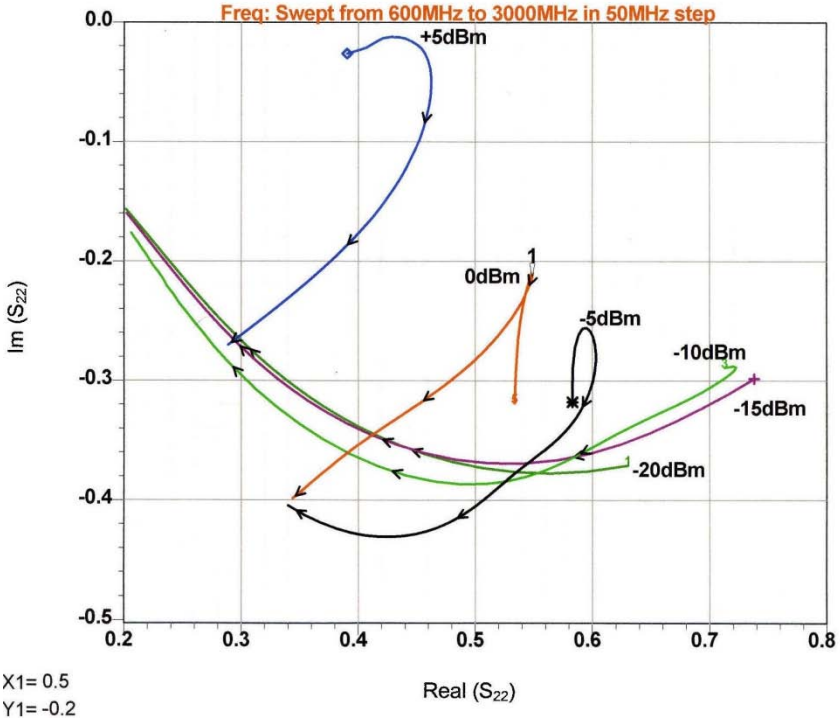


Figure 20: Measured large-signal S_{22} of the BFP520 [2, pp. 69].

The legal definitions of large signal S parameter apply only for a 50-Ohm termination. In our case, an oscillator, the harmonic related S parameters could be neglected. Otherwise the load pull technique applies.

Why are these parameters of interest for us?

They show the dramatic change of S_{11} and S_{21} as a function of frequency and bias level. For the Colpitts oscillator, where the collector is separated S22 is less relevant and since the feedback is external, S12 also less important, depending on the frequency. If calculating the negative resistance to compensate the losses, we must insert the large signal frequency depending value for Y_{21}.

Large-Signal Oscillator Design and Start-Up Condition

As a basic requirement for producing a self-sustained near-sinusoidal oscillation, an oscillator must have a pair of complex-conjugate poles on the imaginary axis i.e. in the right half of s-plane with α>0.

$$P(p_1, p_2) = \alpha \pm j\beta \qquad (12)$$

When the *Barkhausen criterion* is met, the two conjugate poles of the overall transfer function are located on the imaginary axis of the s-plane. Any departure from that position will lead to an increase or a decrease of the amplitude of the oscillator output signal in time domain, which is shown in Figure 21. Figure 22 shows the typical transient simulation of a ceramic resonator-based high-Q oscillator, where node of the voltage is taken from the emitter.

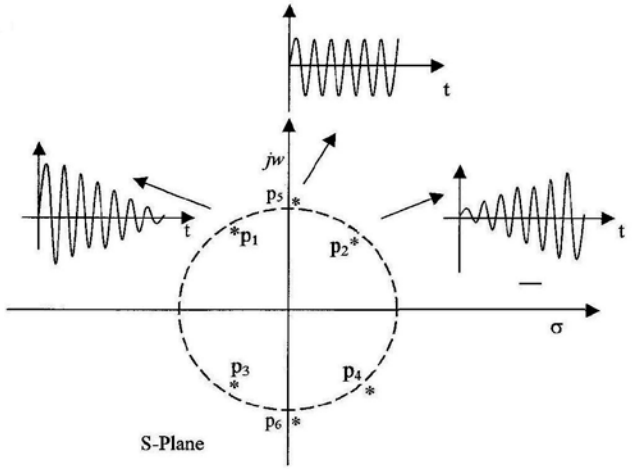


Figure 21: Typical frequency domain root locus and the corresponding time domain response [2, pp. 96].

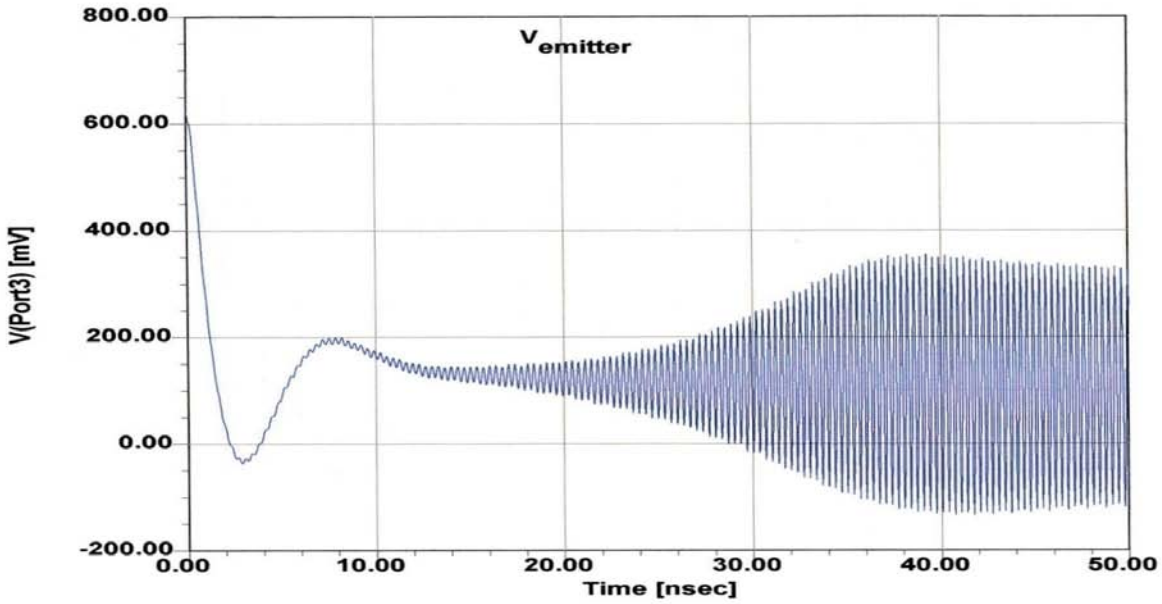


Figure 22: Typical transient simulation of a ceramic resonator-based high-Q oscillator (node of the voltage for display is taken from the emitter) [2, pp.100].

The steady state oscillation condition can be expressed as

$$\Gamma_a(A, f)\Gamma_r(f)\big|_{f=f_0} \Rightarrow \Gamma_a(A_0, f_0)\Gamma_r(f_0) = 1 \qquad (13)$$

For brief insights about the negative resistance oscillator, a block diagram of one-port negative reflection model is shown in Figure 23.

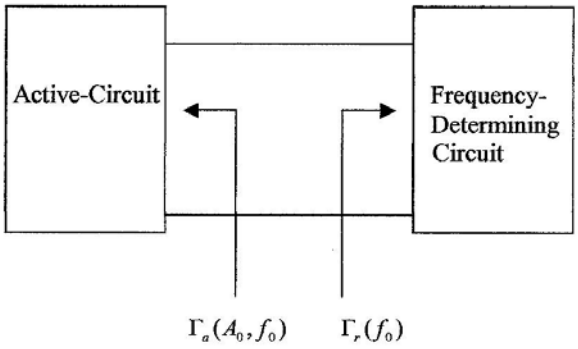


Figure 23: Schematic diagram of a one-port negative reflection model.

Figure 24 illustrates the start and steady-state oscillation conditions.

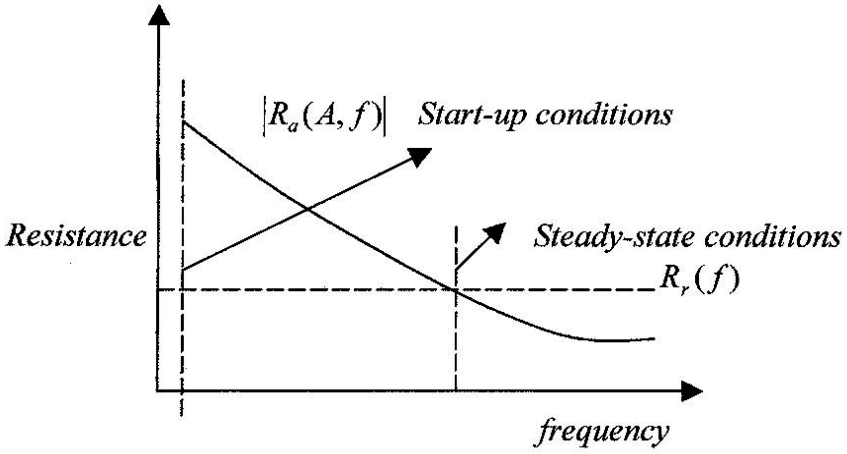


Figure 24: A typical start and steady-state oscillation conditions.

As described in Figure 24, R_a (*A*, *f*) is the starting negative Resistance, which gets lower as the amplitude increases. Therefore, feedback must be sufficient to maintain enough negative resistance to sustain oscillating.

Time-Domain Behavior

The large-signal transfer characteristic affecting the current and voltage of an active device in an oscillator circuit is nonlinear. It limits the amplitude of the oscillation and produces harmonic content in the output signal. The resonant circuit and resulting phase shift sets the oscillation frequency. The nonlinear, exponential relationship between the voltage and current of a bipolar transistor is given as

$$i(t) = I_s e^{\frac{qv(t)}{kT}} \tag{14}$$

$$v(t) = V_{dc} + V_1 \cos(wt) \tag{15}$$

$$i_e(t) = I_s e^{\frac{qv(t)}{kT}} \tag{16}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{\frac{qV_1 \cos(wt)}{kT}} \tag{17}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{x\cos(wt)} \tag{18}$$

assuming, $I_c \approx I_e$ (β>10)

The normalized drive level is

$$x = \frac{V_1}{(kT/q)} = \frac{qV_1}{kT} \qquad (19)$$

$i_e(t)$ is the emitter current and x is the drive level which is normalized to kT/q.

From the Fourier series expansion, $e^{x\cos(wt)}$ is expressed as

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) \qquad (20)$$

$a_n(x)$ is a Fourier coefficient and given as

$$a_0(x)\big|_{n=0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}d(wt) = I_0(x) \qquad (21)$$

$$a_n(x)\big|_{n>0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}\cos(nwt)d(wt) = I_n(x) \qquad (22)$$

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) = I_0(x) + \sum_1^{\infty} I_n(x)\cos(nwt) \qquad (23)$$

$I_n(x)$ is the modified Bessel function.

As $x \to 0 \Rightarrow I_n(x) \to \frac{(x/2)^n}{n!}$ (24)

$I_0(x)$ are monotonic functions having positive values for x≥0 and n≥0; $I_0(0)$ is unity, whereas all higher order functions start at zero.

The short current pulses are generated from the growing large-signal drive level across the base-emitter junction, which leads to strong harmonic generation. The emitter current represented above can be expressed in terms of harmonics as [2].

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} I_0(x)\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \qquad (25)$$

$$I_{dc} = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \tag{26}$$

$$V_{dc} = \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s I_0(x)}\right] \Rightarrow \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s}\right] + \frac{kT}{q}\ln\left[\frac{1}{I_0(x)}\right] \tag{27}$$

I_s = collector saturation current

$$V_{dc} = V_{dcQ} - \frac{kT}{q}\ln I_0(x) \tag{28}$$

$$i_e(t) = I_{dc}\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \tag{29}$$

αI_e and Y_{21} are the current source and large-signal transconductance of the device given by the ratio of the fundamental-frequency component of the current to the fundamental-frequency of the drive voltage.

$$Y_{21} = \left.\frac{I_{1peak}}{V_{1peak}}\right|_{fundamental-frequency} \tag{30}$$

$$I_1\big|_{n=1} = I_{dc}\left[1 + 2\sum_1^{\infty}\frac{I_1(x)}{I_0(x)}\cos(wt)\right] \Rightarrow I_{1peak} = 2I_{dc}\frac{I_1(x)}{I_0(x)} \tag{31}$$

x = normalized drive level

$$V_1\big|_{peak} = \frac{kT}{q}x \tag{32}$$

$$Y_{21}\big|_{large-signal} = G_m(x) \tag{33}$$

$$Y_{21}\big|_{small-signal} = \left.\frac{I_{dc}}{kT/q}\right| = g_m \tag{34}$$

$$Y_{21}\big|_{large-signal} = G_m(x) = \frac{qI_{dc}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} = \frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \tag{35}$$

$$\frac{[Y_{21}\big|_{large-signal}]_{n=1}}{[Y_{21}\big|_{small-signal}]_{n=1}} = \frac{G_m(x)}{g_m} \Rightarrow \frac{2I_1(x)}{xI_0(x)} \tag{36}$$

$$\left|Y_{21}\right|_{small-signal} > \left|Y_{21}\right|_{large-signal} \Rightarrow g_m > G_m(x) \qquad (37)$$

This allows us to calculate the frequency dependent transconductance, which is needed to optimize the circuit for best noise performance.

The following picture (Figure 25) shows the collector current as a function of time and the normalized base drive voltage *x*. For larger values of *x*, the current and voltage peaks may require a larger transistor. As a result, the time the tuned circuit during less time gets loaded, is reduced and the time average Q is higher.

Figure 26 shows the phase noise of an LC-based 1GHz oscillator as a function of X. For higher values of X the phase noise improves significantly.

The dependency of x can be expressed as

$$x = \frac{R_P G_m C_2}{C_1} \qquad (38)$$

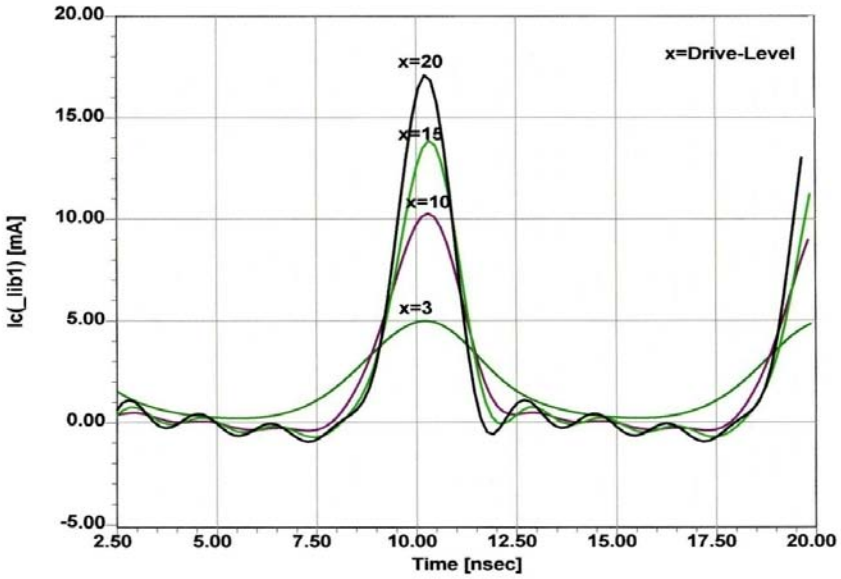


Figure 25: Plot shows the collector current as a function of time with respect to normalized base drive Voltage *x*.

For large drive level, $x \propto C_2$, and the corresponding conduction angle of the output current is given as

$$\varphi = \cos^{-1}\left[1 + \frac{\ln(0.05)}{x}\right] \Rightarrow \varphi \approx \cos^{-1}\left[1 - \frac{3}{x}\right] \qquad (39)$$

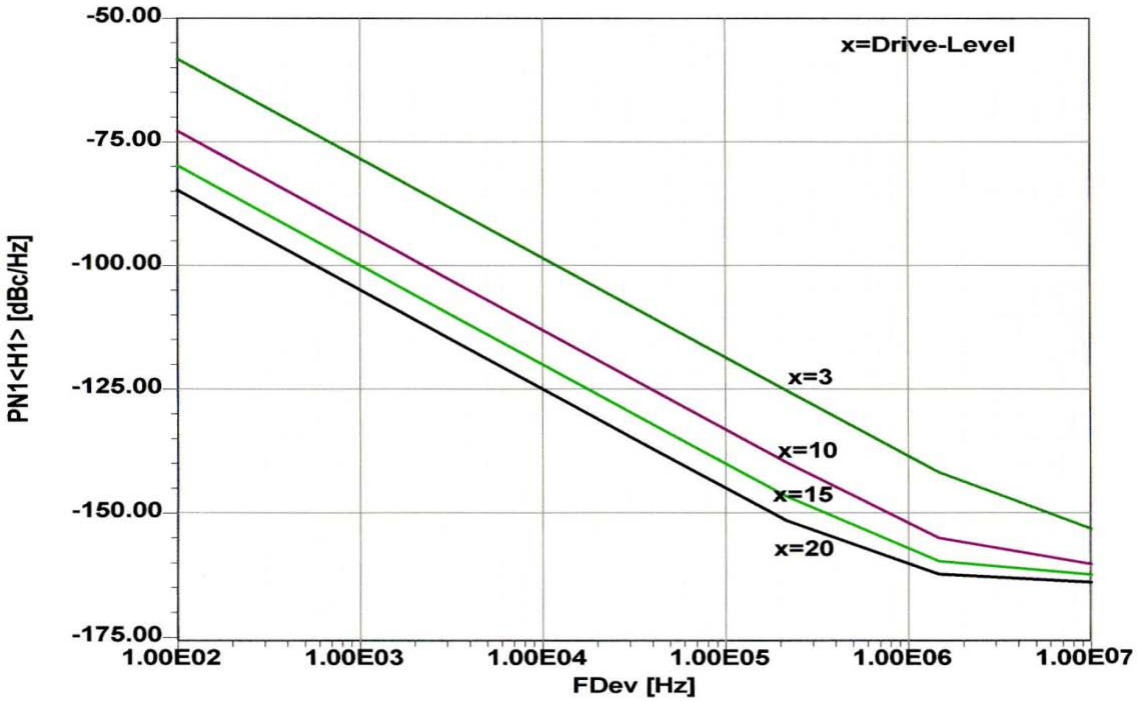


Figure 26: A typical phase noise plot of 1GHz oscillator as a function of x

There is a limit for x, not only due to the limits of voltage and current but also because of reverse biasing of the base collector diode which then makes the circuit really noisy.

Having learned how to design the feedback circuit and introduced the conducting angle and its calculation we have simulated and confirmed the influence on the phase noise, but have not really introduced the oscillator phase noise.

Phase noise in Oscillators

A Linear approach:

In 1965 Leeson developed a model for a noisy transistor oscillator based on a phase modulator, an amplifier, a low pass filter and a resonator, see (Figure 27). In general, oscillator can be viewed as a mixer, where the sum of all inputs is collected and superimposed on the oscillator. Figure 28 shows the components where oscillator acts like a mixer circuit.

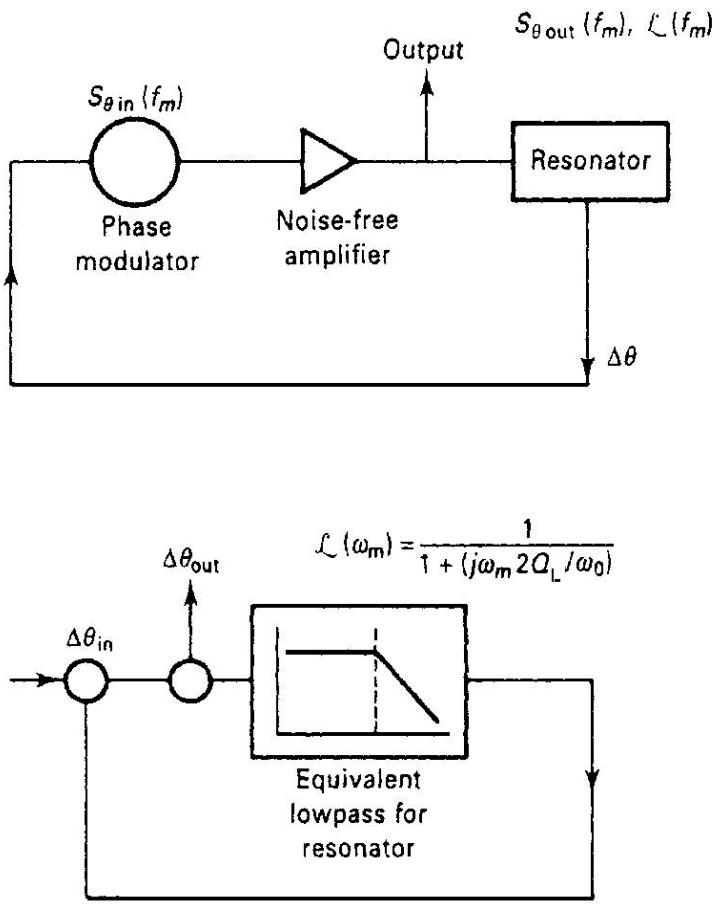


Figure 27: A typical linear oscillator phase noise model (block diagram)

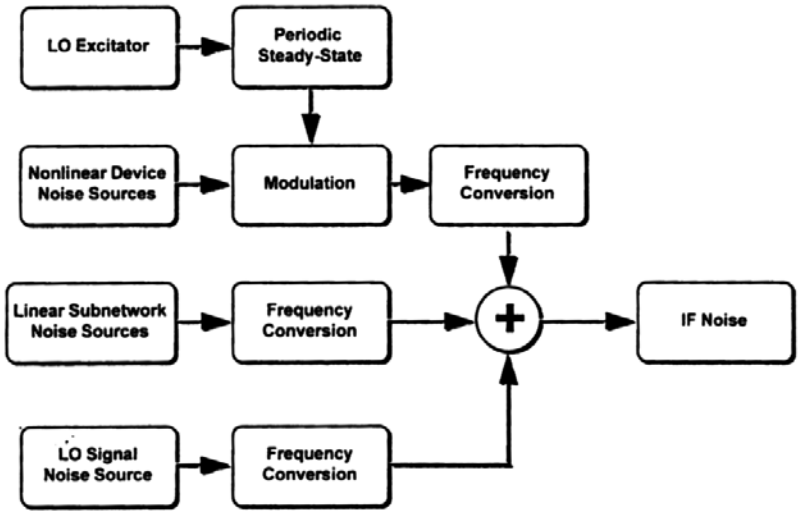
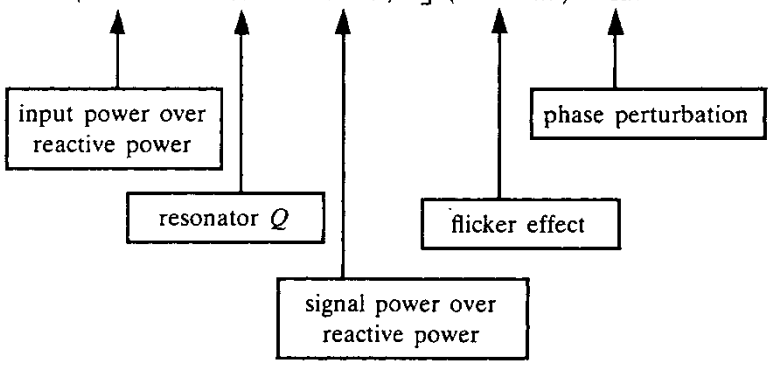


Figure 28: A typical block diagram of mixer circuit, where the oscillator acts like a mixer.

From [2], the resulting signal in linear terms can be calculated as

$$\mathcal{L}(f_m) = \frac{1}{2}\left[1 + \frac{\omega_o^2}{4\omega_m^2}\left(\frac{P_{\text{in}}}{\omega_o W_e} + \frac{1}{Q_{\text{unl}}} + \frac{P_{\text{sig}}}{\omega_o W_e}\right)^2\right]\left(1 + \frac{\omega_c}{\omega_m}\right)\frac{FkT_o}{P_{\text{sav}}}$$



(40)

Equation (40) is the linear Leeson equation, with the pushing effect omitted and the flicker term added by Dieter Scherer (Hewlett Packard, about 1975), the final version with the pushing (VCO effect) added by Rohde, is

$$L\ (f_m) = 10\log\left\{\left[1 + \frac{f_0^{\,2}}{(2f_m Q_L)^2}\right]\left(1 + \frac{f_c}{f_m}\right)\frac{FkT}{2P_{sav}} + \frac{2kTRK_0^{\,2}}{f_m^{\,2}}\right\} \qquad (41)$$

Where

$L\ (f_m)$ = ratio of sideband power in a 1 Hz bandwidth at f_m to total power in dB

f_m = frequency offset

f_0 = center frequency

f_c = flicker frequency

Q_L = loaded Q of the tuned circuit

F = noise factor

$kT = 4.1 \times 10^{-21}$ at 300 K_0 (room temperature)

P_{sav} = average power at oscillator output

R = equivalent noise resistance of tuning diode (typically 50 Ω - 10 kΩ)

K_o = oscillator voltage gain

The problem with this is that key values like loaded Q, large signal NF and output power are not known a priory and the effect of transistor distortion are not included. In some way this provides sometimes an unrealistic good phase noise. On the other hand, it shows the limitation for reasonable values and this presentation will show some mechanism to overcome this.

Figure 29 shows the plot for an ideal 1 GHz LC-based oscillator phase noise of about -140dBc/Hz at offset of 10 kHz offset, assuming unloaded Q of 1E6, loaded Q of 500, noise factor 6 dB, flicker frequency 1kHz, oscillator voltage gain 1Hz/V, equivalent noise resistance of tuning diode 1Ohm and average power at oscillator output 10dBm. Even today this is very much state of the art designer can achieve.

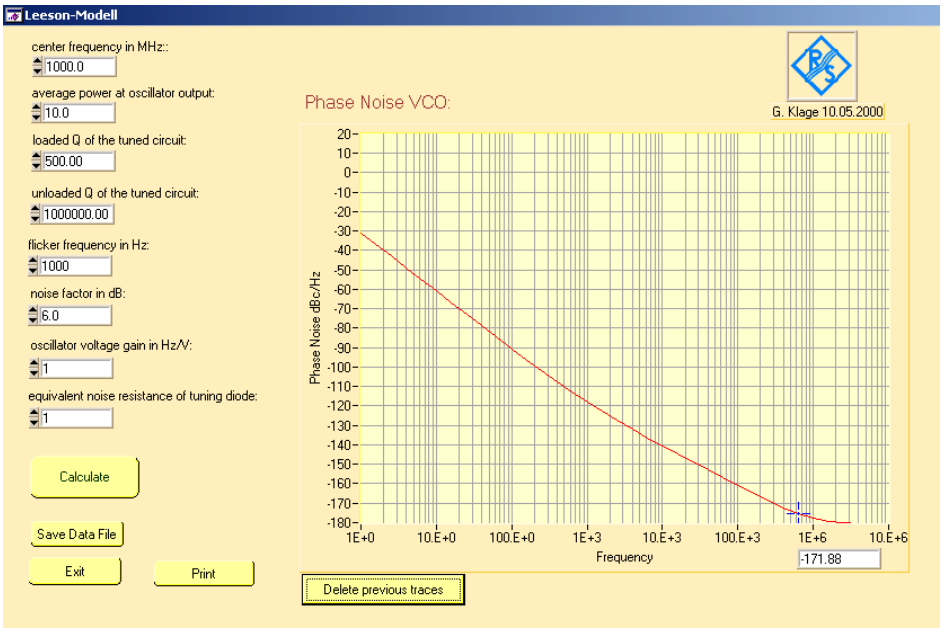


Figure 29: A typical phase noise plot for an ideal 1 GHz oscillator phase noise of about –140dBc/Hz at offset of 10 kHz offset, assuming unloaded Q of 1E6, loaded Q of 500, noise factor 6 dB, flicker frequency 1kHz, oscillator voltage gain 1Hz/V, equivalent noise resistance of tuning diode 1Ohm and average power at oscillator output 10dBm.

The non-linear noise approach [2, Ch-8]:

The equations (41) use a linearized system and are too simplified.

To start the nonlinear noise calculation, we look at the noise sources. The resonator noise is [2, Ch-8, pp. 159-232]

$$\left|\overline{e_R^2(f)}\right|_{\omega=\omega_0} = 4kTBR_s \qquad (42)$$

R_s is the series equivalent noise resistance, based on the losses of the resonator.

The circuit equation for the oscillator with the negative resistance present is [2, Ch-8, pp. 159-232]

$$L\frac{di(t)}{dt}+(R_L-R_N(t))i(t)+\frac{1}{C'}\int i(t)dt=e_N(t) \qquad (43)$$

This is a non-homogeneous differential equation, which can be simplified to [2, Ch-8, pp. 159-232]

$$L\left[-I_1(t)(\omega+\frac{d\varphi_1(t)}{dt})\sin[\omega t+\varphi_1(t)]+\frac{dI_1(t)}{dt}\cos[\omega t+\varphi_1(t)]\right]+\left[(R_L-R_N(t))I(t)\right]+$$

$$\frac{1}{C}\left\{\left[\frac{I_1(t)}{\omega}-\frac{I_1(t)}{\omega^2}\left(\frac{d\varphi_1(t)}{dt}\right)\right]\sin[\omega t+\varphi_1(t)]+\frac{1}{\omega^2}\left(\frac{dI_1(t)}{dt}\right)\cos[\omega t+\varphi_1(t)]\right\}=e_N(t) \qquad (44)$$

Further

where $\overline{R_N(t)}$ is the average negative resistance under large signal condition.

$$\overline{R_N(t)}=\left[\frac{2}{T_0 I}\right]\int_{t-T_0}^{t}R_N(t)I(t)\cos^2[\omega t+\varphi)]dt$$

Contrary to common publications, this is a time variant resistance; ideally it does not degrade the Q outside the on condition. This resistance however is “noisy”.

Since the negative resistance is related to the large signal transconductance and the feedback capacitors of the Colpitts oscillator, we can insert this in the equation above and after a lengthy set of calculation the phase noise under large signal conditions become [2, Ch-8, pp. 159-232]

$$\pounds(\omega)=10\times\log\left[\left[k_0+\left(\frac{k^3k_1\left[\frac{Y_{21}^+}{Y_{11}^+}\right]^4[y]^{4p}}{\left[Y_{21}^+\right]^6[y]^{6q}}\right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\frac{Q_{\max}^2}{Q_0^2}\right] \qquad (45)$$

Where, $y=\frac{C_1}{C_2}$, $k_0=\frac{kTR}{\omega^2\omega_0^2L^2V_{cc}^2C_2^2}$, $k_1=\frac{qI_cg_m^2+\frac{K_fI_b^{AF}}{\omega}g_m^2}{\omega^2\omega_0^4L^2V_{cc}^2}$, $k_2=\omega_0^4(\beta^+)^2$, $k=\frac{k_3}{k_2C_2^2}$

This results in the phase noise values as a function of the large signal parameters. These are identified and the term k_1 adds the semiconductor noise contributions, which are now bias dependent.

The following is a first in the sense, that we calculate the exact solution of the phase noise of the transmission line, using a smaller than quarter wavelength resonator (inductive) and substitute this for the inductor. This uses a tangent function and if the losses would be applied a hyperbolic tangent function. In this case we assume that the Q is sufficiently high that the value of the $\cosh(\alpha l) \approx \sinh(\alpha l) \approx e^{\frac{\alpha l}{2}}$

The characteristic impedance of most of the coaxial resonator is approximately 10ohms and can be calculated by the following equation. D is the outer diameter or side length of the coaxial resonator, d is the inner diameter of the coaxial resonator and εr is the dielectric constant.

$$Z = \frac{60}{\sqrt{\varepsilon r}} \ln\left(\frac{D}{d}\right) = \frac{60}{\sqrt{38.6}} \ln\left(\frac{6}{2.42}\right) = 8.768\Omega$$

We know that, $L = \frac{Z_l}{\omega}$ [3]

Where, $Z_l(f) = jZ\tan(\beta l)$; $Z_l(f) = jZ\tan\left(\frac{\omega}{v_P} l\right)$;

Therefore $L = j\frac{Z}{\omega}\tan\left(\frac{\omega}{v_P} l\right)$ where, v_P is the Phase velocity and l is the length of the coaxial resonator.

As seen from this equation L is the function of frequency and needs to be calculated for each computation of frequency sweep.

So the modified equation for phase noise calculation is as follows.

$$\pounds(\omega) = 10 \times \log\left[\left[k_0 + \left(\frac{k^3 k_1 \left[\frac{Y_{21}^+}{Y_{11}^+}\right]^4 [y]^{4p}}{\left[Y_{21}^+\right]^6 [y]^{6q}}\right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right]\frac{Q_{\max}^2}{Q_0^2} \qquad (46)$$

Where, $y = \frac{C_1}{C_2}$, $k_0 = \frac{kTR}{\omega^2 \omega_0^2 \left(j\frac{Z}{\omega}\tan\left(\frac{\omega}{v_P} l\right)\right)^2 V_{cc}^2 C_2^2}$, $k_1 = \frac{qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega^2 \omega_0^4 \left(j\frac{Z}{\omega}\tan\left(\frac{\omega}{v_P} l\right)\right)^2 V_{cc}^2}$, $k_2 = \omega_0^4 (\beta^+)^2$,

$k = \frac{k_3}{k_2 C_2^2}$

The phase noise equation (46) above can be differentiated to determine the best possible phase noise. This is a better approach then to depend on the optimizer of the HB simulator.

$$\frac{\partial\left|\phi^2(\omega,y,k)\right|}{\partial y}\Rightarrow 0 \qquad (47)$$

$$\frac{\partial}{\partial y}\left[\left\{\left[\left[k_0+\left(\frac{k^3k_1\left[\frac{Y_{21}^+}{Y_{11}^+}\right]^4[y]^{4p}}{\left[Y_{21}^+\right]^6[y]^{6q}}\right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right\}\frac{Q_{\max}^2}{Q_0^2}\right]_{y=m}\Rightarrow 0 \qquad (48)$$

For minimization of noise and regime of y, we leave this task and its calculation and validation to the interested reader; detailed information can be found in [2, pp. 181].

The next step is to think about improving quality factor of resonator tank circuit and techniques to minimize the phase noise for modern oscillators (narrowband and wideband voltage controlled oscillator) for current and later generation of communications systems.

Validation

Modern expensive harmonic balance based simulators such as ADS from Agilent and Serenade from Ansoft, part of Ansys, can be used to determine the resulting phase noise with a high degree of accuracy, about 2dB typical error. By introducing a novel mathematical method as shown above, based on measured large signal parameters, the correct phase noise can be calculated, relative to the simulation. Our test case is figure 12.

A similar 800MHz VCO from the standard listing of Synergy microwave was used to further validate the method. The analysis with the Harmonic balance program indicates the predicted phase noise (Figure 30). The flicker corner frequency is about 1kHz, though it is not distinctly visible due to high Q resonator in use and the the phase noise at 10 KHz offset is -132.14 dB/Hz.

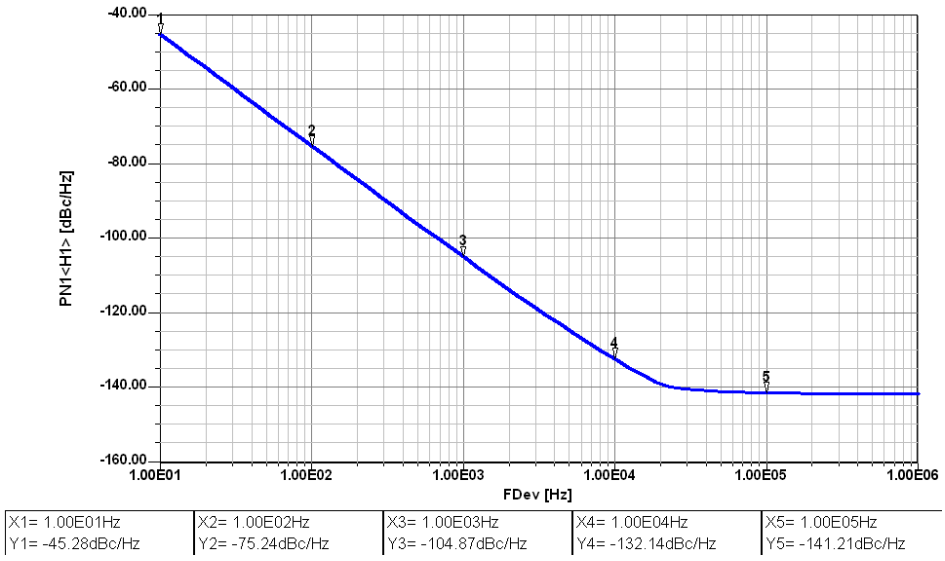


Figure 30: A CAD Simulated (Ansoft Designer) phase noise plot for 1 GHz oscillator

The simulator fails to give any change in phase noise above 1MHz offset due to numerical problems of the simulator. The calculation based on equation 46 predicted the phase noise shown in figure 31. It can show a flicker corner at 1KHz and the predicted phase noise at 10KHz is around 130.5dBc/Hz. The 10MHz offset phase noise calculates to about -170dBc/Hz.

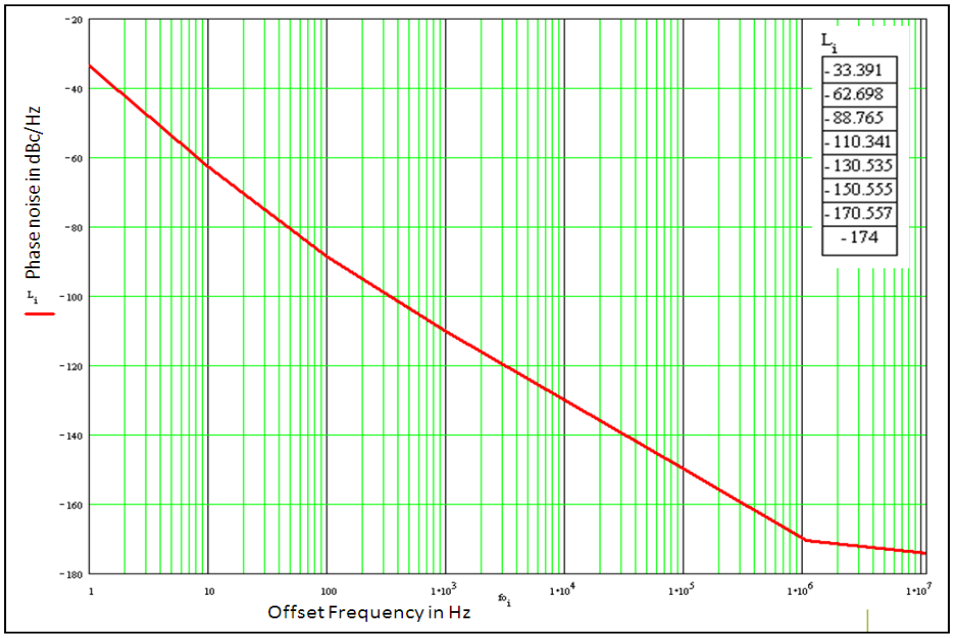


Figure 31: Predicted phase noise based on equation 46 using MathCad.

The measured response of this unit is shown verified on R&S FSUP network analyzer and the Agilent Network analyzer E5052A. Shown in Figure 32-A (R&S FSUP measurement) and Figure 32-B (Agilent E5052A measurement). This data matches well with the calculation but does not agree with the simulation at 1MHz and further out.

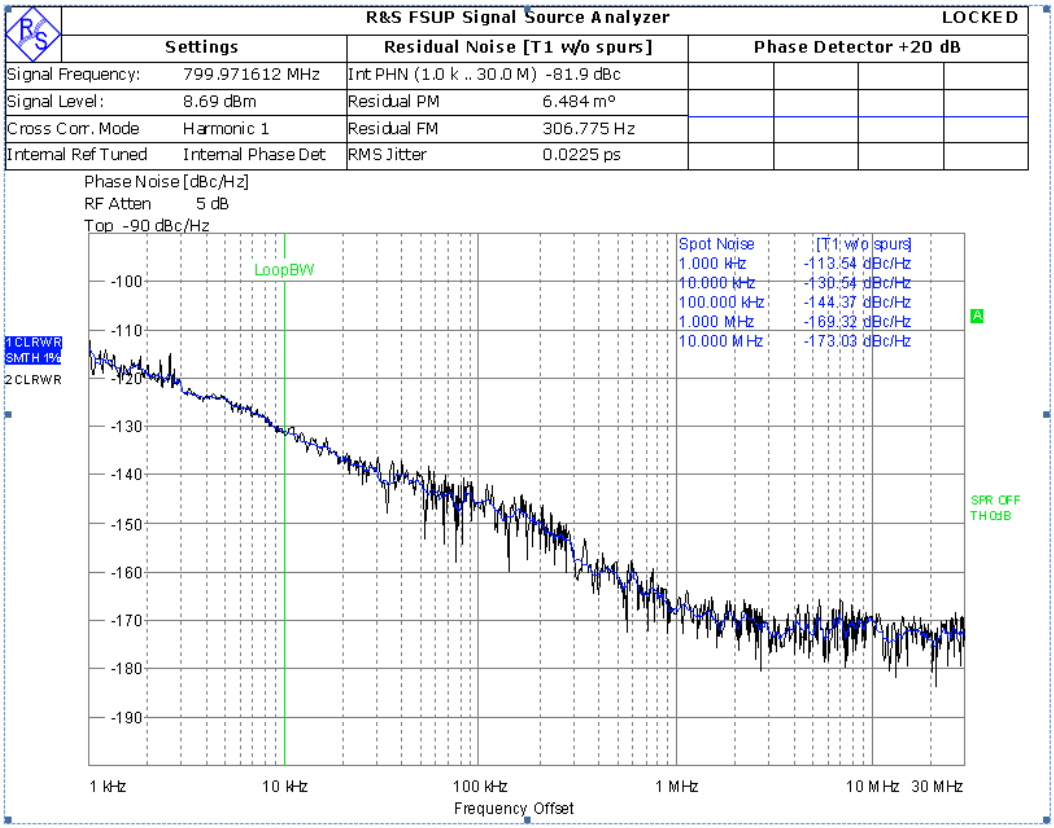


Figure 32-A: Measurement of the unit with an R&S FSUP analyzer.

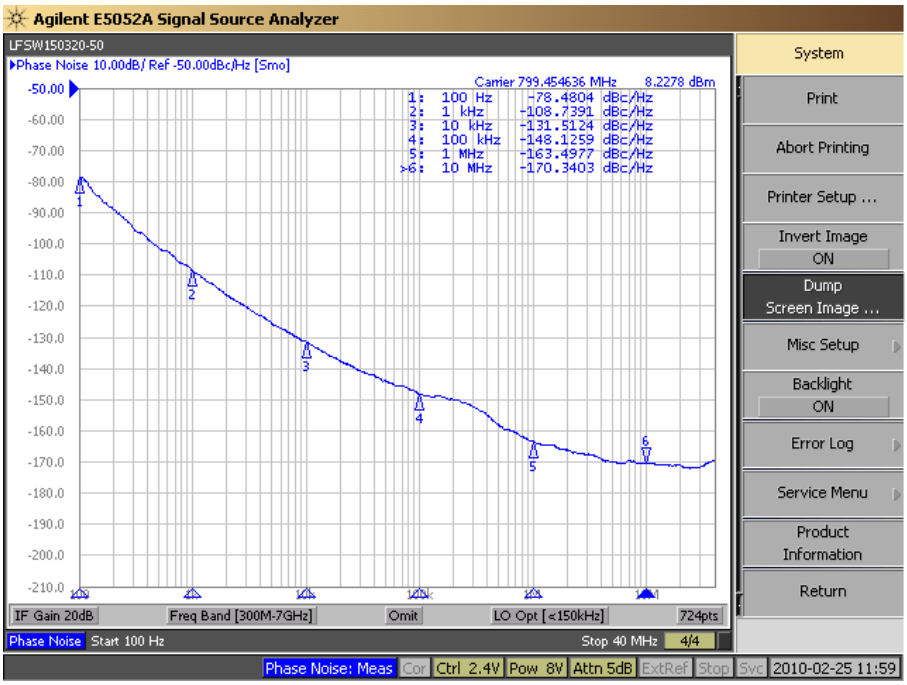


Figure 32-B: Measurement of the Unit with an Agilent E5052A analyzer.

Acknowledgements:

We would like to thank Rucha Lakhe for helping us to put this report together.

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An Educationnal Approach to Electromagnetic Compatibility of Integrated Circuits

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Abstract— **This paper presents the strategies used for effective teaching in integrated circuit (IC) design under Electromagnetic Compatibility (EMC) constraints. It presents the general context of EMC of ICs and details the EMC-aware IC design course given in companies and several institutes in France. Collaborations with industry have produced a set of learning resources and design tools to support the development of industry relevant EMC skills and lifelong learning skills. The courses enable students to learn about EMC measurements and modeling at IC level and their implications using a set of user friendly tools. The courses taught in university and in industry have consistently produced high levels of student/engineer satisfaction.**

Keywords: EMC, Integrated circuits, parasitic emission, susceptibility, standards, IEC, IBIS, modeling

I. CONTEXT

Electromagnetic compatibility (EMC) is considered to be the third cause of integrated circuit (IC) redesign after design errors and Electrical Overstress. EMC is a fundamental constraint that components must meet to ensure the simultaneous operation of all nearby electronic devices and the safety of users. Numerous courses and educational books have addressed EMC at system, cable [1] and printed-circuit board (PCB) levels [2]. However, semiconductor devices are often the source as well as the victim of electromagnetic interferences, as described in the research compilation [3]. Possible mechanisms for coupling of electromagnetic noise at integrated circuit (IC) level include the wire connections such as the supply lines, the coupling of the package leads to electric or magnetic field, or even the coupling of the induced interferences directly to the silicon chip (Fig. 1). Also represented in the figure are couplings through cables and PCB tracks.

Ensuring EMC at circuit level implies an effective reduction of noise sources and disturbance origins, in order to comply with EMC standards defined by the application of by the IC customers. Its modeling has become mandatory to ensure a predictive approach of EM-induced perturbation risk, which requires tools, models and specific EMC knowledge.

Until recently, no specific course focused on EMC of ICs has been made available, mainly because of the intrinsic complexity of the topic, which requires strong skills both in electromagnetism, electricity and microelectronics, the lack of expertise, and the high degree of confidentiality regarding EMC-related design issues. In this paper, we present what we believe to be the first 2-days course only focused on EMC of ICs, based on the latest research results available from the community of EMC-IC experts [4].

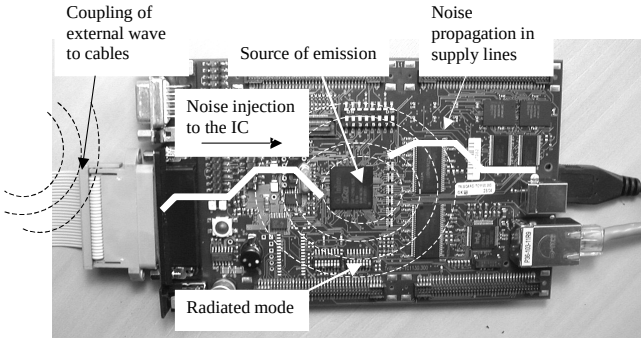

Figure 1. Illustration of electromagnetic compatibility at integrated circuit level (From [3])

II. EMISSION, IMMUNITY

A. Integrated Circuit Emission

Parasitic emission caused by the switching activity of integrated circuits (ICs) has increased in importance with the tremendous progress in Complementary Metal-Oxide Semiconductor (CMOS) technology. When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pluses provokes enormous current flows within the chip, close to 100 A in the latest generation of high performance micro-processors. The switching of internal gates induces transient current flow within the circuit and its surroundings, as shown on figure 2. Supply and bus wires can convert the transient currents into voltage drops on power and ground supplies. Parasitic inductances of interconnections are the main responsible of voltage drops [1-3]. Voltage drops may propagate to circuits sharing the same supply network, which provokes conducted and radiated emission.

This work has been supported by the European project PIDEA+ "EMC Pack", MEDEA+ "Parachute" and French Aerospace Valley project "EPEA"

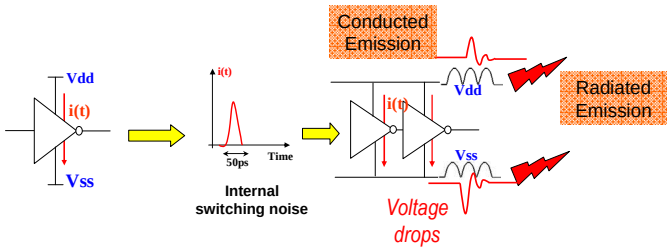

Figure 2. IC parasitic emission due to switching activity and parasitic power supply interconnections

There exists a diverging trend between, on one side, the customer pressure for low-emission IC, and in the other side, intrinsic emission levels which tend to increase and to broaden in frequency domain.

B. Integrated Circuit Susceptibility

The trend towards nano-scale devices has major consequences on integrated circuits (ICs) immunity. First, the constant supply voltage decrease reduces the static noise margin of electrical signals and thus increases the IC susceptibility to RFI. Also, as cut-off frequencies increase, circuits become sensitive to faster transient signals.

With the newest technologies, nearly one billion devices related to mixed analogue, digital and power technologies share the same piece of silicon. Some parts of the chip generate EMI (digital and power parts) while the others have very low sensitivities regarding the EMI level (analogue and RF parts). It is an issue to ensure that all the embedded functions are able to operate (auto-compatibility).

Meanwhile, IC customer requirements in terms of EMC tend to increase. These opposite trends require immunity design guidelines, specific tools, expertise and ways of precise measurements of EMC performances.

III. COURSE DESCRIPTION

The course is targeted to engineering students in master level, as well as IC designers in industry to address the needs for specific training in EMC-award IC design. The two-days course consists in 6 main parts:

- Introduction to EMC for ICs
- Basic Concepts in EMC of ICs
- Measurement methods for emission and susceptibility
- Modeling techniques
- Design Guidelines for improved EMC
- Future challenges

Half of the time is spend with lectures, including problem-based learning, exercises, and demonstrations; the other half is dedicated to practical training.

The first part presents the challenges for electromagnetic compatibility of integrated circuits and recalls some key examples of IC redesigns because of EM-related non compliance. A set of basic concepts is proposed in the second part, covering specific units, impedance, interconnects, origin of noise, noise margins, time/frequency conversion and 50 Ω matching. The third part focuses on the standard measurement of the IC emission [5] and susceptibility [6]. The fourth part is related to modeling approaches for predicting EMC, based on standards such as IBIS, ICEM, and ICIM [7]. The fifth part is dedicated to the presentation of guidelines to reduce emission and improve immunity at IC level. Finally, roadmaps and future challenges are briefly reviewed, inspired from [8].

IV. PRACTICAL TRAINING

A. EMC of ICs in practice

To support and illustrate the course, we have developed a freeware called IC-EMC [9], a windows-based software demonstrator which aims at simulating parasitic emission and susceptibility of integrated circuits. The full package can be downloaded from www.ic-emc.org, a non-profit site dedicated to EMC of integrated circuits. The tool IC-EMC includes a conventional schematic editor, (See Fig. 3), a set of tools to help user to build EMC models, an interface to Spice for analog simulation and a post-processor for easy comparison between measured and simulated parasitic emission and susceptibility. The tool is used by the teacher as an illustration for most basic concepts covered during the formal course, and by students during practical training sessions.

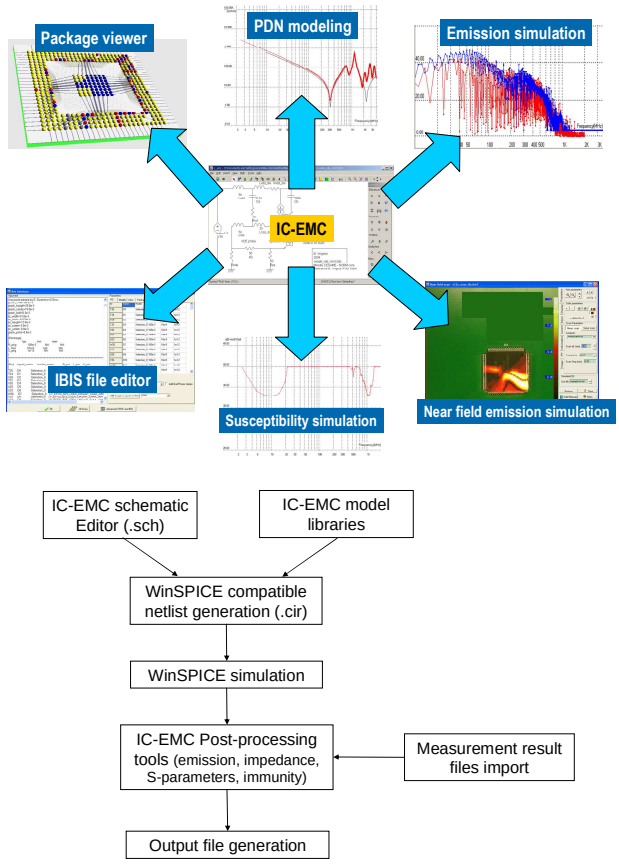

Figure 3. The IC-EMC capabilities in terms of emission and immunity prediction, and the generic flow used to simulate EMC at integrated circuit level

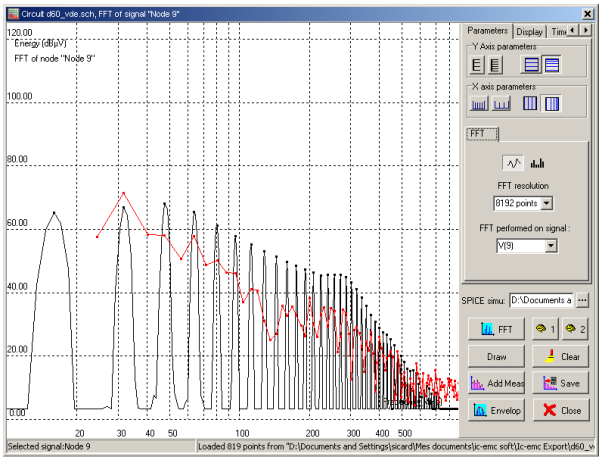

Figure 4. An example of comparison between measured and simulated parasitic emission conducted during the practical session of the course

A set of tools with significant added value for EMC analysis are used during the training:

- An emission model generator which translated an IC specification directly into an approximated noise model. Students are asked to specific a microcontroller and forecast its emission level, without any specific knowledge of the layout details.
- A near- magnetic field estimator based on elementary current dipole radiation. Students may illustrate field cancelation, loop effect reduction at a simple click.
- A library of common standard IEC models, to ease the simulation of 1/150Ω conducted mode and TEM cell radiated mode measurement methods.
- A 3D package viewer based on IBIS, to illustrate the role of R,LC parasitic effects due to package and die connection.

V. EVALUATION

Since the early trainings started in 2002, more than 20 sessions involving 300 students and engineers have been organized, either in a one-day or two-days format. The evaluation of the course impact has made through 1à questions listed in Table I. At the end of this course, the majority of students said they understood the mechanisms of parasitic emission and susceptibility, and felt confident in their ability to handle standard measurements of emission and susceptibility at IC level. Most of IC designers also felt they could take part in a global EM-improvement strategy, and were willing to apply "golden design rules" to address circuits with interference problems.

The evaluation results shown in Fig. 5 include both initial training in engineering departments (ISEN France, ENSME France) and in companies (e.g Nokia, On-semiconductor). It can be observed that not all students find the topic in close relation with their studies, while the vast majority of engineers in companies have found the course highly profitable for their daily work.

TABLE I
COURSE EVALUATION QUESTIONNAIRE

#	Question
1	I appreciated the contents of the training.
2	The level of the training is in accordance with my expectations.
3	The balance between theory and practice was acceptable
4	The contents was adapted to life-long learning.
5	I appreciated the documents given in the training.
6	I appreciated the way the training was taught
7	The contents is clearly related to my work/studies.
8	I may use the contents directly in my activities
9	The lecturer followed the initial planning
10	Overall I was satisfied with the quality of this course.

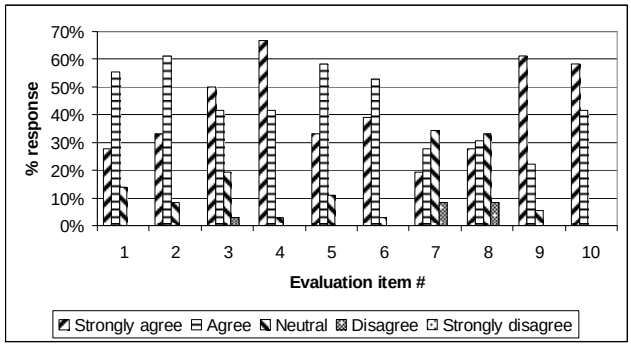

Figure 5. Evaluation of the course "EMC of Ics" compiling 10 course feedback, for a total of more than 100 students

The very high satisfaction rate is also linked with the introducing of a practical training and problem-based approach during lectures, which reinforce discussion, interaction, questions and answers from the audience.

CONCLUSION

This paper has introduced a novel course on EMC of ICs at engineering level, which was successfully taught in engineering schools as well as in industry to enhance the understanding of interference issues at component level and to give practical ways of improving electronic design for improved EMC.

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Adapting to a changing highschool population

Changes in the EE curriculum resulting from math and physics deficiency

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Abstract—**This paper reports the recent changes in the EE Bachelor program at the University of Twente. Recent generations of freshman students exhibited a lack in mathematics skills and the ability to grasp the physics behind the equations. By starting of the curriculum with a new course "Introduction to electronics and electrical engineering (IEEE)" we have managed to solve the issue of lacking entry levels while simultaneously eliminating the unmotivated or under skilled students in a very early stage in their studies.**

I. INTRODUCTION

Due to a change in the Dutch secondary school exam requirements all technical bachelor studies suffer from a discrepancy between the traditionally expected entry levels and the actual knowledge and skills of their freshman. In secondary education the number of hours for physics and math has been reduced and in the mean time there is a growing emphasis on project work, presentation skills, learning to find information and teaching topics that are of social interest (solar cell, global warming). The changes in the high school programs aimed at giving all students, basic math and physics knowledge making math a mandatory part of the exam like Dutch and English language courses. The undesired impact of replacing old fashioned exercise work with project work and computer simulations is that a large portion of the high school population is no longer able to do mathematical manipulation without a graphical calculator. This unfortunately includes some of the students who take up a technical bachelor study. Additionally for good students the high school program is set up so they can finish all assignments in class, resulting in a generation of students that are not accustomed to do homework or work more than 25 hours per week. The present generation of students holds a larger than before percentage of students that consider a pass grade sufficient, nicknamed "the MTV generation attitude".

Fortunately there are still highly motivated and well skilled students graduating from high school with A-level grades as well. This means that any academic education has to deal with a large variety in the level of knowledge and skills when the students start their bachelor studies. Considering the dropping interest to start a career in (electrical) engineering keeping the old BSC EE curriculum and accepting a very large dropout percentage is not an acceptable solution. Therefore at the University of Twente we have decided to change our curriculum by adding an introductory course in the beginning of the first semester. The course "*Introduction to Electronics and Electrical Engineering", IEEE*) should help motivated students pick up the required level and the pace of studying. For those students that do not suffer from a lack in knowledge or skills the course offers the opportunity for to dive deeper into the theoretical background and learning analogies in other technical fields.

II. ASPECTS OF THE NEW IEEE COURSE

The freshman course IEEE has a study load of 8.5 European credits (240 hours). Apart from solving deficiencies in math and physics knowledge and skills it helps students adapt a new work attitude and should work motivational. The course consists of lectures, blocks were students can make exercises (supervised/assisted by teacher), lab works and a final project to integrate the gained knowledge and skills.
Like any class the students encounter the following phases [1]

Orientation
Gaining knowledge
Making it operational
Testing
Reflection

The special part of the course IEEE is that we give an orientation for the entire bachelor program.

A. Mathematical skills

The math skills of all engineering students at the 3 technical universities in The Netherlands is tested in the first week of the semester in a multiple choice test covering high school topics in general algebra, logarithms and powers, goniometric relations and differentiation rules. The test was originally intended as a diagnostic tool. Cleverly chosen wrong answers hinted towards specific problems in the mathematical manipulation skills, see for example figure 1.

The expression $2\ln(p) + 2$ can be rewritten as:

a)	$\ln(p+2)^2$	$\ln p + 2 \neq \ln(p+2)$
b)	$(\ln(pe))^2$	$\ln(p^2) \neq (\ln(p))^2$
c)	$2\ln(pe)$	**Correct**
d)	$\ln(p^2 + e^2)$	$\ln A + \ln B \neq \ln(A+B)$

Figure 1. Multiple choice question and the possible thinking errors

The average score per specialization varies between 35 and 65 %, the highest for the math students. These numbers indicate that the math proficiency is not the determining factor in choosing a career in a technical field.

In interviews, students frequently indicated that they had simply forgotten the knowledge during the long summer break or that a test in the first week of the semester does not give a fair result since they are still getting settled in their new living situation. The first excuse was tested by giving the same test to high school students (with a profile that would qualify them for an engineering study) just after graduation (before the summer break). The results were similar to the freshman results. The second problem was overcome in 2009 by moving the test to the second week of the semester, giving students the possibility to prepare for the test. Although the results did improve slightly, a large majority still did not pass the test despite passing the high school exams.

After having identified the most common deficiencies, a university wide so-called repair course in high school mathematics for those students who fail the entrance test was instated where students could practice numerous exercises to prepare for the second test, 5 weeks later, using a specially developed textbook [2]. Consistently over the period between 2005 and 2009 students in mathematics and applied physics score the best at the entrance test, EE is in the second group.

The second test after the repair program shows an improvement in both the number of correct answers as well as the percentage of students that pass the test, see figure 2. For studies without mandatory repair course the improvement is less and only few students actually follow the program and take the second test. This again indicates that students do not perceive it as a problem when their basic math skills are insufficient.

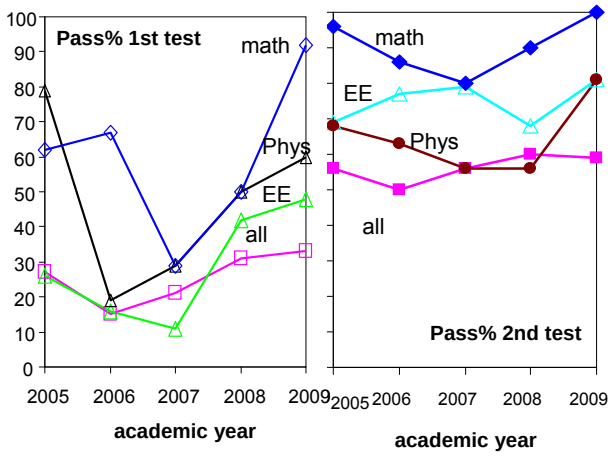

Figure 2. Percentage of students that pass the first (left) and second(right) algebra test for electrical engineering, applied physics, mathematics and all engineering students in the period 2005 to 2009. The repair program is mandatory for EE, Math and approximately 60% of the entire population. It is on a voluntary bases for physics students who fail the first test.

B. Physical insight

A considerable part of the students consider equations as expressions that can be solved using a calculator. The basic knowledge that equations are a description of the physical relation between parameters is taught in school, but since both a graphical calculator and a summary book with equations can be used during the exams the importance of the physical relations does not sink in with the majority of the students.

A second problem that has surfaced is the fact that not all physics knowledge that has to be taught in high school will be part of the exams, and this is known to both teachers and students. This leads to a population of students with a more mixed knowledge. Now not only do students have different high school physics grades indicating different levels of understanding but also depending on their teacher some topics might be sacrificed due to lack of time.

In the course IEEE we intend to deal with difference in physics entrance level treating each topic as “new”, making sure that also for the “good” students there is indeed something to be learned. For example when introducing a resistor in the first lecture we show the different symbols you might find in textbooks, explain that also the connecting wires have a resistance, and that real resistors are temperature dependent.

C. Work attitude and motivation

The curriculum EE is based on a 40 hour work week for the average student. If students do not put in sufficient hours from the first day for their studies a large portion loses the first year al together because they never catch up anymore. Without making attendance mandatory, since this would contradict the learning academic skills idea, we create a program that entices students to put in the required hours. We have allocated a significant portion of the course to lab work. The classes and lab work are intertwined in such a way that the students are motivated to attend class and make the exercises since failure to do so either makes them fail the lab courses, or gets them a just pass grade but they have to miss the “cool” part of the lab work due to lack of time to finish the experiments.

In this freshman class we give and introductory overview of a large part of the bachelor program. This includes topics that are in depth taught in the final stages of the studies. The exam questions on these topics are at the introductory level, but the lab work is much more specialized. In contrast to the old curriculum where the lab works followed the lectures, and was kept to the basics. We now are able to give an outlook over the entire working field of our future graduates. This should have a long term motivational effect. In the first year we introduce the concept of Fourier analysis and show its use for communication systems. We hope this motivates students to work more actively in the second year math course that deals with this topic since they know they will need it later for the telecommunications class.

Next to the motivational aspects for the students the very early overview of the entire curriculum has a second benefits. Students can switch earlier to another education in case the content of the study is not what they expected or the study load or the study pace is heavier than anticipated. Before the introduction of the IEEE-course students would start with

background calculus classes and more abstract EE courses. The first electronics class with immediately visible practical applicability would start only in December (academic year starts in September).

It has to be noted that keep the students motivated we have abolished the words, math repair, math deficiency etc from our vocabulary in all teacher-student interactions. As far as the students are concerned we teach the necessary skills for their engineering career. The repair topics of the algebra/math are integrated in the course the same way as the new math they learn (e.g. 2nd order differential equations)

III. RESULTS OF IMPLEMENTING IEEE COURSE

A. Mathematical skills

For EE we have decided to fully integrate the algebra repair classes in the introductory electronics course (IEEE) starting in September 2007. The order of the topics in the math-repair-lectures is synchronized with the topics in the electronics class. For example, we teach manipulations with fractions when series en parallel networks are taught, and exponents in parallel with RC networks. We have also decided that the grade obtained for the algebra test makes up 17.5% of the final grade for the course. In addition we count the highest grade for the algebra test motivating students who have passed the first test to keep following the classes and try to better themselves the second attempt. For the 2007 and 2008 generation more than 90% of the students who passed the first test also took the second test. For the 2009 generation this was only 35%. This might be cause by the fact that the second test was shifted one week back due to the shift of the first test to the second week. This meant that the algebra was just before one of the IEEE mid term tests.

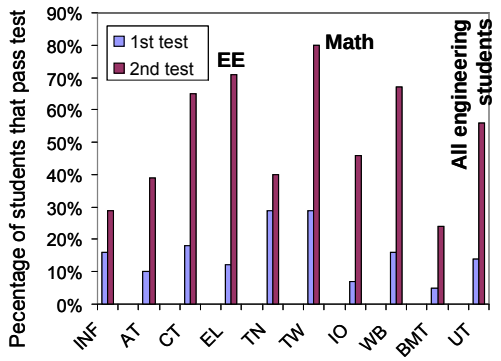

Figure 3. Improved math proviciency for 9 enineering studies (2007).

After 5 weeks the second test is taken to investigate the effect of the math repair program. In the 3 years that the math repair was fully integrated in the IEEE electronics classes more than 80% of the EE students pass this second test. This is second only to the math students. Other populations do show improved results but significantly less than the improvement for EE (figure 3). It should be noted that in 2007 we had replaced most of the algebra exercises used by the other engineering studies with examples from electrical engineering. In 2008 and 2009 we have used the exercises given in the book but we did keep the synchronization with the EE topics.

The results in the improvement of the algebra test and the attendance level in class were comparable indicating that students fortunately do make the link between generic adding with fractions to the applicability in calculating resistive networks.

Figure 4 shows the correlation between the high school math grades (perfect score 10) and the results in the algebra tests (22 multiple choice questions). 13 correct answers was considered pass. The number of correct answers increase, and repair program levels the "slope" of the graph. This is partially due to drop out of students with poor scores. But it is clear the students that scores poorly at the first test do improve after the refresher course.

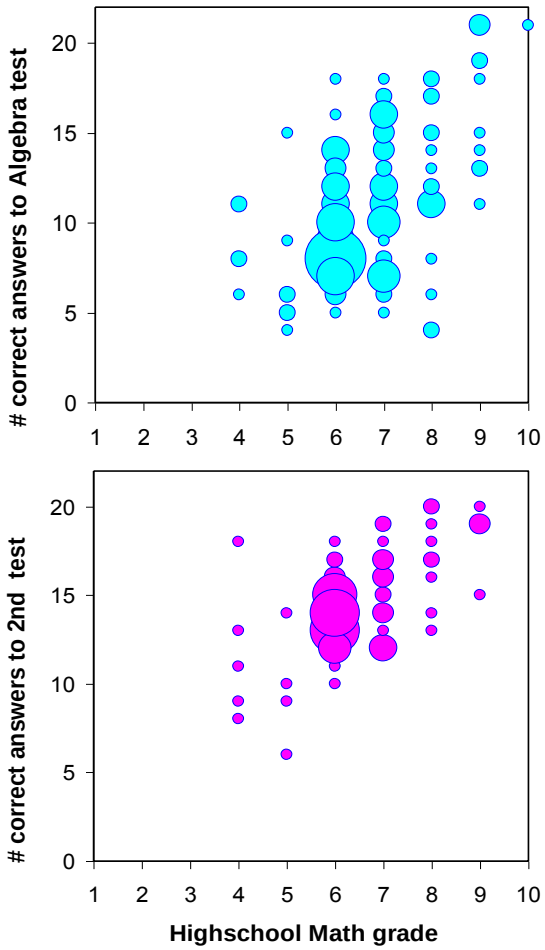

Figure 4: Correlation between the high school math grade and number of correct ansers on the algebra test (max 22) for EE students from 2007-2009. The bottom graph shows the results after the repair lectures. The number of students for the second test was lower since it was not mandatory to retake the test after passing the first test and some students had dropped out.

Figure 5 shows the grades for the first EE course (top) and the first university level math course, Calculus I, (bottom). The level of the math after the repair course (2nd test) shows a good correlation with the first EE course. However for Calculus I there seems to be a correlation with the first test. This may be due to the fact that students underestimate the calculus class

because of their large improvement in the algebra test. We can not exclude the possibility that students like the new course IEEE so much that they spent relatively little time on the parallel course Calculus I. In this case only the students that are already good and motivated, i.e. those with good high school grades and those who score good on the first test also pass this first university level match course.

From figure 4 and 5 it can be seen that high school math grades are still a good predictor of the results at university level. Although there are always exceptions as can be seen from the large band of results, a 7 in math is a good basis for the EE curriculum.

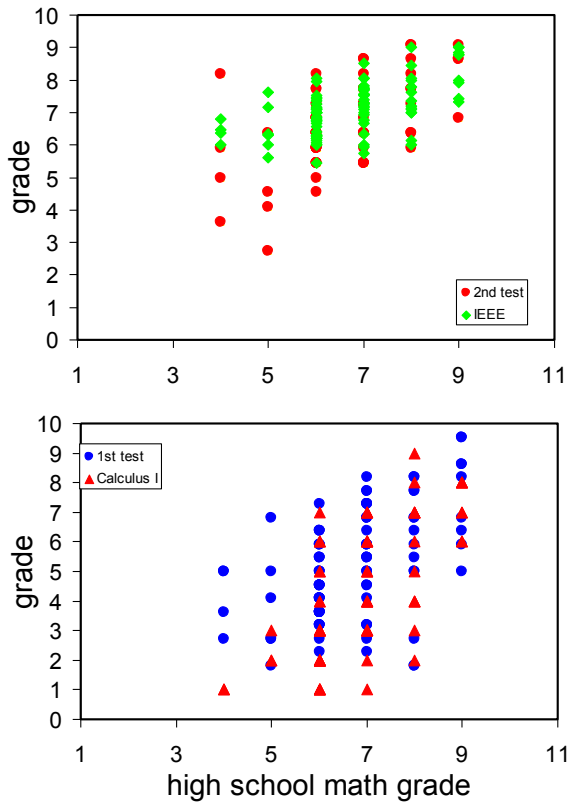

Figure 5: Top grades obtained for the 2nd algebra test (after the repair program) and IEEE, the first EE course. Bottom Grades for the first calculus class and the entrance test in algebra.

B. *Physical insight*

In our newly developed course start with an observation from nature (a capacitor can be charged resulting in a voltage) and work our way up to the describing relation. We also show a large number of physical systems that show the projection to other physical fields where similar behavior can be described with the same mathematical equations. Understanding the mass-spring system helps understanding electronic oscillations. Traditionally only in the third year of the studies these analogues are taught so that students can describe and understand physical systems with equivalent electronic circuits. We believe that in the beginning of the studies the reverse might be the case. By explicitly showing the route to the final system (starting with Hooke's law, ending in a differential equation) the students familiarize themselves in manipulating relations, lowering their dependency on graphical calculators.

During most lectures we show physical demonstrations of certain effects, RC delay related with thermal resistors and capacitors, oscillations in two communicating water vessels, breaking a glass at its resonance frequency, transmission lines with deliberately created imperfections in it etc. When physical demonstrations are not practical we show computer simulations.

C. *Work attitude and motivation*

There is a direct impulse to the students that although math might be perceived to be boring (65% of the students) it is useful (80% of the students). We have also deliberately created assignments that can be relatively easily solved if you understand the theory, but are very hard to solve when you don't grasp the underlying physics and have to do tedious calculations or derivations. The students indicate that they do indeed put in the hours, 80% of the students puts in between 90 and 115% of the study load. This shows that the students are motivated to work hard for topics that are of interest to them. This also means that present day students are not "stupid" but they are on average lazier than previous generations and an external motivator is needed instead of an internal drive.

As mentioned above we do not have sufficient data for the amount of time students spent on parallel classes like Calculus. We can say that the way we teach our course motivates students to put in approximately the study load, but if their workweek actually is increased to 40 hours remains unclear.

The course IEEE ends with a final project; the building of a solid state weather station. Groups of four students make a temperature sensor, a wind-speed sensor, a wind direction sensor and a humidity sensor. They can not all be based on the same measurement principle (capacitive, resistive). Apart from the sensing, also the data transfer and (USB) read out is part of the final product. Students indicate that they are highly motivated because of the project. Most students like the freedom they have in choosing their solution to the sensing challenge. In addition the competitive element of coming up with a more clever solution then the other groups works very motivating. There are bonus points to be gained for extra good results. The wind-speed sensor can for example be tested up to hurricane speed (see figure 5).

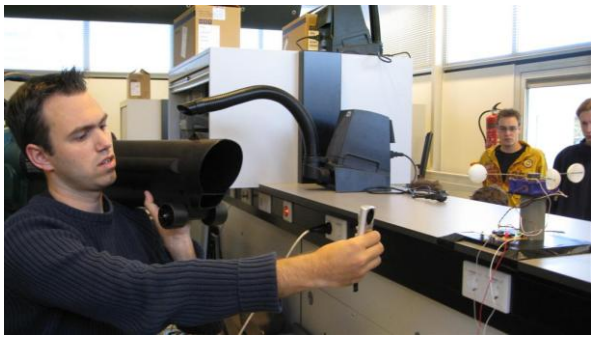

Figure 5: The final product is tested under extreme conditions

The course IEEE is intended to give the students an overview of their bachelor program and thus work motivational for the rest of the studies. Since it is an introductory course, all students who are motivated should be able to pass. We increase the chance of passing by not giving one final exam but three intermediate tests. This serves as a motivator to put in the time and as a wake-up call when the first test was underestimated. This way the students get quick feedback. For the generations 2007 and 2008 we managed to get 100% pass level for the students that remained in the EE studies. All students that did not pass went to other fields.

D. Drop outs and impact other courses

One of the intended effects of giving and early overview of the content of the entire bachelor program is that students who have chosen the wrong career are able to switch early on. For the 2007 and 2008 generations 25% of the students that start stop in the first year. 70% of the students who drop out in the first year leave before February 1st. The other 30% finish the first year and switch in the summer break. From older generations we were not able to trace back when the students stopped since only the year is recorded. It is known that there were also still students switching in the second or third year. For the 2007 generation this was not the case (so far) and we will continue to monitor this aspect.

Upon the introduction of IEEE in our curriculum the percentage of students passing the other courses in the first semester increased, but the observed effect is within the year-to-year variations.

A result of teaching a course with a lot of student-teacher interactions is that the students are motivated to work hard. A side effect is that for courses that follow in the rest of the first year the students have to learn academic skills like planning, studying without a teacher (do homework) and self motivation. The course "Network-analysis" has shown a clear correlation between the students who prepare for the exercise blocks and the grade in the exam. Students who prepare at home can use the time in class to ask questions and keep the pace of the lectures. The students that do not make homework loose the first half of the interaction time in trying themselves and have insufficient time in the end. This results in lower grades, usually failing the exam. Students who do not attend at all typically realize too late that they needed the help of the teaching assistant. They fall back so far that they usually do not even attempt the exam and have to repeat the next year.

IV. IS THE DESCRIBED APPROACH GENERALLY APPLICABLE?

The University of Maastricht attracts a lot of German students due to its border location. Their comparison of the algebra level between Dutch and German high school students summarized in table 1 indicates a higher score for some German secondary education tracks but the general lowering of math skills does not seem to be a typical Dutch problem.

Secondary school education		score
VWO B12	Dutch, math at level needed for engineering studies	48%
Grundkurs exam	German, basic math	45%
IBMathHL	International, extensive Math	55%
Leistungskurs	German, extensive Math	58%

TABLE I. : SCORES ON ENTRANCE ALGEBRA TEST OF STUDENTES ECONOMY AND BUSINESS ADMINISTRATION AT THE UNIVERSITY OF MAASTRICHT FOR SEVERAL HIGH SCHOOL EDUCATIONS [3]

The changes in our curriculum were a result a change in the Dutch school system combined with the attitude of young people to be happy with a pass grade. In a number of European countries this is a relevant topic. Motivating the students to work hard is necessary for all teachers. Some universities have the luxury of being able to select only the best students, e.g. in countries where a higher education is your only ticket out of poverty. Although the described approach might be less relevant for them, still intertwining theory, practical assignments and math education in the engineering classes may enhance motivation of the students.

V. SUMMARY AND OUTLOOK

In several European countries the numbers of electronics and electrical engineering students are dropping. By keeping the students motivated the dropout numbers can be reduced while still maintaining the same standards for the BSc degree end-terms. We have chosen to do this by integrating math and algebra lesions in the electronics classes in combination with a totally intertwining the lectures and lab courses. Our approach has resulted in a significant increase in the math proficiency test. Also the following electronics classes in the first year have an increased pass percentage. The gradual transition from renewal of knowledge that is (or might) already be known to part of the population to new topics allows us to quickly adapt to upcoming changes in the high school math and physics program. By shifting the emphasis of the lectures or include new subtopics we will be able to deliver a more homogeneous population to the teachers of the other EE classes.

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Introducing Computer Systems Related Topics in the First Study Semester

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Abstract — **To keep students interested of studying the selected study line, a new introductory course was introduced at Tallinn University of Technology for the computer systems specialization. The course is taught at the first study semester and gives an overview about problems and tasks when designing an embedded system. A simple robot platform is used for practical exercises. Feedback from the students has been very positive but some changes will be made to improve the course.**

Keywords - computer systems education; introducing specialization; hands-on exercises.

I. INTRODUCTION

Increased competition for students among universities rises an important issue – how to make "hard" study programs attractive. Computer systems specialization, taught at the Tallinn University of Technology (TUT), like many of the engineering studies can be classified as such a hard program. The main problem lies mostly in the simple fact that one must study "boring" subjects – physics, mathematics, etc. – for few semesters before being able to get to the interesting subjects – creating complex embedded systems. As a result, the undergraduate students frequently loose the motivation to study and leave the university before the end of their studies. To rise students' interest and to keep them studying, many universities have introduce so called learn-by-doing courses at the very beginning of studies. One issue still remains with such project-based learning [1] – it is hard to cover all important topics with out proper prior knowledge or the project task(s) should be rather simplified.

In order to give the better overview of the specialization and related subjects, we have created a new course at TUT targeting the first year undergraduate students. The main goal of the course is to attract the interest of these students to the specialization of computer systems and to give an overview of goals and possibilities of studying computer science and engineering in TUT. The main focus of the course is on practical work, although there are two lectures to give an overview how are related course taught for the students and problems they'll face when designing a system.

The main idea of the course is to present in a simplified manner the whole process of creating a system from raising a problem to a working prototype solution. Due to the fact that most of the first year undergraduate students have little knowledge in computer systems, the practical part of the course is implemented using Boe-Bot robots from Parallax, Inc. [2]. Robots are perfect to make an example of an embedded system because the use of a set of sensors and actuators, and a simple micro-controller to control them. These particular robots are using "Basic"-like programming language that is quite simple to understand and to learn quickly. Using Basic is a good advantage because the first year undergraduate students have different programming skills. Those with no experience can learn it fast and experienced students can easily adapt their previous knowledge. The robots also provide a lot of possibilities to study and play.

The course was taught first time during the autumn semester in 2009 and some improvements have been planned for the next time.

II. HANDS-ON EXERCISES

The main task of the practical exercises is to provide the robot with the possibility to follow a line. This can be done in various ways and it shows very clearly the existence and main nature of design trade-offs. Such an approach makes it possible to show that when increasing the functionality, the complexity of the system and a cost of it also increase.

There are four practical exercises during the course. The first exercise is an introductory one. During this class, the possibilities and area of the specialization of computer systems are discussed. We also describe the tasks of the follow-up practical classes at this point. As it was stated before, there are various ways to solve the line following problem. It is good to show the students that all of them have both advantages and disadvantages. During the introductory class we present and demonstrate four different approaches to accomplish the task. These approaches are as follows:

- programmed movements – to follow a predefined path, movements of the robot are hard-coded into the robot's software;
- controlling movements via infrared (IR) Remote Control – movements of the robot are controlled by a student with the help of a remote control devices similar to TV remote controls;

- line following using IR-sensors – movements of the robot are controlled by IR lights and sensors that are used to detect and follow black line on white surface;
- line following using CMUCam camera – movements of the robot are controlled by CMUCam camera module (following black line on white surface again).

During the last part of the introductory class, some project works of graduate students of our specialization are demonstrated and discussed. In principle, these projects are system-on-chip (SoC) examples implemented using FPGA-s. Among them is a classic "Sokoban" game [3] that has a simple graphical interface; and uses keyboard and VGA monitor for input and output respectively. Nevertheless, it is a complete system consisting of some interface controllers, a micro-controller and memory subsystems, implemented using of low-cost FPGA. It is very handy to show the students that it is possible to build a complete system based on the knowledge they'll obtain during their graduate studies. Another good demonstrated example is a mobile video compression and transmission system that is also implemented using FPGA. It utilizes Bluetooth radio link to transfer the compressed image to personal computer. This example also demonstrates what students can achieve when utilizing theoretical and practical knowledge taught at the university – building a complete system with both hardware and sofware components. These are used to build up a vision of what kind of possibilities and knowledge can be achieved at the end of the graduate studying.

The second class is more practical and covers studying the basic robot movements and practicing the control of the robot. Students are divided into groups of four members. A robot was provided to each group. During this class students learn the basics of servo motor control and various programming structures to implement the control. In order to practice with their knowledge, the main task of this class is to inline the movements into the controlling software in such a manner that the robot can follow the black line on white surface.

The robots used in the course use servo motors for their movements. This is very useful because the servos are very popular actuators to do various tasks in today's systems. It is also good that in order to control a servo, one should learn some theory of its operation. It makes the task more interesting than just switching motor power on/off. The servos use pulses of different lengths to control their rotation speed and therefore the basics of measuring time in microcontroller systems is also needed to be explained. In the particular task, this is done using "FOR... NEXT" cycle. The trade-offs between complexity of the control and functional capabilities of the system can be shown at this stage as well. For example, students can see that they can make the robot movements along the curves much smoother with the possibility to have motors running at different speeds. Together with the advantages of such a "hard-wired" approach, such as minimum hardware components and simplified control, the disadvantages can also be studied during that task. Students found out that the initial position of the robot affects the quality of the movement, especially at the end of the track were the error is accumulated. Also, hard-wiring movements into the code is very time consuming even for a small track and the same code can not be used on another track at all. On top of that, calibration of both motors is needed for every robot because accuracy of the servo motors is not perfect and this makes robots' programming even more difficult. One can not forget that battery discharge also affects the robot movements dramatically, which makes the accomplishing of the task quite tricky at the end of the class. This task demonstrates very clearly various trade-offs between system's simplicity and functionality. At this stage, it is very good also to show that in order to make the system better, even more complicated things need to be learned.

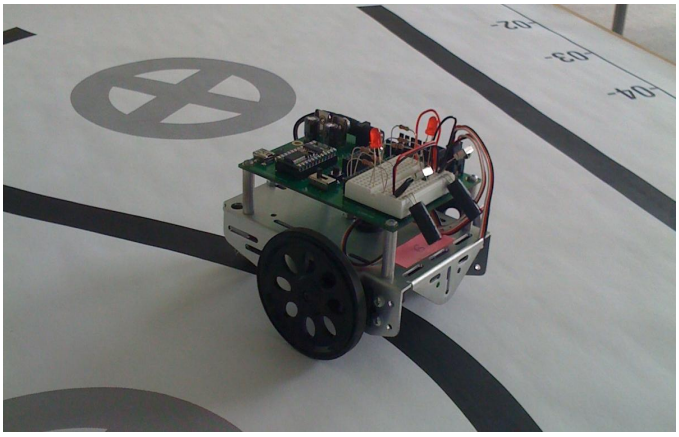

Figure 1. Robot equipped with IR Led's and receivers follows black line

The third class is about automating the movements using (IR) light emitting diodes (LED) and sensors (see also Fig. 1). The students learn the basics of feedback control and IR object detection during this class. They also study the programming interface of the IR lights and sensors. The practical task is to follow the black line with the use of IR navigation. In order to do that, they have to detect the black line on the white background and make the right movements based on the received information. A simple model of an embedded system – read sensors, make calculations and activate actuators – is introduced at this point. There are two IR LED-s and two IR sensors on the left and right sides at the front of the robot. In order to solve the task, students need to find the right frequency of emitting the IR light to detect the line correctly. The position of IR sensors and LED-s can be also modified to achieve better sensitivity.

The detection process is based on the property of a white surface to reflect the light more intensively than a black surface does. Therefore adjusting the sensitivity of the sensors, the students can make the system not to capture the reflection of the black surface and to recognize the reflection from the white surface. The task is a little bit tricky for understanding because in the case of the particular sensors used, their sensitivity can be adjusted by controlling the frequency of the signal emitted by IR LED-s that can be confusing. However this is a good example how a more complex approach can affect the functionality of a system. It can be shown that almost all disadvantages from the previous task were removed using this method and a different type of control architecture. Also, advantages of the feedback control were quite obvious and could be seen used in practice. The students were given the

possibility to manipulate the frequency of the emitted signal and to adjust also the position of the sensors. However, it was not quite trivial task because there were few sub-ranges in the given frequency range where the system worked partly or completely oppositely to the specification, which added more confusion. Nevertheless, it gave a good possibility to point out that there can always be some sort of phenomenon – interference, noise, etc. – that can affect the system's behavior. The designer of the system should be aware of these and has to know how to minimize those effects. In this particular task, the system behaves quite stable in a particular frequency sub-range and therefore this could be thought as one possible solution.

The last class was planned to allow the students to finish the previous tasks and to have a competition between robots to summarize their achievements. During the competition, the time is measured and the quality of robots' movements is estimated.

III. LESSONS LEARNED

During the first tryout of the course, several problems were identified. One of the problems arose during the second class, when basic robot movements were studied. It came out, that the first version of the track, created for robot movements, was too complex to accomplish the task within a given time period. The main reason was that the track was drawn by hand and had a big amount of curves with different and imperfect radiuses. Because of that, we had to allocate half of the next class to finish this task. We have created also a new simpler field. It has four curves that have the same radius but different angles and directions. This gives a possibility to reuse the code for similar curves and therefore to reduce the time needed to complete the task. This was tested on another group of students and almost all of them accomplished the task within a given time. This new track is intended to be used also in the next years. Most of the new track can be seen in Fig. 2 where a robot with "hard-wired" movements is following the black line.

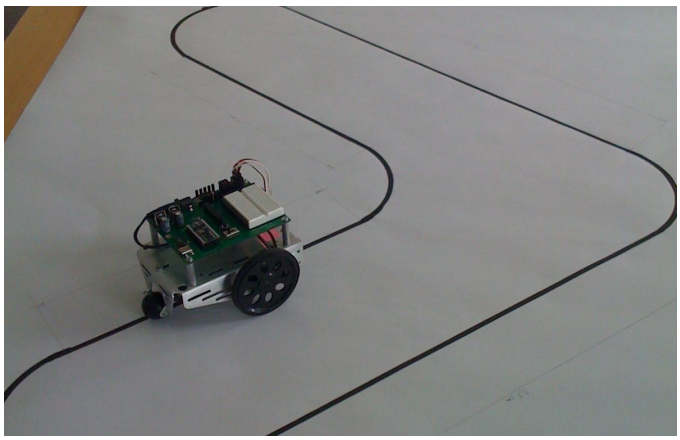

Figure 2. Robot following a predefined path along the black line

It eventually came out during the classes, that it is reasonable to make a competition at the end of every class rather that during the last class only. Because of that, the fourth class will be changed in the next years. Fortunately, in this study year, the last class could be used to complete the two previous tasks that were not finished in time because of the too complicated track. In the future, it is planned to use the last class for studying the IR remote control approach and make the competition based on that.

The competitions gave good experience for the students. In addition, students and course assistants together evaluated the implementations. Based on that, most of the students tried to identify the problems and improve their solutions. Some of them achieved even better results after improving their previous implementation. It is a good example of the fact that a working prototype can be used very efficiently in order to improve the performance of a system. This fact should be pointed out to the students at this stage.

Students gave positive feedback also during the course. The feedback came not only from the students who had taken the course but also form the students who had heard of the course. Some of them were completely excited. They appreciated very much the possibility to do something interesting in addition to study the basic subjects. Some of the students thought it was great to do something with robots. There was also a case when a student from another specialization considered switching to the computer systems specialization because of the information received from other students about this particular course.

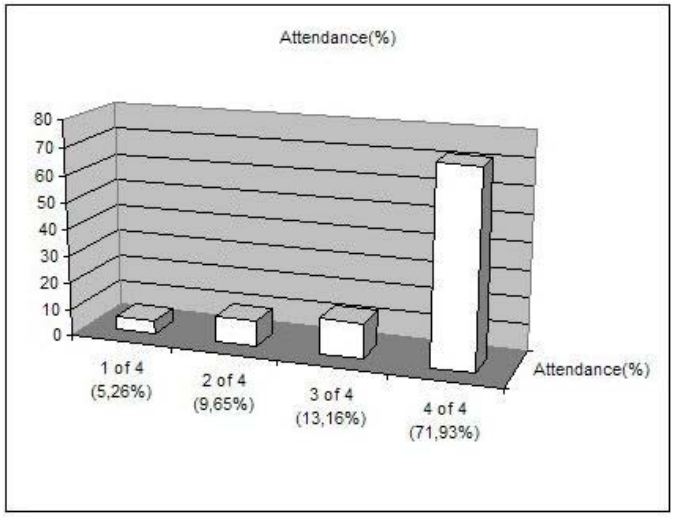

Figure 3. Class attendance statistics

The statistics of attendance is quite positive as well. As can be seen from Fig. 3, 85% of all students who took the course attended the class most of the time (three and four classes). It should be added that some of the students who attended less than 3 classes, joined the course in the middle of the study semester because of various personal reasons. It should be pointed out that because the aim of the course is to motivate the students to finish their studies in the future, the impact of the course can only be measured when these particular student will finish their studies. Therefore it is almost impossible today compare the results and estimate what will happen in future. Also, there was no similar course in the curricula before and

the course can not be compared to something from the past either.

Another advantage of the course is that it is using a quite simple and globally available robot platform. Virtually any university worldwide can obtain them for an affordable price from the company's Internet shop. Number of specific additional sensors and actuators are available for these robots to be able to modify the course with even more interesting challenges. Robots and personal computers are the only things needed for the course and they are internationally available. Because of that, it is very easy to setup this course in any university worldwide, within a little time period. The great part of educational information on the labs is given in the robot's documentation. It can be accessed on the Internet at any time free of charge and therefore considerably reduces the time to prepare the course. Of course, any other robot from any other company that offers similar simplicity to start with and possibilities to extend its capabilities can be used as well.

IV. CONCLUSION

In fall 2009, a new introductory course was introduced at Tallinn University of Technology for the computer systems' first year students to keep them interested of studying the selected specialization. The course gives an overview about problems and tasks when designing an embedded system. A simple and widely available robot platform is used for practical exercises. Feedback from the students has been very positive but some changes will be made to improve the course because some lacks were found in the smoothness of the course's time-line.

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Authors' index

A

Abramov B. p.35
Aders M. p.141
Alekseiev I. p.47

B

Bartleson K. p.119
Ben Dhia S. p.78
Benkovská J. p.64
Berekovic M. p.18,p.94
Boyer A. p.177
Bruun E. p.86
Bykov D. V. p.39

C

Chepurov A. p.47
Chertov A. p.47
E. Coersmeier p.117

D

Das C. p.1
Declercq M. p.70
Decking J. p.117
Demey B. p.74
Devadze S. p.47
Diez A. p.141
Donoval D. p.64

E

Eikel J. p.180
Ellervee P. p.185

F

Faber E. p.180
Ferreyra-Ramirez A. p.31
Fristot V. p.113

G

Gharbi A. p.141
Glösekötter P. p.117
Goettsche R. p.18,p.94
Goldman R. p.119
Gorev M. p.89,p.185
Gruhler G. p.45
Gulley J. p.84

H

Hamdi B. p. 53
Hamon J. p.113
Hanke M. p.18,p.94
Harmatha L. p.64
Hartnagel H. p.145
Holl F. p.84
Hoppe B. p.122
Huss S. A. p.127

J

Jacquemod G. p.27
Jansen D. p.108
Jenihhin M. p.47
Jeppson K. p.135
Joost R. p.98
Jutman A. p.47

K

Kharitonov I.A. p.39
Kranich T. p.18,p.94
Keren O. p.35
Kochanski T. p.84
Kostin S. p.47
Kováè J. p.102
Kuzmicz W. p.74

L

Lang M. p.45
Larsson-Edefors P. p.135
Latorre L. p.23
Levin I. p.35
Lu. Z. p.131

M

Maes H. p.70
Mahfuzul Aziz S. p.78
McLean J. p.1
Melikyan V. p.119
Molinar-Solis J. E. p.31
Müller-Glaser K.D. p.141
Munteanu I. p.12

N

Nemec M. p.64
Nouet P. p.23

O

Ocampo-Hidalgo J. J. p.31
Odjik M. p.180

P

Pesonen V. p.89,p.185
Petrosyants K. O. p.39
Peterson L. p.135
Piednoir J.-O. p.27
Pradarelli B. p.23
Prinz M. p.117

R

Raik J. p.47
Reis R. p.7
Ring Nielsen I. p.86
Rhode U. p.145
Rolland R. p.113
Rucinski A. p.84
Rößling G. p.131
Rybár J. p.102

S

Salm C. p.180
Salomon R. p.98
Schulze J. p.45
Schuster T. p.12,p.94
Schwalb T. p.141
Šebok J. p.64
Sicard E. p.53,p.78,p.177
Shoufan A. p.131
Stuchlíková L. p.64,p.102
Schwelgengräber W. p.98
Svensson L. p.135

T

Tammemäe K. p.89

U

Ubar R. p.47

V

Vagedes S. p.117
Van der Heijden F. p.180

W

Wessels K. p.117
Wood T. p.119
Wuttke H.-D. p.47