

# EUROCHIP-EUROPRACTICE

## 20 Years of Design Support for European Universities

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**Abstract**—The EUROPRACTICE CAD and IC Service has enabled over 650 European universities and research institutes to enjoy access to advanced microelectronics-based design tools and prototyping services over a period of 20 years. EUROPRACTICE services have been used by virtually all of the major universities and research institutes in Europe engaged in microelectronics-based design to underpin their training and research activities.

**Keywords**—CMOS, VLSI, CAD, EDA, deep submicron, Microsystems, training

### I. INTRODUCTION

In 1989 the European Commission launched the VLSI Design Training Action in order to help European universities train students in VLSI design. The objective was to select 50 universities and provide them with a lecturer post, modern IC CAD tools, low cost IC prototyping and an IC tester. A Service Center, called EUROCHIP, was established to select, negotiate, coordinate and provide these services. In 1995, the Action ended after about 400 European universities had taken up IC design. In 1995, the EUROCHIP project was followed-on by the EUROPRACTICE project, funded by the EC. The goal was to continue the offering of CAD tools and IC prototyping services to the European universities, extend these services to include Microsystems, and also to expand the service to offer industry (mainly SME's and start-up companies) low-cost MPW IC prototyping services plus a service for low volume IC fabrication. Today, after 20 years of successful continuous operation, about 650 European universities and research institutes are using the service and in addition about 200 companies have been able to have their IC designs prototyped and produced in volume.

### II. EUROCHIP (1989-1995)

The Service Center EUROCHIP was established in 1989 in order to provide 50 selected European universities with industrial CAD tools for IC design, MPW prototyping and a tester. The Service Center EUROCHIP was set up by a consortium of experienced national centers: IMEC in Belgium, RAL in UK, DTU in Denmark, GMD in Germany, CMP in France and later on also CNM in Spain.

This consortium joined individual forces and started a pan-European service, unique world-wide. The call for 50 selected universities got a huge response and in addition to the 50 selected universities, another 68 universities joined on a pay-as-use basis. This was the first time that universities across the whole of Europe could get access to the same set of CAD tools and IC technologies. This was the basis for the start of true pan-European microelectronics education support. The service started off by selecting 4 CAD packages and 3 IC technologies (3 $\mu$ , 2 $\mu$  CMOS). The EUROCHIP Service organized training courses in modern IC design. Standard cell libraries and design kits, fitting the CAD tools, from the foundries were made available. As a result the first designs from the universities were prototyped in 1990.

Over the 6 years of EUROCHIP operation, the Service continually grew and expanded its offering in CAD tools and IC technologies and by 1995 about 400 universities were making use of the Service.

### III. EUROPRACTICE (1995 – TODAY)

In 1995, the European Commission launched a new call for a continuation of the service for universities but also for an extension of the fabrication service to small and medium companies. As a result of the call, a new consortium was formed with some industrial partners (that had offered for a few years a similar service to industry – ChipShop). The new service was called EUROPRACTICE and was coordinated by experienced partners: IMEC in Belgium, RAL in UK, Fraunhofer IIS in Germany, Nordic VLSI in Norway and Delta in Denmark. The service offering was significantly extended. A wider range of CAD tools were offered including tools for MCM and Microsystems design. The IC technology portfolio was expanded with more advanced IC technologies, for example 0.8 $\mu$  down to 0.25 $\mu$  CMOS, and also BiCMOS, SiGe and high voltage options were introduced. In 2000, the EUROPRACTICE service had reached such a level of maturity in its offering towards companies that the EC decided to only continue to fund the service for the universities. Companies could further make use of the service but only on a fully-paid financial basis. Consequently the consortium changed to reflect the new business model and since 2000 the

EUROPRACTICE IC Service is coordinated by IMEC in Belgium, RAL in UK and Fraunhofer IIS in Germany. Today, after 20 years of continuous operation, about 650 European universities and research institutes are EUROPRACTICE members. The level of complexity of design methods, CAD tools and IC technologies has increased dramatically and will further increase as new design methods and technologies emerge. EUROPRACTICE has successfully helped universities to increase their design capabilities by offering affordable access to the most modern CAD tools, affordable access to advanced (65nm) IC technologies and coupled train-the-trainer courses in MEMs and deep-submicron design.

More than 650 institutions in 44 countries close to Europe currently have a common design infrastructure which is an ideal basis for collaborative research projects. Additionally, designers can quickly become productive when moving between universities or from university to industry.

Although EUROPRACTICE is an EC-funded project, 85% of the project turnover is from the universities. This makes the project unique has contributed to its longevity.

#### IV. EVOLVING REQUIREMENTS

European academia and has always had a strong capability in Microelectronic design, and EUROCHIP/EUROPRACTICE has provided access to the commercial design tools and processes required to develop those capabilities to the fullest.

The microelectronics design sector changes rapidly, and the EUROCHIP/EUROPRACTICE offering has had to constantly evolve to reflect these changes in order to remain relevant.

The original EUROCHIP scheme was entirely dedicated to IC fabrication. All CAD tools and processes were selected to provide an integrated flow to implementation and test. To this day, this integrated flow from design tools through design kits to IC fabrication is the mainstay of the EUROPRACTICE one stop service.

The mix of design types has changed over time. The emergence of programmable devices for teaching and research offered a viable platform for a class of digital designs that previously could only be realised on custom ICs. At the same time, the number of mixed signal designs and complex digital systems has increased, reflecting the strength of European industry and universities in areas such as communications and automotive electronics.

Today's EUROPRACTICE is still built around the strong central flow, usually defined by the reference flow described by the foundry, e.g. TSMC. Different combinations of tools can be used within the flow depending on the preference of the university, and all possible combinations are supported by EUROPRACTICE.

A wide range of tools not dedicated to IC fabrication are now part of the EUROPRACTICE portfolio. These are tools cover a wide range of areas, for example high level system design, PCB layout and analysis, and even device modelling (Technology CAD).

#### A. IC Design

The aim of EUROCHIP/EUROPRACTICE has always been to stimulate the adoption of new techniques and technologies. During EUROCHIP, this was done by making integrated flows available and using multi project wafers to reduce fabrication costs. With modern complex technologies, additional stimulation activities were required.

For Deep Sub-Micron (DSM) technologies of 90nm and below, the high cost of manufacture was a barrier for many universities. Even after a silicon subsidy was applied, the cost was not affordable for university projects. Aware that the technical demand was there, and that price was the problem, EUROPRACTICE was obliged to solve the problem. The solution was sub divide the minimum block size offered by the foundry, and allow universities to buy one of more sub blocks. After introducing this program, dubbed "mini@sic", there was a distinct increase in the number of designs submitted for the eligible technologies.

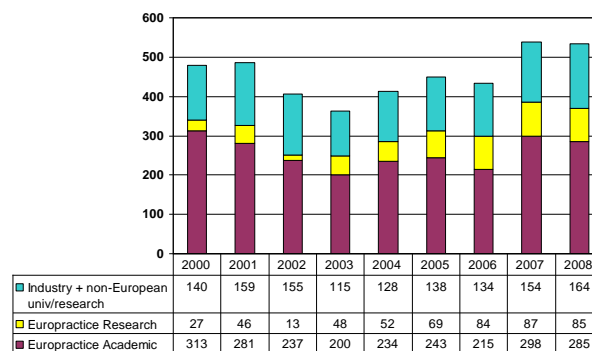


Figure 1. Increase in prototyping due to mini@sic

After the introduction of the mini@sic program, it was clear that there were still some universities who were unable to contemplate designing with these DSM technologies. The reason cited for this was a lack of training on the specific problems of designing at or below 90nm. This problem was addressed by the EC training action, IDESA that addressed these issues, and gave practical tutorials illustrating DSM using tools and technologies from the EUROPRACTICE portfolio. This tightly coupled training action is only possible due to the commonality of tools and design kits across Europe.

## B. FPGA Design

The early MPW runs of EUROCHIP featured large numbers of digital circuits, but by 1994 a new platform for digital design was beginning to emerge, the programmable device.

At first, these programmable devices whose software ran on low cost PCs rather than expensive UNIX workstations, were seen as a replacement for university tutorial sessions that had traditionally employed breadboards, with perhaps the possibility of some small student projects using the largest available devices. EUROCHIP introduced software and hardware from the programmable device vendors Altera and Xilinx to the portfolio but also introduced a wider range of PC based software to allow the fullest possible exploitation of the technology.

The programmable devices that required a separate hardware programmer gave way to the reprogrammable FPGAs that we know today, and sizes ramped up from a few thousand logic gates to tens of thousands and eventually millions. Steadily more and more digital design projects became feasible on FPGA, and digital ASICs were less essential for all but the most challenging projects. The software required to create designs on FPGA became more sophisticated as these large digital designs faced many of the same problems that large digital ASICs did. EUROCHIP sought to provide FPGA capable tools from vendors already within the portfolio to provide as much overlap between existing IC holdings and new FPGA holdings. Where available, all interfaces between existing tools and FPGAs were also made available.

Now, EUROCHIP users can implement a 64 bit microprocessor in an FPGA on a low cost development board using the same synthesis and verification environment used for IC design. Modern FPGAs can offer a quick implementation of an algorithmic or C based design, or a prototype of a more complex system.

## C. MEMs

Micro Electrical Mechanical systems (MEMs) was a discipline largely confined to the laboratory at the beginning of EUROCHIP. In EUROCHIP, the MEMs activity that was growing in Europe was supported first by the introduction of tools for MEMs design. Where possible, these tools were selected to complement the existing IC layout tools available, so that universities could build upon their existing expertise and save the cost of buying additional layout tools.

The initial adoption of MEMs technology outside of a core group of universities was not as rapid as had been hoped, despite access to design tools and fabrication.

The obvious solution was to reuse the thinking from the IC history, and launch an integrated flow including a Multi Project Wafer service for MEMs. Today universities can

submit designs to MPW runs on the Tronics MEMSSOI and three different processes from MEMSCAP. The current MEMs MPW and software offerings are already larger than the initial IC offering of EUROCHIP.

One of the challenges of designing MEMs is that detailed knowledge of the specific processes is required in order to obtain maximum design efficiency. To this end, the EC training action STIMESI was created. The original project ran between 2006 and ended in 2009. Short courses were offered in a wide range of MEMs areas at locations across Europe. Recently a second phase of the project was announced, this time focusing entirely on the MPW and software available via EUROCHIP in order to address the widest possible range of universities, and give them the best possible chance of exploiting what they have learnt.

## D. System on Chip

As the geometries of ICs have shrunk, it has become practical, and for many applications, highly desirable, to incorporate one or more general purpose processors onto a die with other digital logic.

A major barrier when producing an SoC is the selection of a microprocessor. During the early phases of SoC adoption, EUROCHIP secured processor IP, along with the right to use that IP in a non commercial design with no licensing fee. This approach, while appropriate at the time was somewhat restrictive, in that universities were limited to a single architecture and a small selection of processes. As time moved on, EUROCHIP was able to support open standard busses and processor IP that could be synthesised for any process.

A recurring theme of these projects is that cost is always a consideration for universities. It can be difficult to justify the cost of creating an ASIC to demonstrate a working SoC, even for a project where the architecture of the SoC is the primary focus. As with digital ASICs before, the solution became available with high density FPGAs. EUROCHIP has supported SoCs on FPGAs since their earliest days, including the brief phase when FPGA manufacturers implemented fixed processors on the FPGA die. Ultimately synthesized processors became the best solution, and the rich library of system IP available on FPGAs makes this an excellent companion platform to ASICs for SoC development and research.

As large scale SoCs became viable, interest in system modelling also increased. Where previously this had largely been undertaken as a separate exercise unconnected to the implementation flow, the examination of architectural trade-offs between hardware and software, between single versus multi-core and in the optimal deployment of complex bus hierarchies has become a critical part of the design process. The introduction of system modelling languages like SystemC and System Verilog, and the tools to use them has attracted yet

another type of user to the scheme, hardware and software aware, but distinct from both.

Many of the systems designed using these languages are destined to remain theoretical, but a full path down to silicon or FPGA exists if required.

#### E. Embedded Software

Early systems that included software most often had either a microcontroller or a small microprocessor. In either case, it was quite feasible to write microcode by hand, or implement an assembler for the limited instruction set.

Modern SoCs run much more sophisticated code; they are far more likely to be running a video processing algorithm or TCP/IP stack than acting as a simple job scheduler. Developing the system software to run on these SoCs requires a more complex programming environment. In recent years, EUROPRACTICE has introduced embedded tool suites based on the Eclipse tools, as well as the ARM RealView developer suite. Now designers can develop not only the systems software, but also the application software, using compilers in a fully integrated development environment, with a comprehensive range of software IP.

In industry, it is common practice for the development application software for SoCs to begin as early in the design process as possible. Universities have embraced these tools for creating Virtual Platforms or Programmer's View models to give training on embedded systems programming, or to allow multi-disciplinary teams to work together on a mixed hardware/software project.

For some applications, there is no ideal processor available for a specific task. In this circumstance an Application Specific Instruction set Processor (ASIP) can be developed using tools within the EUROPRACTICE portfolio. Once the processor is specified, a full hardware description language can be generated and passed to a standard synthesis tool to create a gate level description. In addition, a full set of programming tools can be derived from the same source, giving an assembler, debugger and c-compiler unique to the processor.

Clearly these processor development tools are of interest not only to the IC design community, but also to those interested in teaching and researching processor architectures, so the EUROPRACTICE community continues to diversify.

## V. MEMBERSHIP MODEL



Figure 2. Current EUROPRACTICE members

The current EUROPRACTICE membership stands at more than 650 institutes in 44 countries close to Europe. The laws and business practices in these countries are all different; some are in the EU while others are not. Most of the countries have a local office, or appointed representative, of the commercial vendors that supply the software and device manufacturing capabilities to the scheme members. Despite this, all goods and services are supplied through the EUROPRACTICE consortium, and European academics have a single set of prices and terms that apply to all.

All universities sign up to the same Membership agreement, the same End User Agreements (EUAs) for software, and the same Non Disclosure Agreements (NDAs) for access to foundry design kits.

This is achieved by, where possible, having each university join the scheme as a single member, rather than one membership per department. This gives the university cost savings on membership and maintenance fees, but perhaps more importantly enables the commercial vendors to perceive that they have a corporate level account with the member university through the scheme. The scheme interacts with the commercial vendors at either head office or European office level, to ensure that the same terms and conditions can apply across such a wide and diverse region.



## VI. OPEN EUROPEAN INFRASTRUCTURE



Figure 3. EDA Software Partners

As the beginning of EUROCHIP, the model was to provide design tools, design kits and access to fabrication as a single unified flow that was guaranteed to be compatible. This model can be supplemented by coupled training activities to provide a complete solution for Microelectronics based training.

Many things have changed since EUROCHIP, but this classic model still holds true today. Design kits are more complex, and design tools are perhaps more likely to come from multiple vendors in a single flow, but the basic model still holds true. Today's deep submicron flow follows this model, with IDESA, an allied, but separate, project providing the training. For MEMs, the training is available from STIMESL.

For the emerging photonics area, the route to fabrication is not within the EURO PRACTICE project, but via the ePIXfab an EC project to provide photonics MPW services. The tools available via EURO PRACTICE have been aligned with the requirements of this MPW service to provide a seamless flow for users.



Figure 4. Foundry and Design Kit Partners

The more established IC field has many options for fabrication, including other MPW services and direct foundry access. As often the decision on which technology to use is

heavily influenced by collaborating partners, or specific technical advantages, EURO PRACTICE has always maintained good links with other fabrication providers, and cooperated with them to ensure compatibility between EURO PRACTICE tools and their processes.

Similarly the EURO PRACTICE MPW service is open to all. While European academic members benefit from a silicon subsidy, it is possible for universities to gain unsubsidized access without becoming a member, as can commercial companies. There is no requirement to use tools sourced via EURO PRACTICE to submit designs to the EURO PRACTICE MPW service.

EURO PRACTICE always strives to maintain open interfaces in the design tools and design kits that it provides. The commercial design tools and design kits supplied are exactly the same as those provided to industry, so if a design kit contains data for tools not available via EURO PRACTICE that data will be supplied. All EURO PRACTICE tools contain the same interfaces as when supplied to industry, so that a university is free to use design tools supplied by EURO PRACTICE in the same flow with design tools from other sources, even tools developed within the university.

## VII. INDUSTRIAL IMPACT

Microelectronics is an important industry for the European economy, and keeping that industry healthy in an increasingly competitive global marketplace is a significant challenge. European universities are a vital part of the supply chain for European industry, both through the opportunities created by university research and the supply of highly skilled graduates that are the raw materials for future industrial success.

EURO PRACTICE provides universities with access to the same tools that are used in industry, the same design kits that are used in industry and the same processes that are used in industry. This common platform ensures that the skilled graduates being produced are far more immediately useful to industry, and that collaborative projects between universities and industry have a common basis on which to work.

To further facilitate cooperation with industry, all EURO PRACTICE MPW services are open to industry for prototype and small volume production.

EURO PRACTICE software is provided under a strict non commercial use policy, but by special arrangement, a university can apply for an extended license that, subject to approval, allows a collaborative project to be undertaken with an industrial partner.

In order for European industry to prosper in the future, it will need to continue to exploit emerging technologies as early and as efficiently as possible. This has driven EURO PRACTICE and its university customers to diversify into areas such as

photonics and microfluidics. By making tools and processes in these areas available as early as possible, EURO PRACTICE helps European universities be in the best position to establish industries around these new technologies.

#### VIII. THE FUTURE

The EURO PRACTICE scheme has always striven to remain as close as is practical to the leading edge of industry standard design flows, tools and processes. For this reason we are able to look into the near future with some reasonable confidence.

In the IC fabrication area, we will have already seen university access at the 65nm node. We would expect that within twelve months, it should be possible for universities to gain access to 40nm technologies. In accord with EURO PRACTICE principles, this technology would be available as a mini@sic process to allow affordable access to these advanced processes.

Photonics has emerged as an exciting area for designers in recent years. Although still in its early stages as a design discipline the EURO PRACTICE portfolio already has tools to perform optical analysis and tools that allow for the layout of photonics structures as custom structures or as standard structures from a library of optical components. These tools will complement the MPW service via ePIXfab.

New tools for C based design of circuits have recently become available, and further tools in this area will follow.

In increasingly important areas such as BioMEMs, universities are well placed to take advantage of the diverse EURO PRACTICE offering when designing heterogeneous systems. In addition to IC and MEMs design tools and fabrication options, EURO PRACTICE also has design tools for PCB design, including System-in-Package (SiP).

An interesting new development in the tool area are tools for evaluating the impact of design decisions on a final chip at a very early stage of the design process. Designs can be

evaluated for traditional criteria such as power, but for the first time they can be evaluated on cost to manufacture. These tools will show the full cost of fabricating a chip, the likely yield and the number of devices that must be produced to achieve a given price point. These tools have a very direct application for those who produce large numbers of chips for large research projects, but also afford a great opportunity to illustrate the economic and business aspects of IC design as part of a modern curriculum.

#### IX. CONCLUSION

European Universities and Research Institutes have affordable, one-stop access to the best design tools, design flows and processes normally only available to the largest multi-national corporations. European fabless design companies have easy access to prototype and small volume fabrication, packaging and test. This common European microelectronics-based design infrastructure facilitates cooperation. Graduates entering industry from European universities are more appropriately trained and are more able to meet future challenges of industry.

As the requirements of European academia have evolved, so have the offerings of the scheme. The areas of study have diversified, and the EURO PRACTICE user community of today is far broader both geographically and thematically than could have been envisaged at the beginning of EUROCHIP.

#### ACKNOWLEDGMENT

The collaboration of all EUROCHIP and EURO PRACTICE project partners with the authors of this paper is gratefully acknowledged.

The European Commission is acknowledged for its continuous support under several Framework Programs FP2, FP3, FP4, FP5, FP6 and FP7.