Industrial Testing Education at Undergraduate Level: A Datasheet and Diagnosis Based Labs Approach

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Abstract—**This paper addresses industrial testing education. This work is done in the context of a French network (CNFM) which provides an access to industrial test equipment to academic people. The actual shared resource is a Verigy V93K System-on-Chip (SoC) tester platform. Undergraduate students often use digital integrated circuits (IC) in their labs and refer to the datasheet without a deep understanding of the device electrical and timing parameters. In our lab-based training, the students are guided to rediscover the role of a component datasheet, through the development of a test program. They become familiar with industrial test environment and mass production testing concepts such as test flow, test limits, parameters margins, and so on, that bonds the design, the manufacturing and the test of an integrated circuit. In addition, labs have been oriented toward the diagnosis of faulty behaviors. To do so, a fault-free circuit is first implemented into an FPGA that emulates the real circuit behavior. The design then allows configuring faulty circuits, including stuck-at faults or timing faults. Diagnosis bases are then addressed this way.**

Index Terms- Test, Testability, ATE programming, Faulty behavior, Diagnosis.

I. INTRODUCTION

This paper describes the French experience in the education of undergraduate students to industrial testing and diagnosis of integrated circuits (IC) using a lab oriented approach.

In the industry, the mass production testing is a specific environment which requires skilled technicians and engineers to handle the test equipments (tester, handler and prober) performing the automatic verification of dies on wafers and the final test of packaged parts. Technicians have key roles as they are in charge of the test equipments setup, the control of the production, the retrieve of test results and the first debug actions in case of sudden yield loss. Due to the lack of know-how and specific hardware resource in the academic environment, industrial testing is not well addressed while in the same time, microelectronic industry offers many opportunities in this field. In order to fill this gap, the National Test Resource Centre of CNFM (so-called CRTC) team has developed dedicated labs at undergraduate level that allows students to get familiar with the main concepts of production testing and equipment usage.

The CRTC has been created to respond to the industrial demand in engineering curriculum with Design & Test competences [1]. CNFM (Comité National pour la Formation en Microélectronique) is a public organization that federates academic and industrial partners for the purpose of education in Micro and Nano-electronics [2]. CNFM focuses on making heavy educational resources such as professional CAD tools, clean rooms, or industrial test equipments available for common use, by all French universities and industrial partners. Considering the huge cost of up-to-date IC testers, the policy of CNFM was to setup a single test center for all the French academic centers. So in 1998, the University of Montpellier was chosen to implement the CRTC. In 2003, after a 2-year long project, students from Europe were able to take control of the tester for remote labs [3]. The technical platform benefits from the competence of more than 25 people (researchers and professors) from a research laboratory (LIRMM, www.lirmm.fr) internationally renowned in the field of design and test of integrated circuits and systems. Research projects include DFT and BIST for digital, analog and mixed-signal circuits and design and test of integrated MEMS. Since 2006, the CRTC team includes a test engineer who manages all the technical support to users and develops training materials [4].

II. LAB ENVIRONMENT

A. Network

As CRTC first duty was to share the tester resource between different universities in France and Europe, a training environment was originally setup which allows a remote access to the test system as presented in fig. 1. In this configuration all test resources (licenses and tester) are installed in Montpellier.

As only one online session can be available at a time because of the unique hardware resource, the students work first on simulator (offline mode) and use the tester when their test program is ready for the debug session.

B. Test resources

The CRTC tester is a V93K from Verigy®. Verigy is one of the four major test equipment manufacturers in the world and is well represented in the European microelectronic industry.

Fig.2 illustrates the basic elements that compose the Automatic Test Equipment (ATE). The main part is the testhead. It can host up to 18 boards (Pin Electronics) for a maximum number of 512 digital pins (or channels) based on existing 32 channels boards. Programming is performed using a regular computer running dedicated software under Linux. The communication between the testhead and the computer is an optical GPIB link.

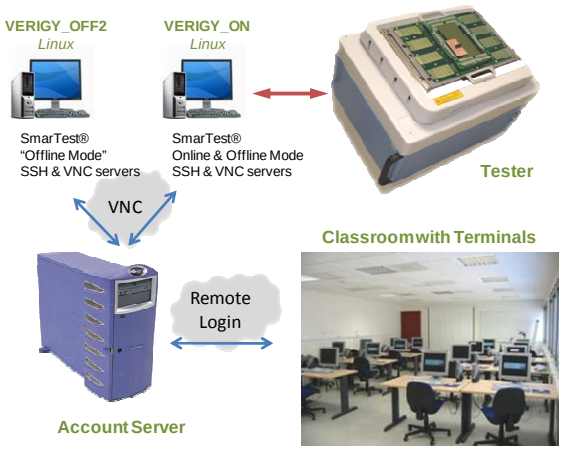

Figure 1. CRTC labs environment

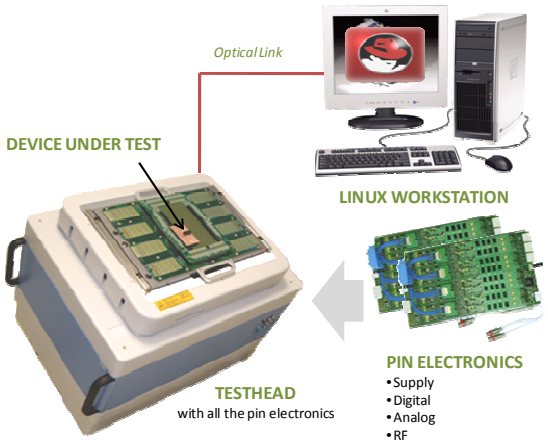

Figure 2. Industrial tester main components

VNC technology offers an easy way for the distant access to the tester. We promote this approach in the context of distant learning as the same desktop can be shared between users. This capability brings a strong interactivity between students and teacher [5]. The testhead is equipped with power pins, digital pins and mixed-signal resources as summarized in table I.

TABLE I. CTRC TESTER CONFIGURATION

Board	Ressource Type	Qty	Channels / board	Specifications
PS3600	Digital	1	32	3.6GSps / 64Mvec memory
PS800	Digital	1	32	800MSps / 64Mvec memory
AV8	Mixed-Signal	1	8	24bits / 200kSps for Audio 14bits / 65MSps for Video
MSDPS	Supply	2	8	-8V to 8V / 2A

III. LAB PROGRAM

At undergraduate level, students are using electronics components daily, and have become familiar with their data sheet without having any idea on how this latter has been constructed. One objective of the lab is to let them rediscover the role of the circuit data sheet and how its behavior and parameters are verified. As the only prerequisites to test an IC are the basics of fundamental electronics, they develop the test program to understand how electrical and timing parameters are measured using an industrial tester.

Most of the time, students are surprised when a device which works in design simulation doesn't operate properly once manufactured. They omit that the manufacturing steps are various and technically complex and can introduce defects in the ICs. So, a second objective is to initiate them to the detection and diagnosis of faulty behaviors.

A. Part 1: Study of the Datasheet

The device under test (DUT) used for the labs is a simple 8-bit shift register (74ACT299) which is in use in professional trainings for years. From the datasheet specifications, the students are guided to understand the information displayed in the different sections (DC Parameters, AC Parameters, …) and how this data relates to the test program. The operating conditions will represent the test conditions in temperatures and voltages. The device pin function and the truth table, respectively available is the datasheet are strategic data to allow the students becoming familiar with the device behavior.

In order to check the device behavior according to its truth table, the students have to create a test pattern (also called test vectors) to stimulate the chip. This test vector consists on applying signals on the inputs and on verifying if the data collected on the outputs are as expected. Doing so, they learn how to translate the information from the truth table to a test vector. Table II, shows an example of a test pattern where a '00000001' byte is first parallel loaded into the register and then 8 shifts right follow to move the '1' through all of the 8 I/Os pins. In this table, '0' and '1' represent the data applied by the tester to the device input pins, while 'H' and 'L' represent the expected device response.

TABLE II. 74ACT299 PARTIAL TEST PATTERN

	Pin	MR	CP	S0	S1	DS0	DS7	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	Q0	Q7
# Cycles	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
	2	1	1	1	0	0	0	L	**H**	L	L	L	L	L	L	L	L
	3	1	1	1	0	0	0	L	L	**H**	L	L	L	L	L	L	L
	4	1	1	1	0	0	0	L	L	L	**H**	L	L	L	L	L	L
	5	1	1	1	0	0	0	L	L	L	L	**H**	L	L	L	L	L
	6	1	1	1	0	0	0	L	L	L	L	L	**H**	L	L	L	L
	7	1	1	1	0	0	0	L	L	L	L	L	L	**H**	L	L	L
	8	1	1	1	0	0	0	L	L	L	L	L	L	L	**H**	L	**H**

In an industrial context, test vectors are automatically generated by CAD tools called ATPG (Automatic Test Pattern Generators), using an approach based on fault simulation. In this training, as the device is simple, students are requested to write a test vector themselves. It is crucial that they understand how the IC behaves before focusing on the electrical and timing parameters. Moreover, it is the logical order to develop

and execute a test program. As a matter of fact in mass production, this order allows detecting gross defaults and rejecting defective parts before performing any measurement.
Most of the time, students do not realize the importance of electrical and timing parameters in the design of circuits, in relation with process technology scatterings and the consequence regarding components compatibly when mounted on printed circuit boards (PCB). On the other hand, the definition and role of the input and output voltages (V_{il}, V_{ih}, V_{ol}, V_{oh}), the leakage currents, dynamic output and quiescent supply currents parameters are usually well understood as they use them regularly during experimentations at school. Verifying them on an industrial tester simply consists in applying the Ohm's law, i.e. forcing a current to measure a voltage and vice-versa; and programming the test equipment accordingly.
A majority of students ignore the importance of timing parameters like operating frequency, set-up time (t_{su}), hold time (t_{hd}) and propagation delay (t_{pd}) in sequential circuits. During labs, they learn the meaning of these specifications and how they can be measured on tester using a reference signal, like the master clock of the device.
Today consumer electronic products are relevant examples to help them understanding the overall relation between circuit design, manufacturing, test and these parameters. Like in mobile phone applications, the measurements of the current consumption in operating stand-by and quiescent modes allow verifying the battery duration in call and idle modes.
Once the students are comfortable with all these concepts, they are requested to extract electrical and timings information from the datasheet and to implement a suitable the test program.

B. Part II: Introduction to Indutrial Testing

The electronic resources available in the testhead are presented first: the driver that applies input signals to the DUT; the comparator that captures output signals and compares the result to the expected values specified in the test vector; and the programmable load to source or sink currents to or from the DUT. A dedicated instrument allows performing precise DC voltages and currents measurements. All these hardware resources are available for each single channel which authorizes parallel or concurrent testing. A good knowledge of the tester hardware helps the students understanding how an electrical signal is created by the combination of a voltage referring to logic state and a timing information (waveform).
Next, the software environment is introduced. The test program is developed into a dedicated tool called SmarTest®. Once, the students have defined the levels (Vil, Vih, Vol, Voh) the timings for all pins and written the test pattern, they are ready to implement a test flow with all the functional and parametric tests to be executed sequentially.
Fig. 3 illustrates the developed test flow. The strategy behind test flow implementation is addressed here.. When the result produced by a single test is "Pass", the next test in the flow is executed. Otherwise, it goes to a virtual waste basket called "bad bin" and then the program execution is stopped. Sometimes, when a test fails, another test is performed. For instance, a microprocessor device failing a 1GHz test which will be tested again and may pass a 500MHz one. The test flow ends on a "good bin" indicating that the device matches its datasheet parameters. A functional test is usually performed first, then the parametric ones (static and dynamic parameters) where the program developer has set as test conditions the values previously extracted from the datasheet.

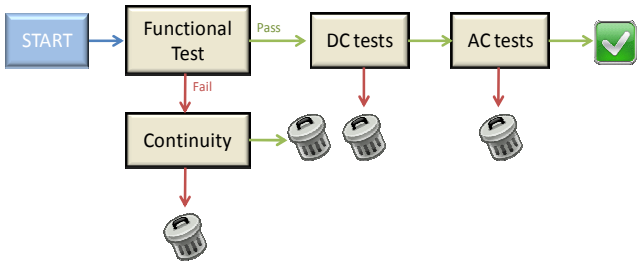

Figure 3. Example of a simple 74ACT299 Testflow

C. Part III: Analysis of Test Results

The functional test is a "go/nogo" test so that the outcome is just a "Pass" or "Fail" result. When focusing on parametric test results, it may not be straight for students to understand the meaning of the measured values. For example, the V_{il}/V_{ih} test of the 74ACT299 requires an initial setting, say 0.8V for V_{il} and 2V for V_{ih} on all inputs. The output of the characterization test provides actual V_{il} and V_{ih} values, say 1.2V and 1.4V. These values show the functional margins of the device and the robustness of the design towards the manufacturing as it means that the device still functions when 1.2V is assigned to a logic state 0 and 1.4V to a logic state 1.

Once the students get familiar with the analysis procedure using electrical parameters and the concept of margins, the timing results are analyzed. If we measure a 9.5ns propagation delay between the clock rising edge and an output of the circuit, while the datasheet specifies a delay of 12.5ns, then we can conclude that the device operates slightly faster than the guaranteed limit.. This margin improves the production yield because it accommodates some level of process shift.

D. Part IV:Initiation to Faults Detection and Diagnosis

As the device used for the training is obviously a good one, it is not possible to confront the students with failing behavior. Our approach was to implement a gate-level copy of the circuit into an FPGA that can be altered to inject either stuck-at faults (node stuck at '0' or '1' logic state, or extra delays) to emulate real failures.
The 74ACT299 device has been coded into a structural VHDL module that represents the very same circuitry as the original integrated circuit. Additional lines and gates have been inserted allowing the configuration of faulty behaviors…

The targeted FPGA is a Xilinx xx available on Digilent Nexys development board. In our setup, the FPGA I/Os are directly connected to the ATE channels, while the Nexys board is

externally supplied (see Fig. 4). The development board features switches, buttons and a 4 digits 7-segments display that have been used to develop a simple user interface that allow the teacher to easily select the operating mode or the emulated circuit (fault-free mode, stuck-at fault mode, or delay fault mode). Due to the limited number of switches, a reduced number of nodes have been selected to insert stuck-at faults and additional propagation delays. Delays are also selectable in a range from 3ns to 40ns. The choice of the node for fault injection has been made allowing various diagnosis difficulty levels.

Figure 4. The Interface board and FPGA board connected to the testhead.

From educational point view, this approach is very efficient as it allows the teacher to introduce various faults in the device at different times without the need of reprogramming the FPGA.

In the last part of the labs, the students face faulty behaviors and they learn how to develop a diagnosis strategy.

The training starts with an easy stuck-at fault case and goes crescendo. The students use the "pattern debugger" tool to visualize the failing vector cycles and failing output pins (fig. 6).Other investigation tools such as the "timing diagram" which provides the chronograms of the signals on all pins are also used. The type of fault may be assumed based on simple observations available in the pattern debugger… For instance, if only high states (H) or low states (L) fail, the failure is probably a stuck-at fault. If both high and low states fail, the failure may be a delay one. Next, we focus on identifying the failing pin. Here, we need to make assumptions and check if the combination of the defect and selected pin produced all the failures displayed in the test vector. The students are not used to this exercise but the outcome is an overall understanding of a product life cycle (design, manufacturing and test).

This exercise may be organized as a game: one student introduces a defect in the circuit from the FPGA board and the others have to apply the diagnosis procedure to identify the pin and the fault. If they are unsuccessful, the student may help them by providing some clues.

		Signal	CLK_IN	CLK_IO	_MR	CP	S0	S1	DS0	DS7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07	Q0	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	L	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	H	H	L	H	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

Figure 5. Example test vector failures

IV. CONCLUSION

This paper details an experience in the field of industrial testing education for undergraduate students. During 8 hours lab, the students acquire a global knowledge and know-how regarding the verification of integrated circuits and then better understand the interactions between design, manufacturing and test. An approach to insert faulty behavior in an FPGA-emulated device has been developed to support training on diagnosis strategies.

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