Teaching CMOS Circuit Design in Nanoscale Technologies Using Microwind

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Abstract—**This paper describes the experience in teaching integrated circuit design using an educational tool called Microwind through a Project-Based Learning approach. The evolution of the tool in the context of technology scale down is described, with focus on nanoscale technologies. An evaluation of the courses taught in two institutions (INSA France, and UniSA Australia) shows high levels of student satisfaction.**

Keywords- Integrated circuit design, VLSI Design, nanometer technology, project-based learning, lifelong learning.

I. INTRODUCTION

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nanoscale technologies for industrial production of high performance integrated circuits (IC). Table 1 gives an overview of the key parameters for technological nodes from 45 nm, introduced in 2007, down to 11 nm, which is supposed to be in production in the 2015-2018 timeframe (Fig. 1). Mass market manufacturing with the 32 nm technology is scheduled for 2011 [1] [2].

TABLE I. TECHNOLOGY ROADMAP DOWN TO 11-NM

Technology node	**45 nm**	**32 nm**	**22 nm**	**16 nm**	**11 nm**
First production	2007	2009	2011	2013	2015
Effective gate length	30 nm	25 nm	18 nm	12 nm	9 nm
Gate material	Metal	Metal	Metal	Dual?	Triple?
Gate dielectric	High K	High K	Very High K	Very High K	Very High K
Raw Mgates/mm^2	1.5	2.8	5.2	9.0	16.0
Memory point (μm^2)	0.3	0.17	0.10	0.06	0.03

Shifting to a new technology node impacts upon the design methodology, and requires improved technology models and tools to accurately predict the performances of the circuits. Engineering students need to be abreast themselves with the rapid changes in technology and design practices. Courses in IC Design [3] [4] must also aim to equip students with the skills of independent learning and lifelong learning. Due to time constraints in a semester long course it is often not feasible to introduce students to complex commercial design tools and at the same time expect them to develop practical circuit design skills and independent learning skills.

We present project-based approaches to teaching adopted in two institutions in Australia and France, both aimed at actively engaging students in stimulating learning experiences for the development professional design skills using the latest semiconductor technologies. We also illustrate the educational tool Microwind [5], developed to support the design of CMOS basic cells and well suited to project-based learning approach. In this paper, we focus on educational developments, teaching challenges, proposed design flow and associated tools in the light of these issues. We also present evaluation of the courses by UniSA and INSA students based on the same evaluation questionnaire.

II. DEVELOPMENTS IN CMOS TECHNOLOGY

A. General Trends

The introduction of every new technology node in the past years has represented massive improvement in MOS device performance. At the transistor level, the channel length of MOS devices is automatically scaled with a new technology node. Roughly speaking, the node corresponds to half of the gate layer pitch, although the definition differs depending on the application domain. Two approaches have been introduced recently to improve transistor current capabilities:

- Decreasing the oxide thickness t_{OX}. The oxide thickness has been reduced to 1.2 nm (5 atoms). Unfortunately, the gate oxide leakage is exponentially increased, which increases the standby power consumption. Starting with the 45 nm generation, so-called “metal gates” have been introduced, based on Nickel-Silicide (NiSi) or Titanium-Nitride (TiN), as illustrated in Fig. 2(a) and (b).

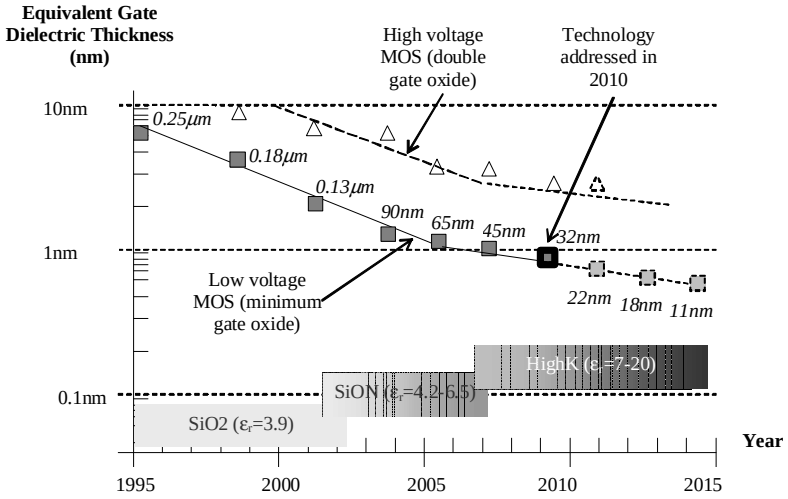


Fig. 1. Technology scale down and nodes, down to 11 nm.

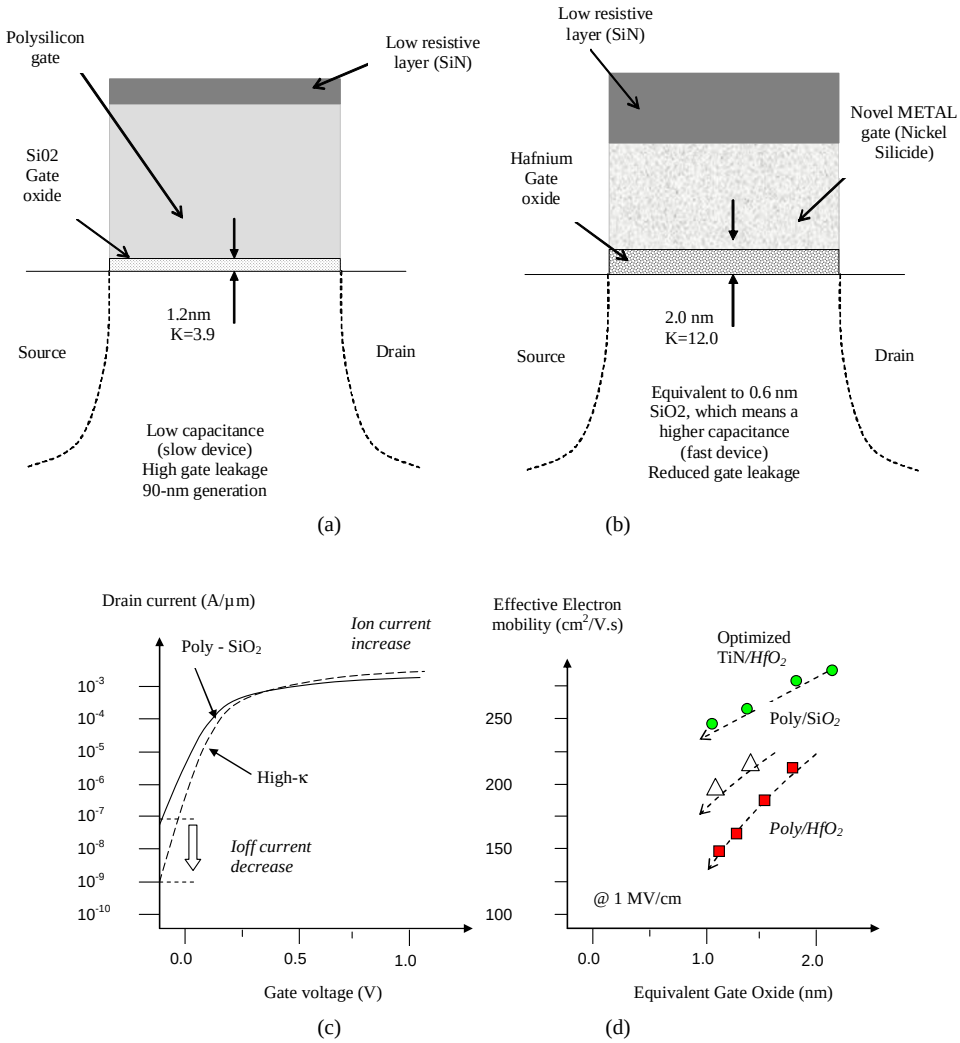


Fig. 2. Compared to poly/SiO2 gates (a), the metal gate combined with High-K oxide material (b) enhances the Ion current and drastically reduces the *Ioff* current (c). Electron mobility vs. Equivalent gate oxide thickness for various materials (d) from [4].

- Increasing the carrier mobility μ. Starting with the 90 nm generation the concept of strained silicon has been exploited to enhance the carrier mobility, which boosts both the n-channel and p-channel transistor performances. The 3rd generation of strain engineering used in the 32 nm technology massively boosts MOS performance [1] [2].

B. *Challenges*

It is acknowledged that the students need to develop as lifelong learners if they are to adapt to the rapid technological changes and the consequent changes in design concepts and methodologies. In addition, it is necessary for them to develop the important graduate qualities of problem solving and critical thinking in order to successfully operate in a continually changing and challenging field of VLSI Design. It is therefore important to consider the following issues:

- The commercial chip design tools available today are very powerful, and are capable of capturing the design and verification needs of modern ICs. However, these tools are highly complex and need long time to learn.
- It is very important for students to develop thorough understanding of the complex process technologies [3] [6] and their impacts on design alternatives using intuitive 2D/3D technology visualizations. Therefore it is necessary to use design tools that are not only less time consuming to learn but also provide intuitive design, simulation and visualization environments.
- Student diversity must be considered. From a pedagogical perspective, any gap in the background knowledge must be addressed first before effective learning of new concepts and skills can occur.

III. PROPOSED EDUCATIONAL SCENARIO

In order to address the design tool issue both UniSA and INSA courses use a set of user friendly design and simulation tools, namely Microwind and Dsch [5]. These tools and associated text books [7] [8] incorporate the most recent CMOS technologies and provide an interactive learning environment for the development of skills in design and analysis of integrated circuits.

A. *Educational Approach*

The design courses proposed to students for physical design of layout-level functional blocks include:

- An introduction to the technology scale down and its impacts on device integration, performance and design challenges.
- A tutorial on MOS devices, based on problem-based learning, introducing width/length effect, *Ion/Ioff* and *Vt* illustration, for both N and P devices (Fig. 3). To develop skills in modeling [3] and simulation the set of user-accessible SPICE model parameters is reduced to around 30 most important ones for BSIM4.
- The design of inverters, and a simple ring oscillator, and a small student contest to achieve the maximum oscillating frequency on a common technology node.
- The design of basic logic gates introducing interconnect design, compact design strategies, and impact on switching speed and power consumption.
- The design of analog blocs introducing amplification, voltage reference, addition of analog signals, and mixed-signal blocs [4].
- A capstone design project, e.g. microprocessor.

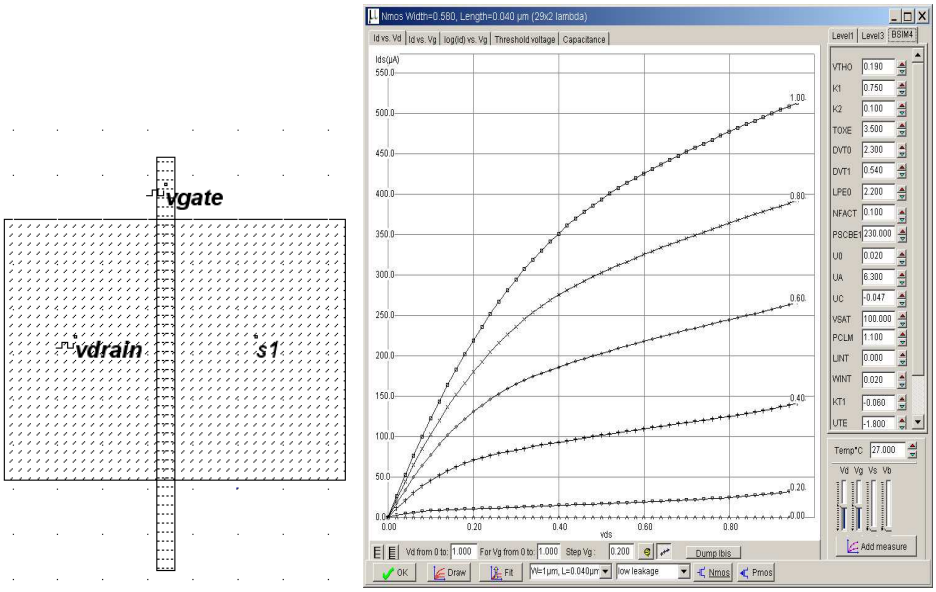


Fig. 3 : Student drawing of a MOS device with simulation properties (left), corresponding I/V curve using BSIM4 (right).

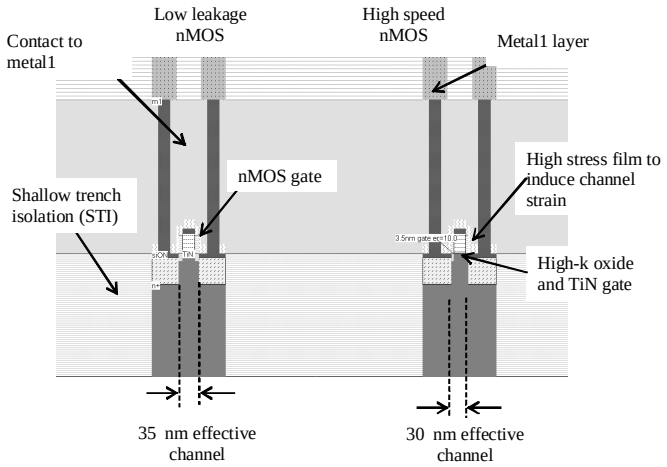


Fig. 4. 2D cross-section of Low-leakage/high speed MOS.

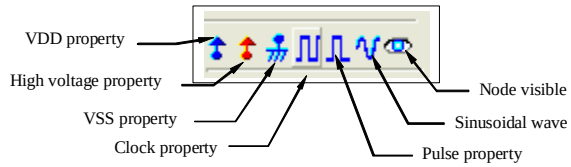
B. *Design Tool*

Microwind is a CMOS circuit editor and simulation tool, for logic and layout-level design, running on Microsoft Windows. It has been developed since 1998 through several versions, and is available as a freeware (lite version [5]) for educational purpose, and sold to universities through Ni2designs, India. Microwind allows students to draw the masks of the circuit layout (Fig. 4a), use a set of simulation properties (clocks, pulses, DC voltage sources, Fig. 5a) to build a test scenario, and validate the current/voltage relationships through built-in analog simulation (Fig. 5b). Our approach aims at giving students immediate confidence to design MOS devices. The approach consists of a step-by-step illustration of the most important relationships between the layout and its performance. We concentrate on 2D (Fig. 4), 3D views (Fig. 6), static and dynamic characteristics (Fig. 5), and the MOS model parameters that are considered most significant for educational purposes (Fig. 3-right).

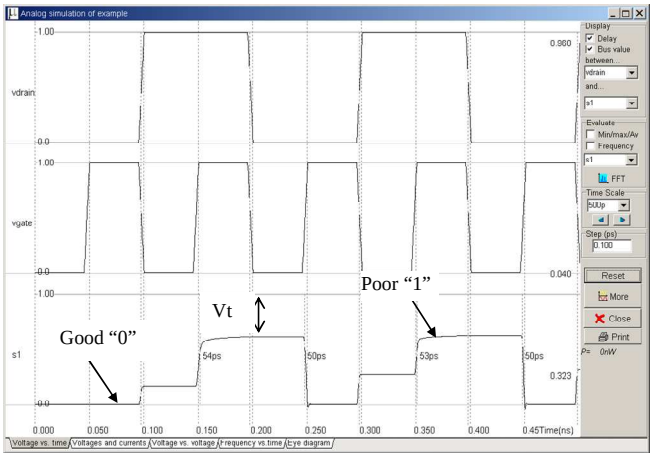
Through careful investigation of the simulations students are able to gather information about the key properties and drawbacks, for example junction capacitance effect that samples undesired intermediate voltage, threshold effect that jeopardizes the high voltage levels, and ultra-fast charge/discharge (in the picoseconds range). Microwind's layout library (MOS generators, and Cell compiler from Verilog-HDL description) is used progressively to ease the layout design phase.

C. *Project-Based Learning*

Project-based learning methods have been developed for the IC design courses at both UniSA and INSA. UniSA offers a course titled *VLSI Design*, which focuses on Digital CMOS IC design. It is offered in Masters by coursework programs and also as a final year course in undergraduate programs. Students are expected to have the necessary background knowledge and experience in digital logic design and electronics. The issue of student diversity is addressed by following a structured project-based approach. At INSA a similar approach is adopted for an introductory course titled *Physics and Modeling of Semiconductor Devices*, which is offered in the first year of a two-year *Masters* program *in Automatic Control and Electronics*. However a more open-ended approach is adopted in a second year course titled *Analog CMOS Circuit Design*.



(a)



(b)

Fig. 5. Properties added to the layout (a), and time-domain simulation of the MOS using BSIM4, showing analog memory effect due to junction capacitance and threshold voltage drift (b).

At both UniSA and INSA, the aim of the project-based learning (PBL) approach is to engage students in a stimulating learning experience for the development of professional design skills, and for the development of independent and lifelong learning abilities. The students do simple projects in the early stages using step-by-step *self learning guides*. Critical questions and increasingly complex tasks are gradually scaffolded within the projects.

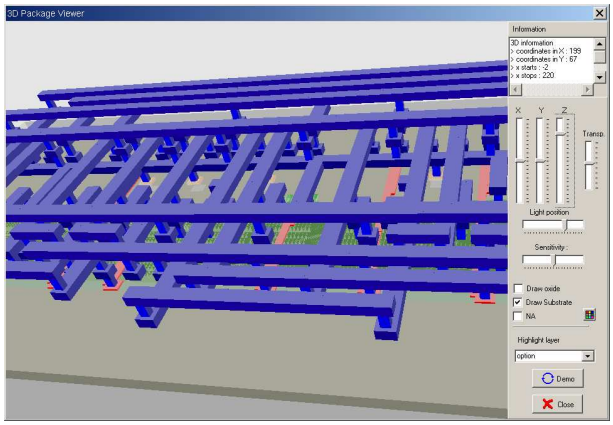


Fig. 6. 3D viewer showing the interconnect structure of a ring oscillator designed by students, with zooming and rotate functions.

These early projects, done mostly in a self learning manner, assist students in

- Reviewing/developing fundamental concepts
- learning how to use the design tools
- developing problem solving/critical thinking skills
- developing independent learning skills

On completion of each of the early projects the students get the satisfaction of designing a circuit that performs some useful function. This is helpful for confidence building and motivation, particularly for the students who are new to the idea of independent learning and whose previous educational experiences may have been quite different from the engaging PBL approach. The projects gradually increase in complexity requiring students to engage in deeper problem solving and critical thinking [9]. Finally there is a capstone project on designing a microprocessor which challenges students by putting the knowledge and skills they have developed to test.

Students develop design skills at layout level, are able to optimize the layout to increase speed, reduce the silicon area, and to check the layout for design rule violations (DRC). They gain valuable experience on the challenges involved in designing and simulating complex integrated circuits and are ready to explore professional tools available to industry.

IV. Evaluation By Students

The IC design courses at INSA and UniSA were evaluated anonymously by students using the same questionnaire. The courses at both the institutions consistently received high rankings in all the evaluation items. In the last five years, on average more than 90% of the respondents expressed satisfaction with the overall quality of the courses [9]. The project-based strategies were also evaluated using the specially developed questionnaire given in Table II. Fig. 7 presents the student responses to the questionnaire using a Likert scale of 1 to 5 (1–strongly disagree, 5–strongly agree). Clearly the students found the PBL strategies very useful for their learning.

TABLE II

Questionnaire for Evaluation of the PBL Approach

#	Question statement
1	I was able to work out how to use the CAD software by using the project handouts provided
2	I was able to learn circuit design techniques on my own by doing the projects using the project handouts
3	The handouts assisted in revisiting some of the background knowledge required for the course
4	The questions given in the project handouts helped me to think critically
5	The projects helped me put the theory of VLSI Design into practice
6	The final capstone project challenged me to test my learning in the course
7	I feel confident about completing similar capstone projects independently
8	The skills I learn in VLSI project work are useful to me
9	Overall I am satisfied with the project-based learning approach used in the VLSI Design course

V. Conclusions

The use of the educational tool Microwind that enable students to develop circuit design skills using modern deep submicron technology has been one of the underlying factors for the successful delivery of the digital and analog integrated circuit design courses in two institutions in Australia and France. Engaging students in design work involving a range of latest technologies has enabled them to understand the impacts of technology scale down on factors such as speed, power and noise. Using project-based learning methodologies suited to the teaching context, digital and analog IC design courses have been delivered with high levels of student satisfaction. Collaboration among faculty members at the two institutions has led to the production of a range of learning resources to support students through project-based learning and to assist them in developing independent and lifelong learning skills. These resources are available at www.microwind.org and http://tiny.cc/UniSAVLSI.

Acknowledgment

The authors would like to thank Bhupesh Purohit and Vinay Sharma of ni2designs, India for their support and inspiration, as well as numerous academics and students worldwide who used our design tools and course resources, and sent valuable feedback.

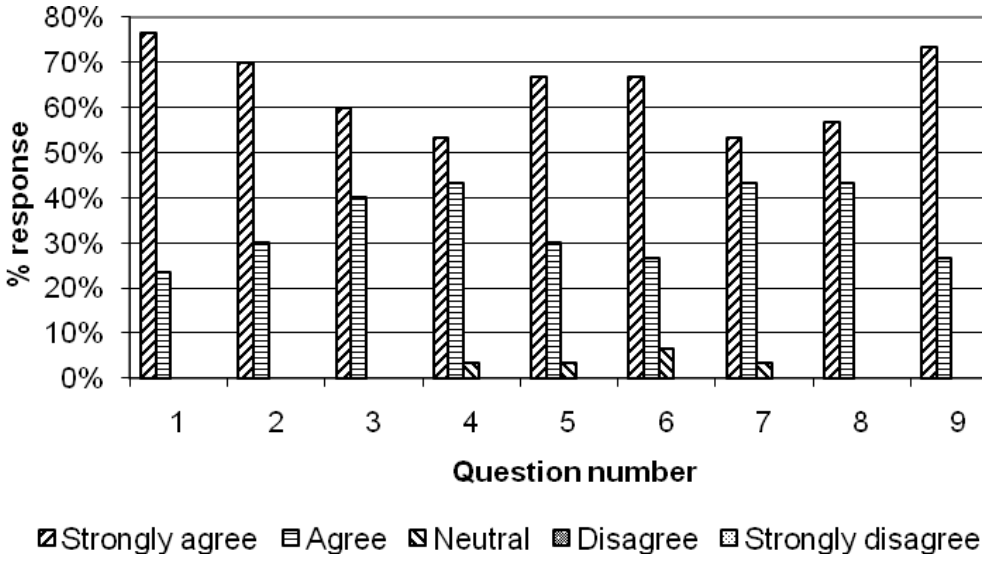


Fig. 7. Student responses to evaluation of the PBL approach, from [9].

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