



An FPGA Design And Implementation Framework Combined With Commercial VLSI CADs



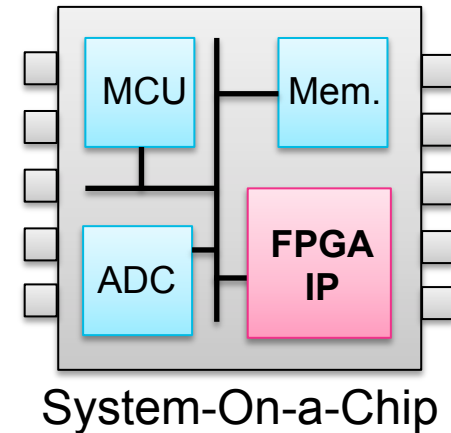
ReCoSoC 2013

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- FPGA IP core development
 - Make SoC programmable
 - Requirements:
 - Synthesizable
 - Architecture exploration
 - Scalability
 - Other features (3D, dependability, etc)



Traditional
academic flows
are not applicable

- **FPGA IP design framework is required**
 - Efficiently evaluate & implement various arch.
 - Connect to commercial VLSI design flow

Goal of this research

- Goal: *Develop an FPGA IP design framework*
- Method: *Develop novel routing tool **EasyRouter***
- New features:
 - Implement new architectures easily
 - C#(Mono) Platform (Linux/Windows)
 - C# script based Arch. definition
 - Arch. Exploration -> HDL & Bitstream generation
 - Same arch. exploration functions as traditional tools
 - Generate HDL & BitStream with simple templates
 - Performance analysis with commercial VLSI flow

Compare with VPR

- VPR is the main academic placement & routing tool

VPR6.0 (current version)

- **Not for synthesizable FPGA**
 - Delay model is not suitable for standard cells based design

- **Only support Island style FPGA**
 - Arch. is defined with XML&C
 - Hard to implement new architectures

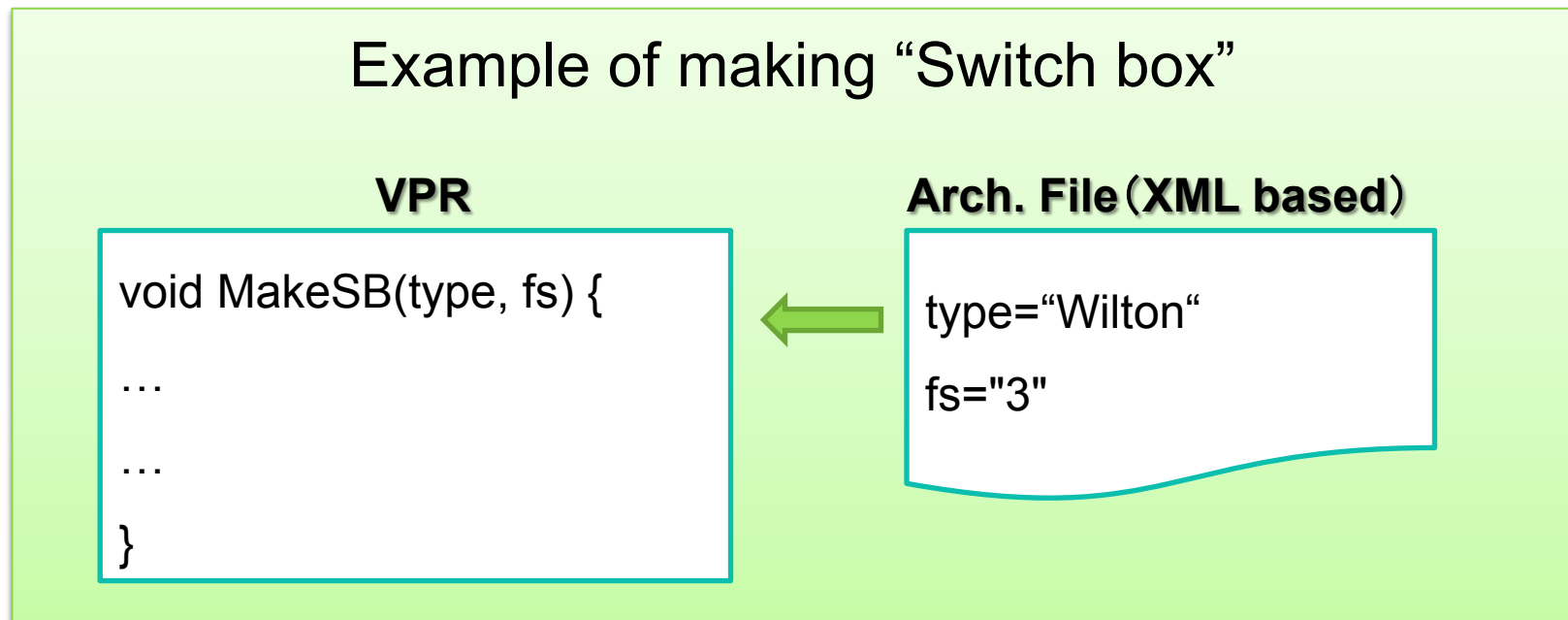
Novel EasyRouter

- HDL & Bitstream generation
- High accuracy analysis with VLSI CADs

- C# language
- Script based arch. definition

VPR: XML based Arch. definition

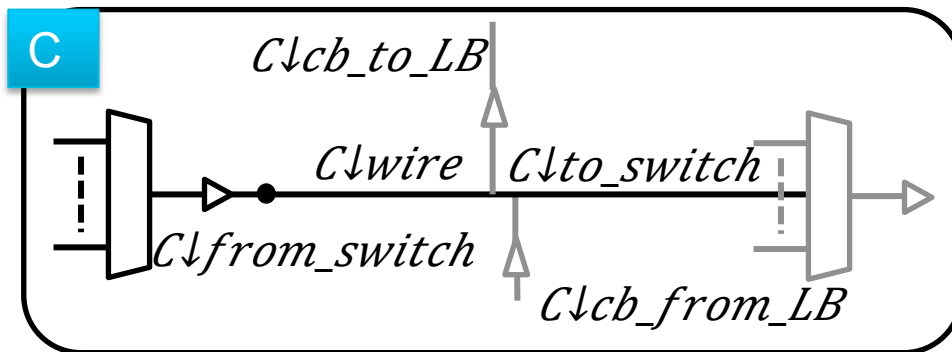
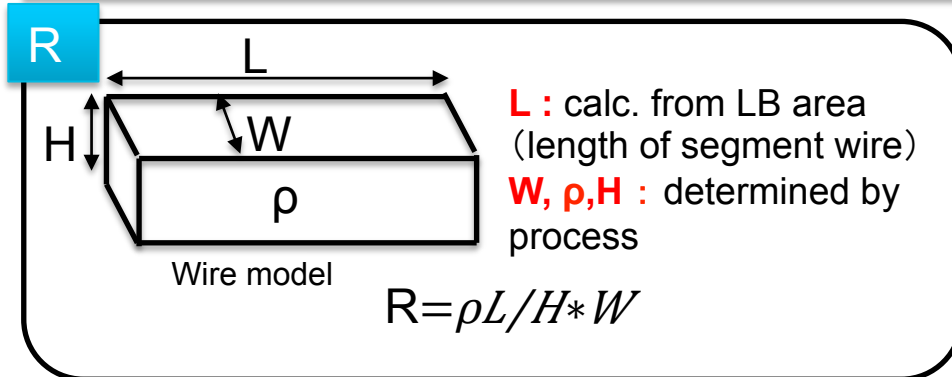
- Only support “Island Style” FPGA
- Parameters can be changed in XML based Arch. File



- Only **small changes** can be made for the supposed Arch.
- For unsupported Arch., need to **modify the source code**

VPR: Delay model

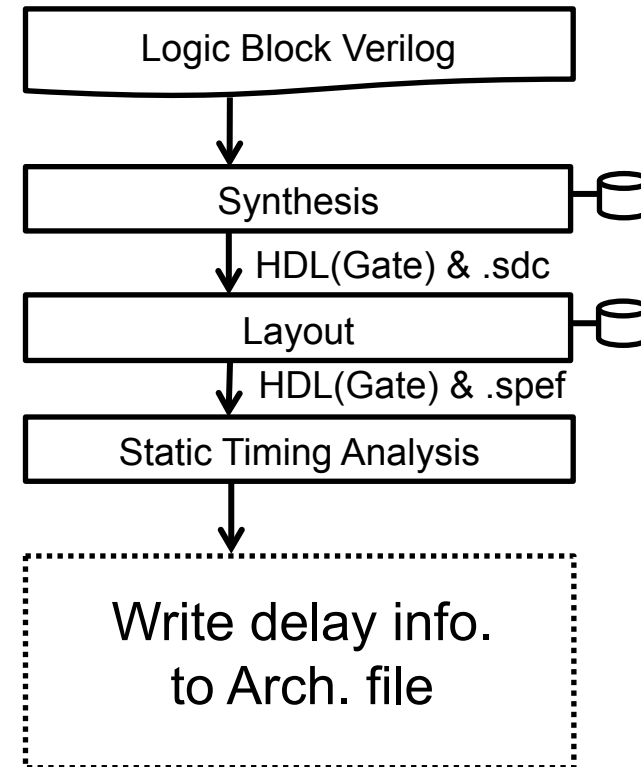
Routing delay



Elmore delay model

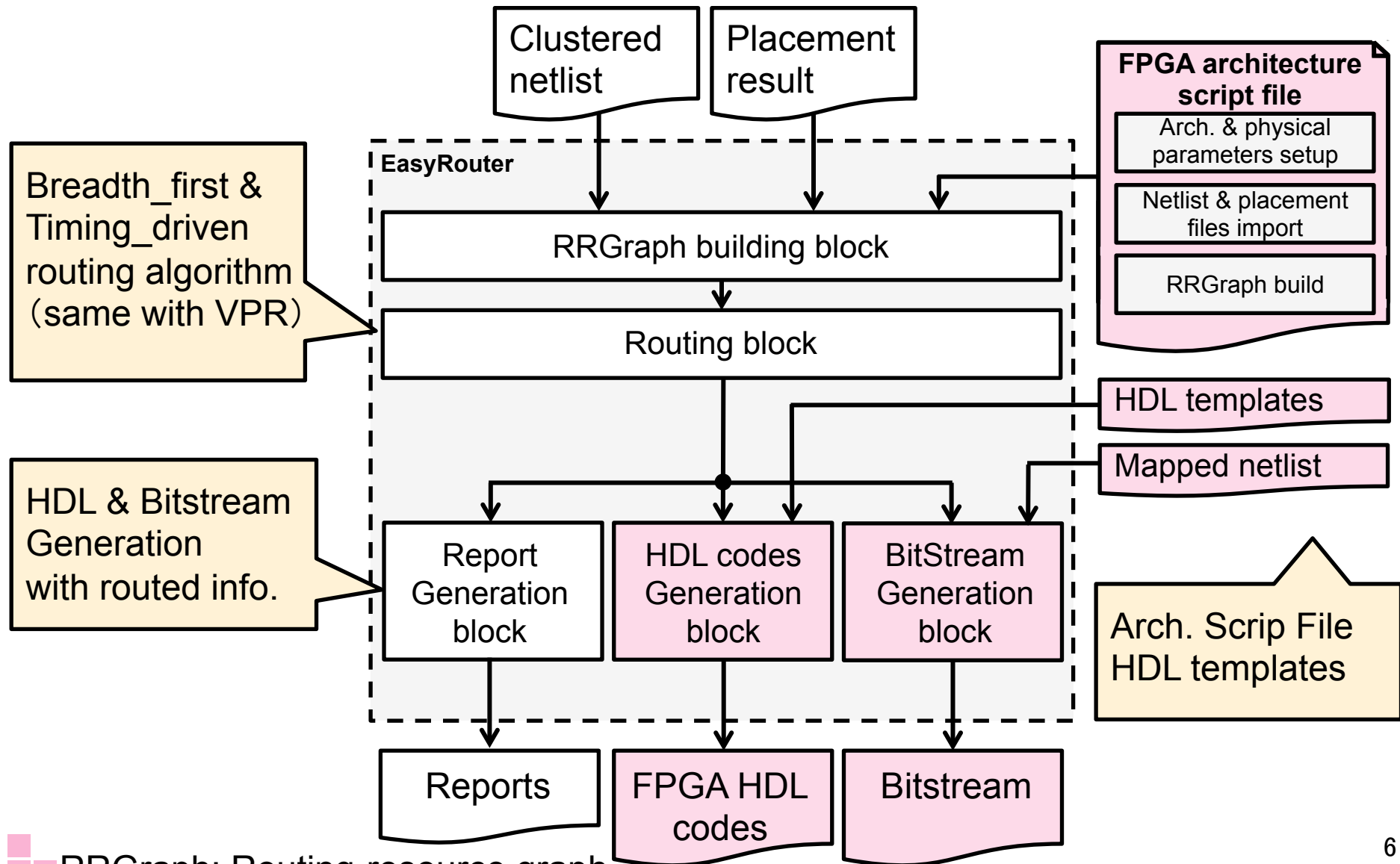
$$\sum_{i \in source\ sink\ path} R_i \cdot C(subtree_i) + T_{d,i}$$

Logic delay

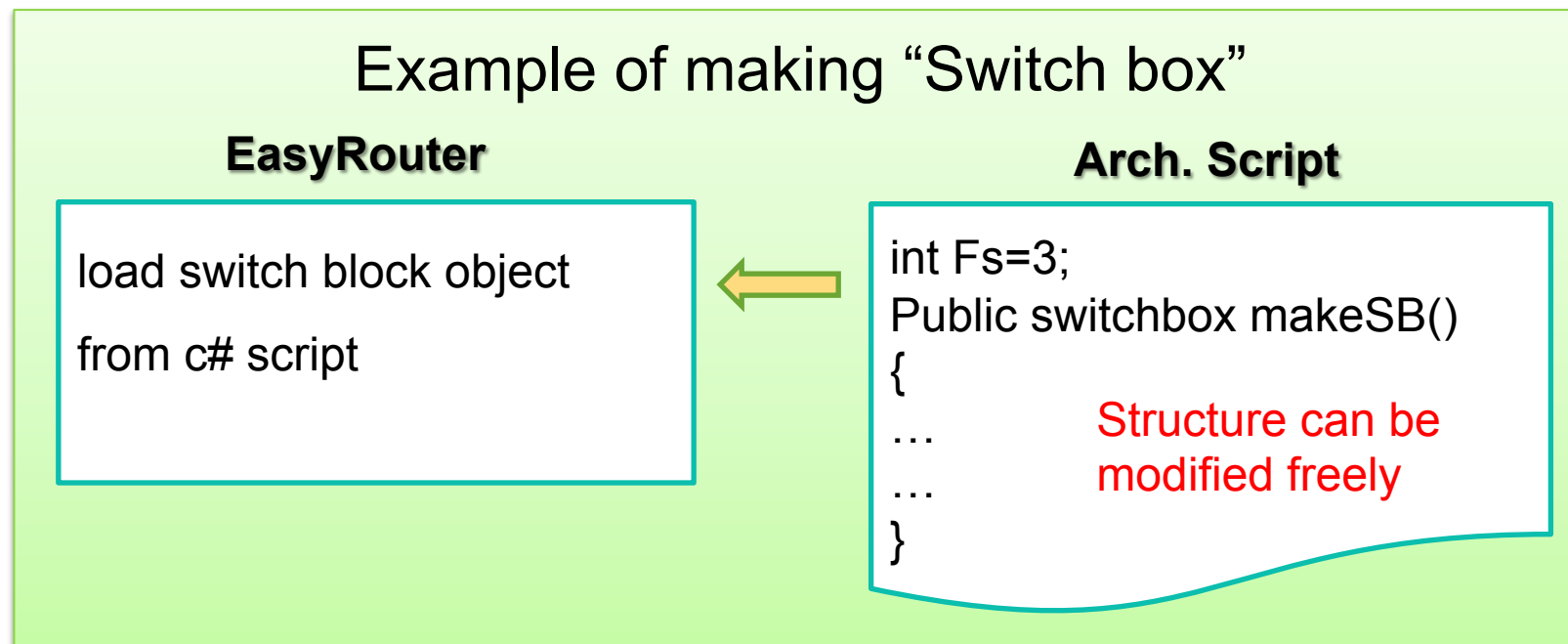


Critical path delay
 (Composed with different delay model)

EasyRouter blocks



- Implement FPGA Arch. in a script file
 - Dynamic compiled during execution
 - Contains both Arch. Implement codes and parameters
 - Any architecture can be implemented in low cost



VerilogHDL

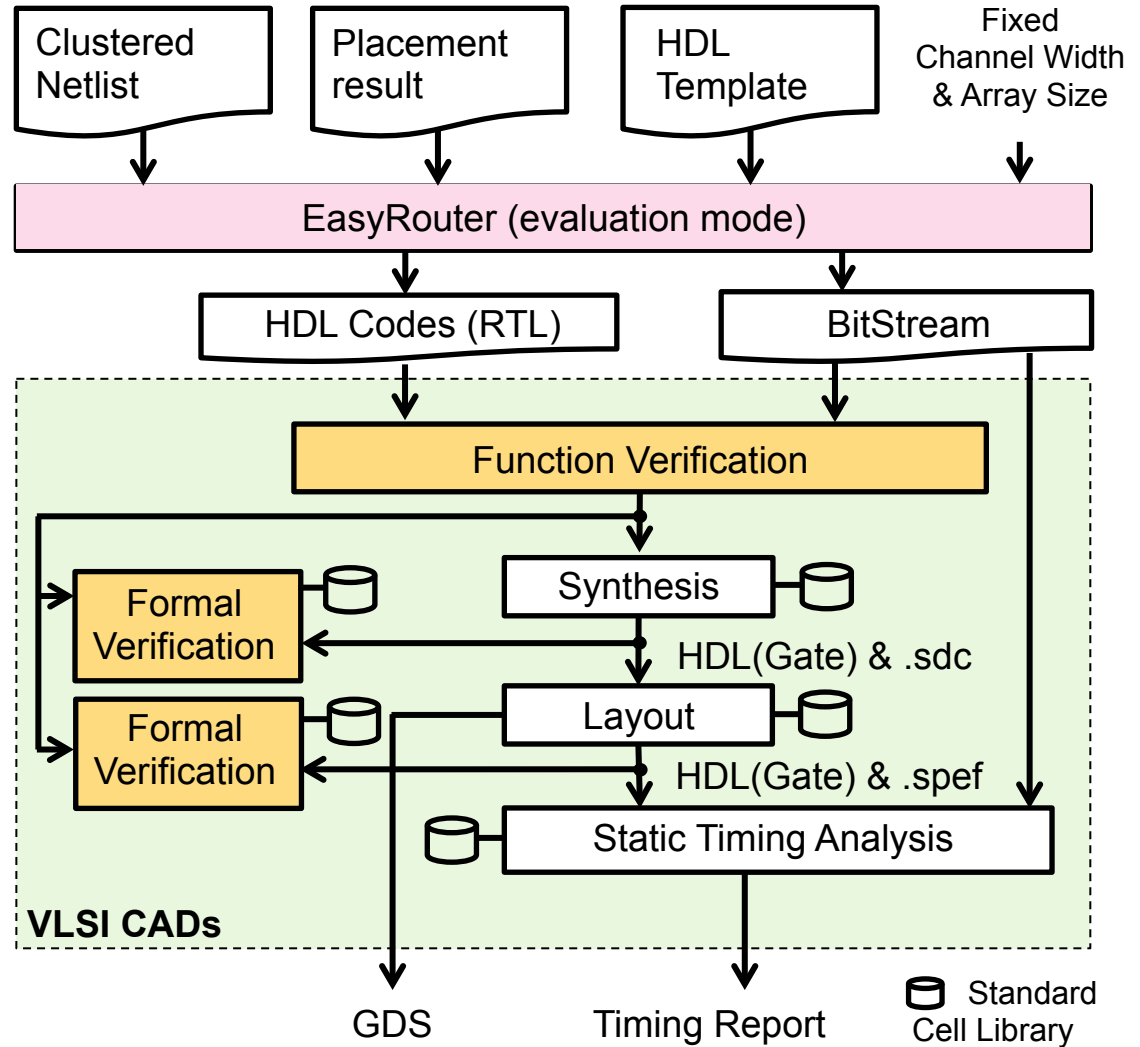
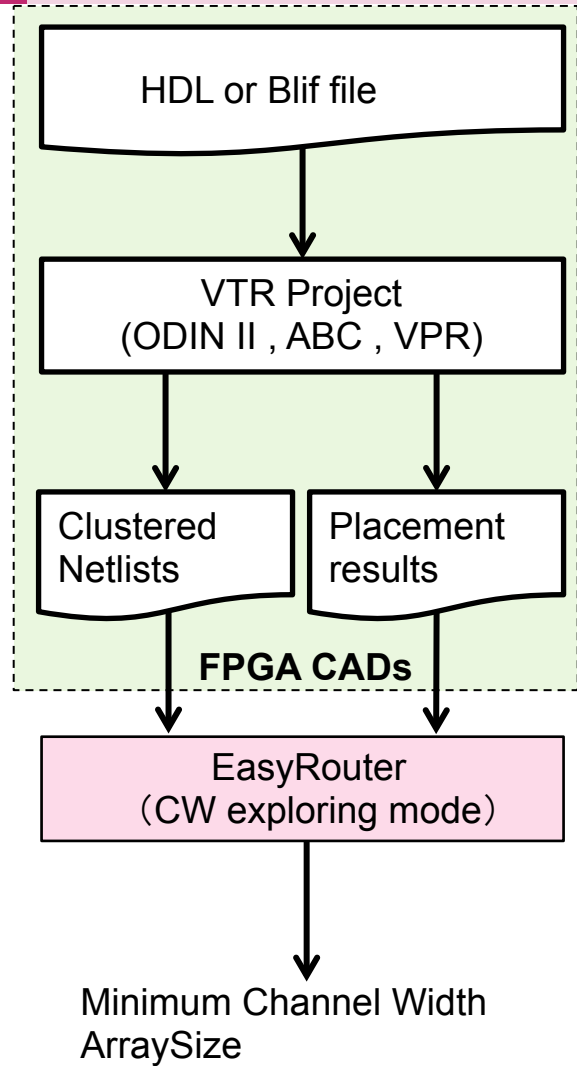
- **Logic block**
 - Prepared in template
- **Routing**
 - Generated according to Channel width / CB,SB topology
- **Chip** :Top level module according to array size

BitStream

- **Routing & Local connection block**
 - Generated according to routed info.
- **Logic block**
 - Technology mapping results



FPGA design flow based on EasyRouter

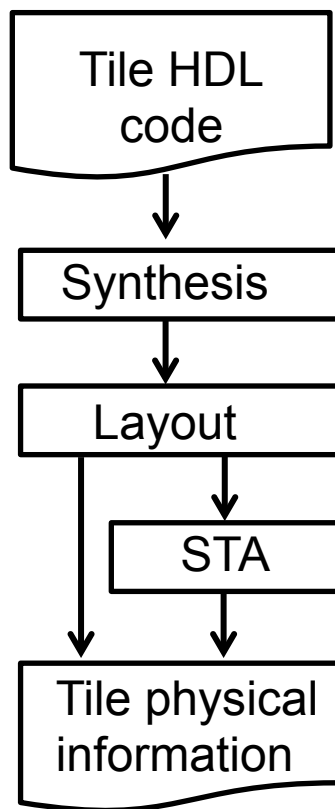


Device scale exploration

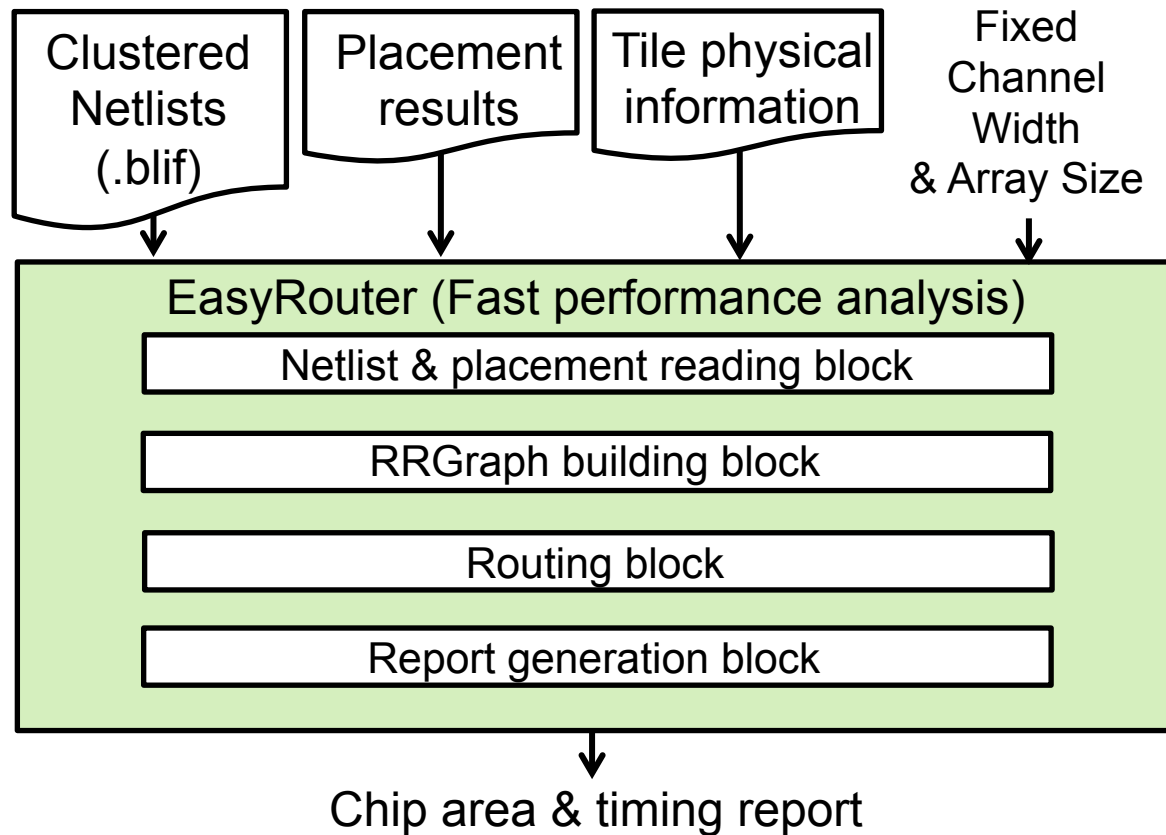
Device implementation

Fast evaluation with EasyRouter

- The fast evaluation with EasyRouter can be used when
 - VLSI analysis is too slow (big chip)
 - No available VLSI flow(3D-FPGA)



(a) Tile info.



(b) Fast evaluation with EasyRouter

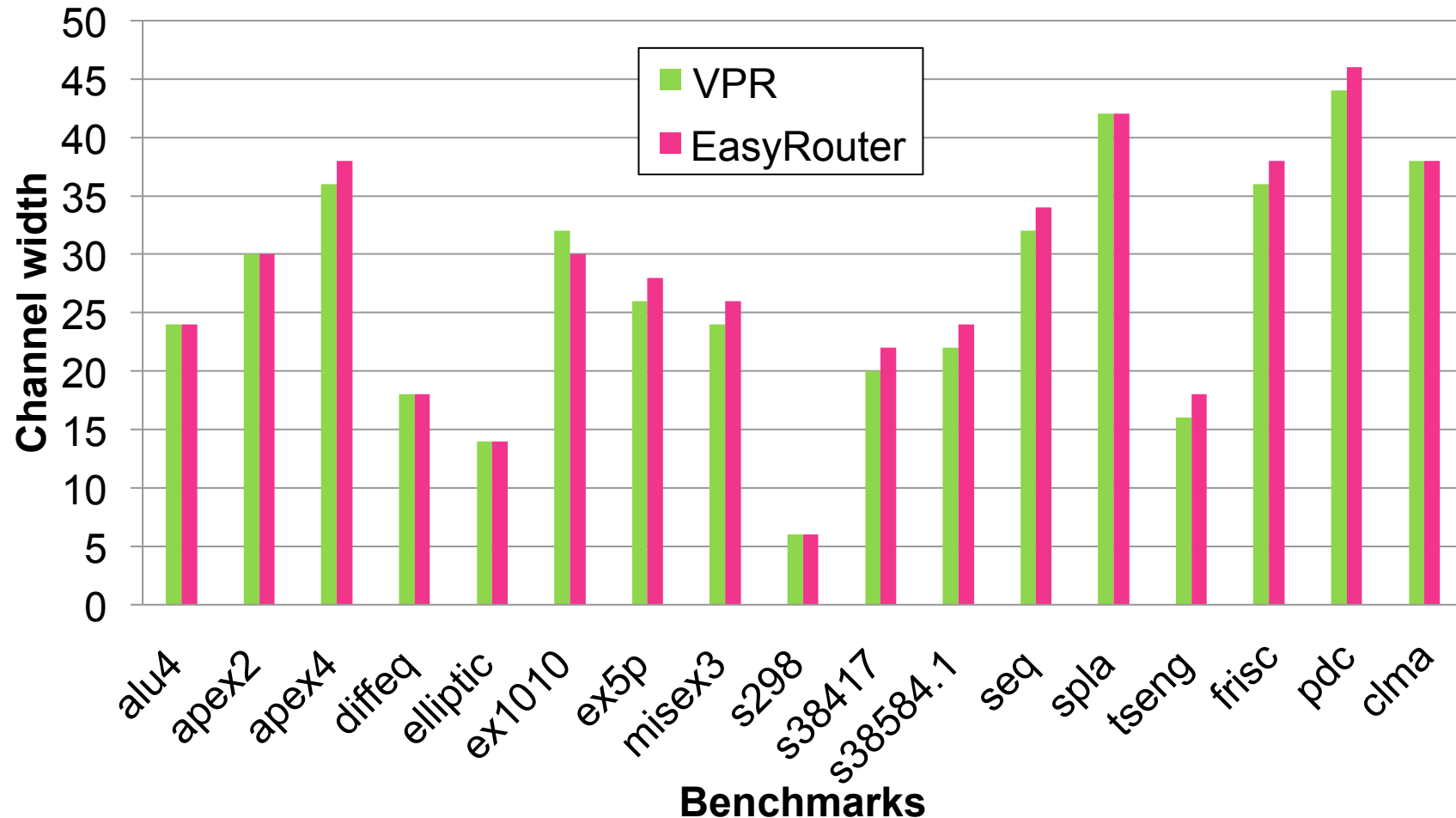
Evaluation : EasyRouter

- Device structure
 - Island style FPGA

Item	value
Logic cluster	4-LUT×4
# of LB inputs	10
SB	Wilton(Fs=3)
CB	Fc_in=0.5, Fc_out=1.0
Channel	Single lines

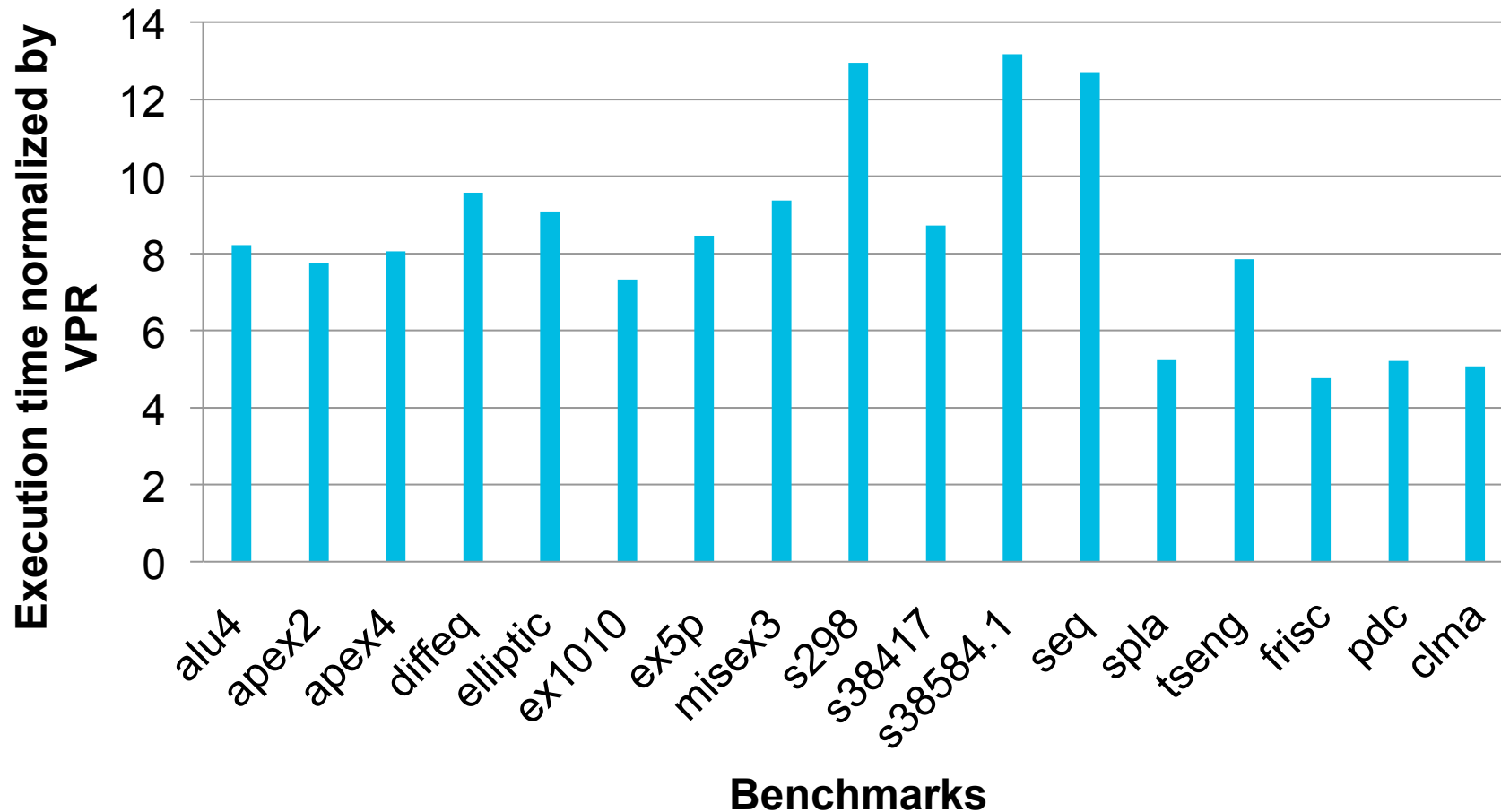
- MCNC Benchmarks
- Evaluation items
 - Minimum channel width for routability evaluation
 - Execution time for tool efficiency evaluation

Minimum channel width (Routability)



- EasyRouter has almost the same routability with VPR
- Minor differences are from different routing orders

Execution time (CPU time)



- EasyRouter is 8 times slower than VPR on average
- Big circuits are about 5 times slower

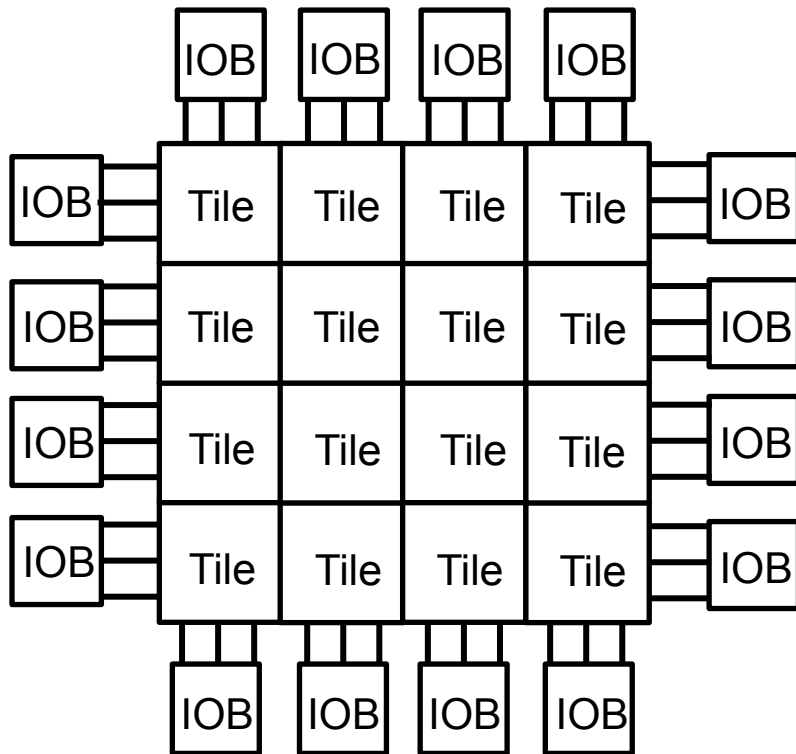
Evaluation for proposed design flow

- Process : e-Shuttle 65nm
- Device parameters

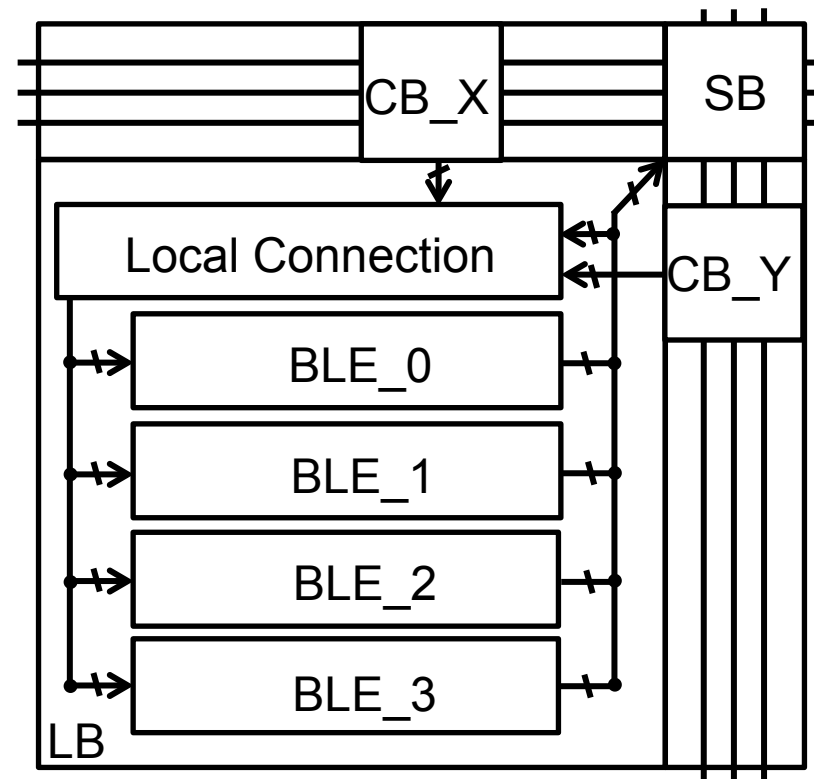
Item	value
Array size	15×15
Logic cluster	4-LUT×4
# of LB inputs	10
SB	Wilton(Fs=3)
CB	Fc_in=0.5, Fc_out=1.0
IOB	Fc=1.0
# of routing tracks(single line)	50/channel

- MCNC Benchmarks
- Evaluation items
 - Critical path delay on average (10 placement seeds)

Device architecture for evaluation



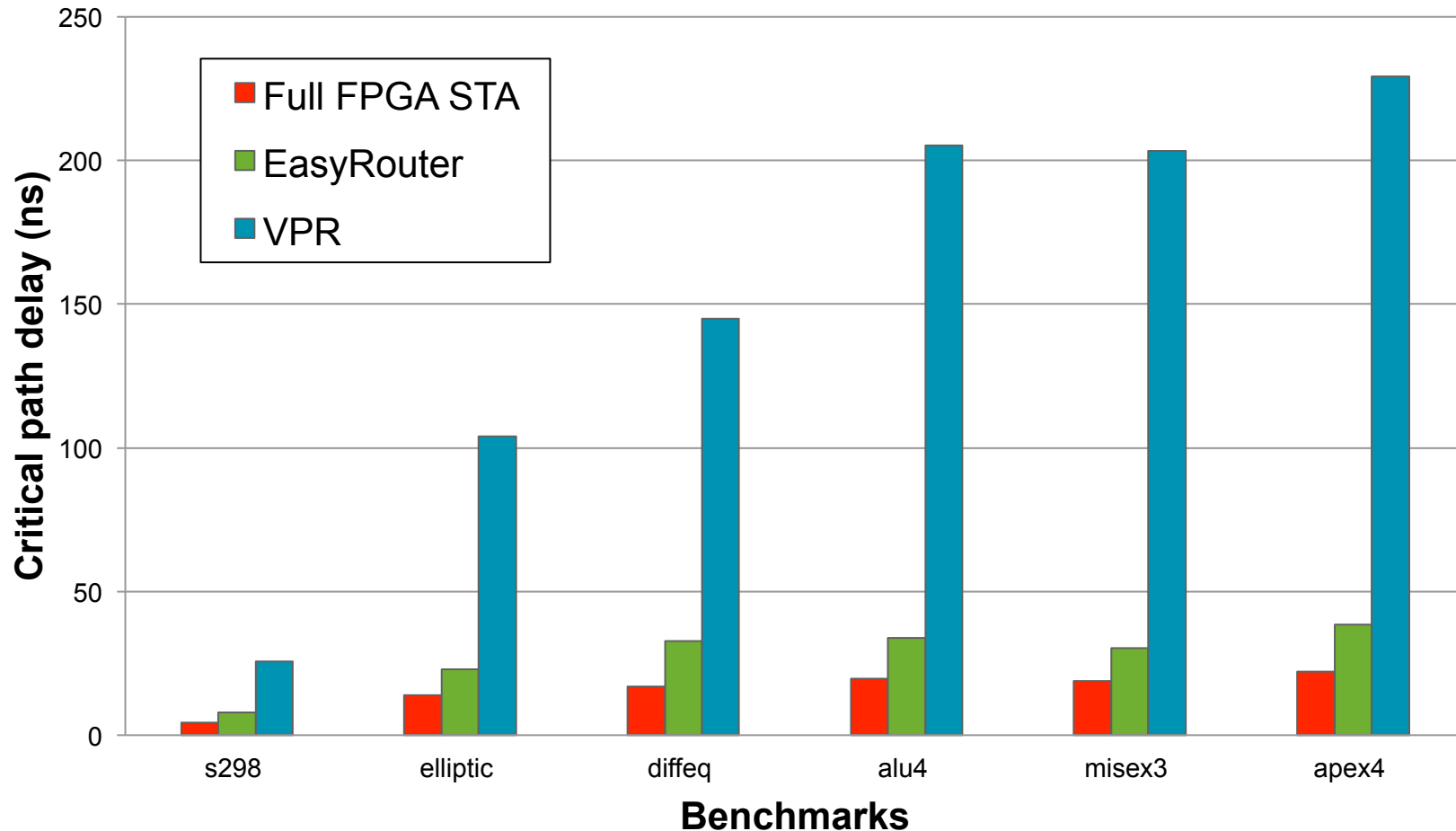
Homogeneous FPGA



Tile structure



Critical path delay results



- Delay from VPR is about 10x worse than STA results
- Delay from EasyRouter is about 1.5x worse than STA results

EasyRouter

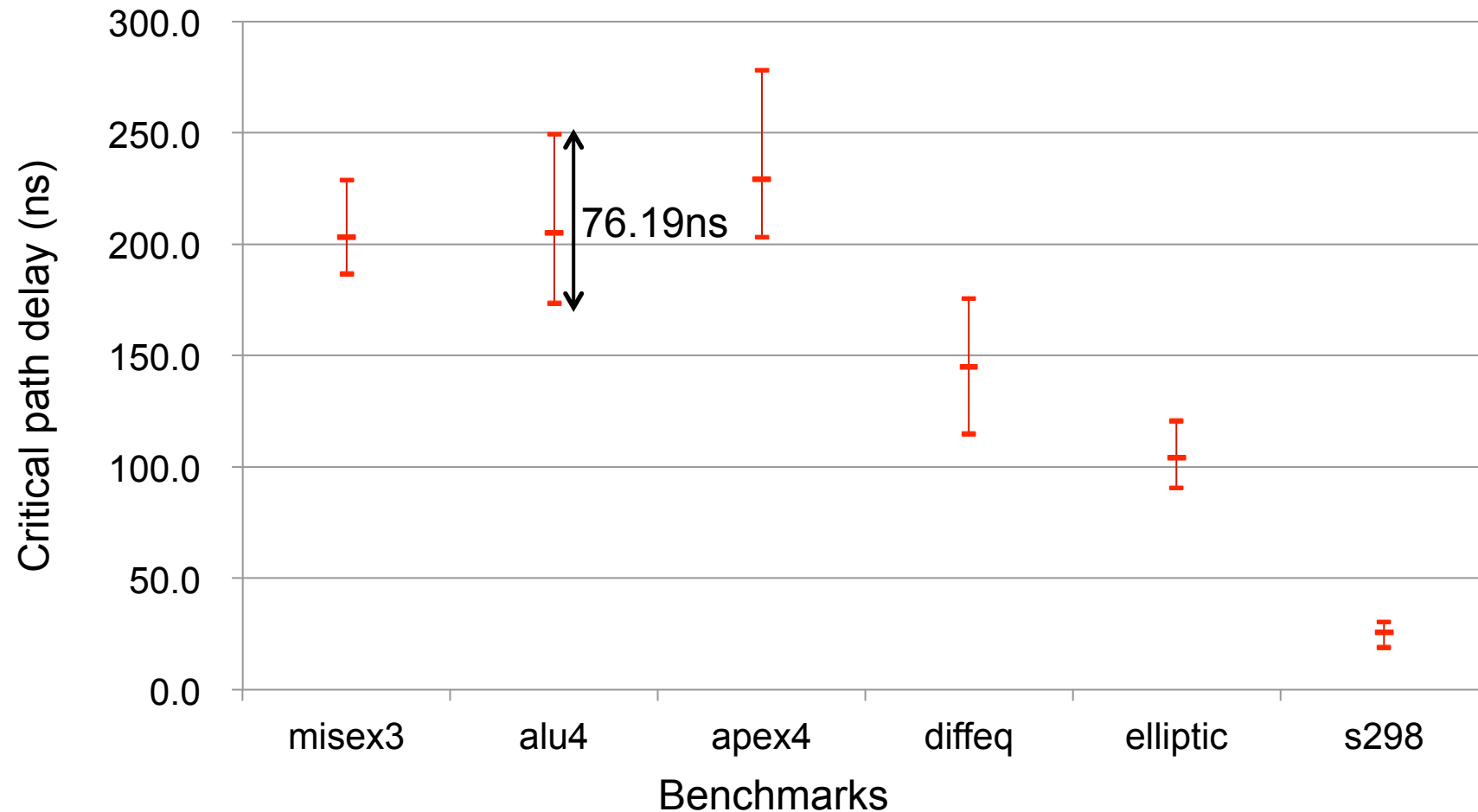
- **Simple**: New arch. can be implemented in low cost
- **High accuracy**: Link academic FPGA tools with commercial VLSI CADs

Other works with the proposed flow

- 3D-FPGA(VLSI-SoC2013)
 - “Three-Dimensional Stacking FPGA Architecture Using Face-to-Face Integration”
- Hierarchy routing FPGA(FPL2013)
 - “Defect-Robust FPGA Architectures For Intellectual Property Cores In System LSI”

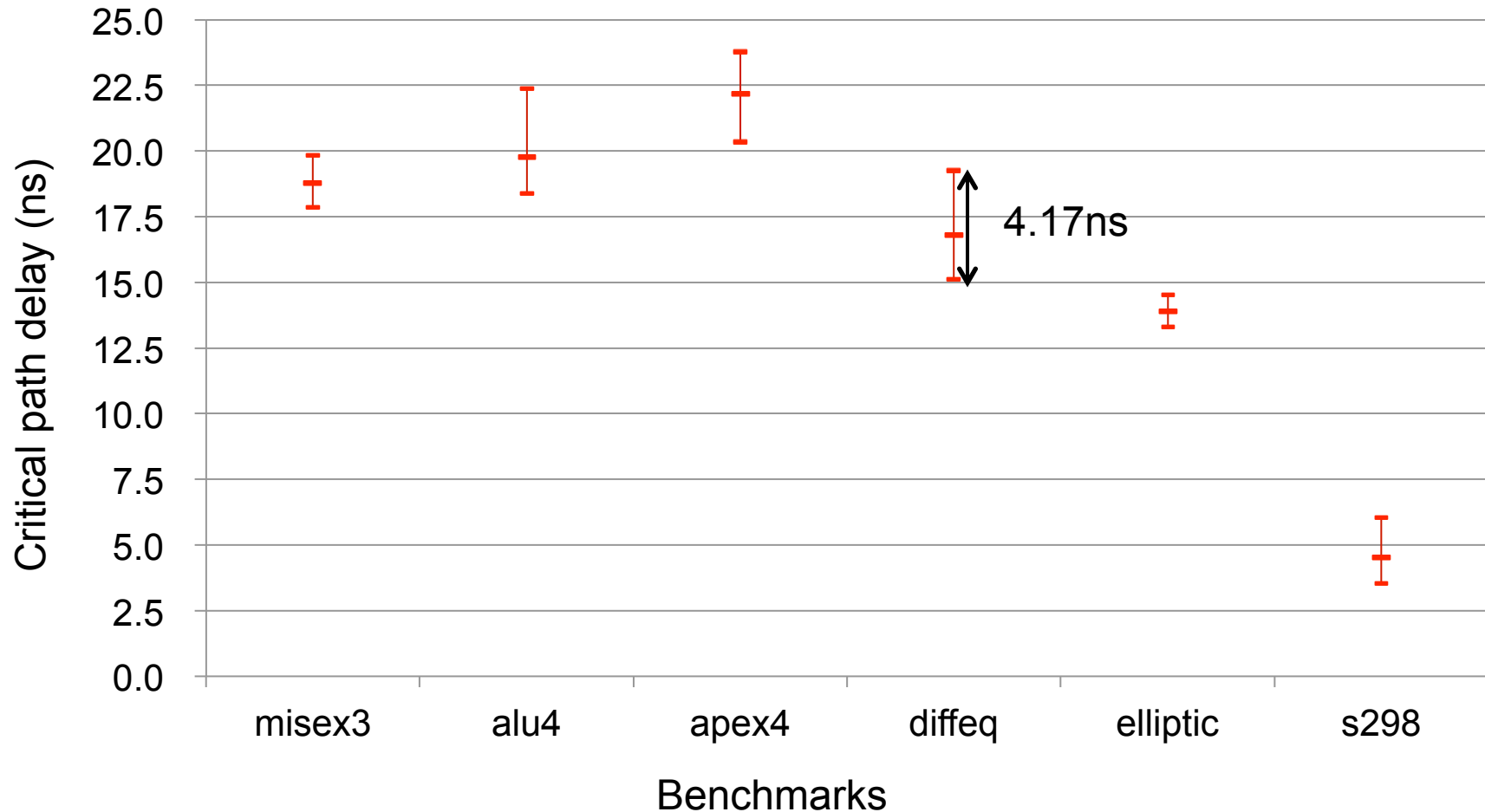
Thank you for your attention.





- **Change range of delay results of VPR is large when placement seed value changes**

EasyRouter (MIN-MAX-AVG. value from 10 seeds results)



- **Change range of delay results of STA results are smaller than VPR when placement seed changes**