And now, where do we go?

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http://cmp.imag.fr

EWME, Darmstadt, 10 May 2010

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Agenda

- Quick look back to the past
- How to cope with the demand for ever more complex systems?
- Cooperate with other Communities: e.g. BioMed
- Address important application areas: e.g. energy management
- Conclusions

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Quick look back to the past:

Infrastructure Services in the world

- Pioneering efforts
- First cooperative initiatives
- National Services in the world

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Pioneering efforts: 70s – 80s

Australia

1982

1982-1984 : 2 services
* CSIRO
* JMRC
NMOS
CMOS (1985)
AUSTEK
no central organisation
ES2, ORBIT, AWA, CMP

Belgium

1986

ARAMIS
UCL
CMOS 3µ
S01 CMOS 3µ

IMEC process stopped in 1991
MIETEC 2µ CMOS
in 1989: 1.5µ 2P 2M
3µ SDBiCMOS
stopped its own operations in 1992
until 1992: 61 runs, 620 designs

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Brazil

1986 VTI

1988 : linear bipolar
Sid-Microelectronics

ES2

Canada

1984 CMC

Northern Telecom:
CMOS 1.2µ, BiCMOS .8µ
20 GHz GaAs

GENNUM CORP. : bipolar linear array

300 designs/year, 15 runs/year

France

1981 CMP

CMOS from ES2, AMS
BiCMOS from AMS
Bipolar from TCS
GaAs from VSC, PML
.5µ CMOS from STM (JESSI)
prototype / small volume

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Germany

1984	EIS SIEMENS
	AEG
	FhG
	ended 1987
	Darmstadt
	ITT-Intermetall
	1.2µ

India

Plans	DoE
	3 levels
	level I : central at DoE New-Delhi
	level II : Academic Institutions,
	R/D labs
	UNDP

Ireland

1984	NMRC
	CMOS .5µ 15V

Italy

1988	SGS
	EC Special Action for SMEs
	ES2, AMS

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Japan

Local agreements
ASTEM (ES2)
plans

Korea

1990 **Seoul National University**
1.5µ CMOS
3-4 runs/year
Seodu Logic: ORBIT

Malaysia

1985 MIMOS
Norchip, Australia
plans

Portugal

INESC, 1982
FUNDETEC, 1989

Scandinavia

1981 NORCHIP
VTI, ES2
until 1993: 99 runs, 1670 designs
Now: Nordic VLSI (CHIPSHOP)
CMOS from AMS

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Spain

1986 CNM
UCL CMP
CMOS from ES2

Switzerland

MICROSWISS, EPFL/LEG
SMEs
CHIPSHOP + CSEM – Faselec (CMOS LP) + EM (CMOS)
HMT to STM
ASCOM in Bipolar

Republic of China

1984 1991: 2 runs CMOS 1.2 µ
1992: CMOS, BiCMOS
CIC (NSC)
advanced processes: industry and academics, CMOS .8µ DP/DL and SP/DL, .8µ BiCMOS
educational processes: CMOS .8µ SP/DM and 3µ DP/SM
plans for n.6µ GaAs
about 200 designs so far

The Netherlands

ES2
DIMES metallizes analog bipolar
CMOS gate array, CMOS sea of gates

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United Kingdom

1978 Central Fabrication Facilities
Universities of Southampton, Edinburgh, Sheffield for process, lithography at RAL
Design and Test Centers, 1984
→ commercial foundries: Plessey, Ferranti, GEC

ULVC, 1986
University of London
ES2, CMP
ECAD, 1986
CAD

Microelectronics in Business, 1993
SMEs

USA

1972 CALTECH: shared wafers
MEAD/CONWAY, 1978: 9 Universities
US Universities in 1979
MOSIS, 1983
CMOS from ORBIT, HP, GaAs from VSVC

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First cooperative initiatives

EUROMOS

CMP, Darmstadt, Norchip, NIHE

1985

Protocol of Grenoble:

CMP, EIS, NORCHIP, IMEC, NELSIS, ARAMIS, PE-Micro

1987

EUROCHIP & CHIPSHOP (EUROPRACTICE)

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National Services in the world, besides EP

CIC : Taïwan
CMC : Canada
CMP : France
ICC : China
IDEC : Korea
MOSIS : USA
VDEC : Japan

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CIC – Taiwan
1992
E, R, I

90nm MS CMOS	UMC
0.13µm MS/RF CMOS	TSMC
0.13µm Logic/MS CMOS	TSMC
0.18µm 1P6M CMOS	TSMC
0.35µm 2P4M CMOS	TSMC
0.35µm SiGe BiCMOS	TSMC
0.15µm PHEMT GaAs	WIN
0.35µm CMOS MEMS Post Process	TSMC
0.18µm CMOS MEMS Post Process	TSMC

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CMC - Canada
1984
5 year contracts from NSERC
E, R

45nm, 65nm and 90nm CMOS	STMicroelectronics through CMP
0.13 µ CMOS	IBM through MOSIS
0.18 µ CMOS	TSMC through MOSIS
0.35 µ CMOS	TSMC through MOSIS
0.5 µ SiGe BiCMOS, 5AM & 5HP	TSMC through MOSIS
0.8 µ CMOS in three process flavors: high-voltage--up to 300V, mid-voltage range--+/-20V, and standard-voltage--2.7V to 5.5V	DALSA Semiconductor
2.5 GHz Bipolar linear array	Sound Design Technologies
PolyMUMPs surface micromachining process	MEMSCAP through CMP
MetalMUMPs	MEMSCAP through CMP

Microfluidics: Sensonit glass-based microfluidic process with metallization (through Micronit); Protolyne glass-based process (CMC through partnerships with Micralyne and Canadian university laboratories)

Photonics/optoelectronics: InP, GaAs, EPI-only InP/GaAs, Silica/Si and Silicon-on-Insulator based technologies (through Canadian Photonics Fabrication Centre): SOI (EpixFab through IMEC)

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ICC – China
2000
1996 – 2000: Fudan University
E, R, I

0.35µm CMOS	Chartered
0.25µm CMOS	Chartered
0.18µm CMOS	Chartered
0.13µm CMOS	TSMC
0.18µm CMOS	TSMC
0.25µm CMOS	TSMC
0.35µm CMOS	TSMC
0.09µm CMOS	SMIC
0.13µm CMOS	SMIC
0.18µm CMOS	SMIC
0.35µm EEPROM	SMIC
0.18µm CMOS	HJTC
0.25µm CMOS	HJTC
0.25µm EEPROM	HJTC

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IDEC - Korea
1995
IDEC Chip Design Contest
E, R

CMOS 0.18 µ, 1-poly 5-metal	Samsung Electronics
CMOS 0.13 µ, 1-poly 6-metal	Samsung Electronics
CMOS 0.35 µ, 2-poly 4-metal	Magnachip/Hynix
CMOS 0.18 µ, 1-poly 6-metal	Magnachip/Hynix
CMOS 0.18 µ, 1-poly 6-metal	Dongbu HiTek
CMOS 0.13 µ, 1-poly 6-metal	Dongbu HiTek
HVCMOS 0.5 µ, 1-poly 2-metal	KEC
BJT 4 µ, 1-poly 2-metal	KEC

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MOSIS - USA
1981
1995 E, R, +I

Agilent/HP (Avago)	**0.5µ CMOS**
AMI Semiconductor	**0.35µ, 0.5µ, 0.7µ, 1.5µ CMOS**
IBM	**45nm, 65nm, 90nm, 0.13µ, 0.18µ and 0.25µ CMOS**
	0.13µ, 0.18µ, 0.25µ, 0.35µ and 0.5µ SiGe BiCMOS
TSMC	**65nm, 90nm, 0.13µ, 0.18µ, 0.25µ, 0.35µ CMOS**
Austriamicrosystems through CMP	**0.35µ CMOS; 0.35µ HV CMOS**
	0.35µ SiGe BiCMOS

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VDEC - Japan
1996
E, R + I (STARC)

1-poly 12-metal CMOS 65nm	e-Shuttle, Inc.
2-poly 2-metal CMOS 1.2µm	SCG Japan Ltd. (OnSemiconductor Ltd.)
1-poly 5-metal CMOS 0.18µm	Rohm Co. Ltd.
2-metal 0.8µm bipolar	NEC Compound Semiconductor Devices Ltd.
1-poly 6-metal CMOS 90nm	NEC Electronics Corporation
1-poly 4-metal SiGe SOI BiCMOS 0.25µm	Hitachi Ltd.
VDEC-MOSIS CMOS 0.25µm / 0.18µm	TSMC
VDEC-MOSIS Si-Ge BiCMOS 0.5µm	IBM

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All of them: same legal status

- **non profit**
- **hosted at Universities**

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Where should Service Organizations go?

- **Today: cooperation, in action**
- **Tomorrow:**
  - **+ nanoelectronics: complexity**
  - **+ cooperate with other Communities**
  - **+ address important application areas**

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Nanoelectronics

- complexity: 3D
- ultra low power: Magnetic Logic Circuits

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Complexity

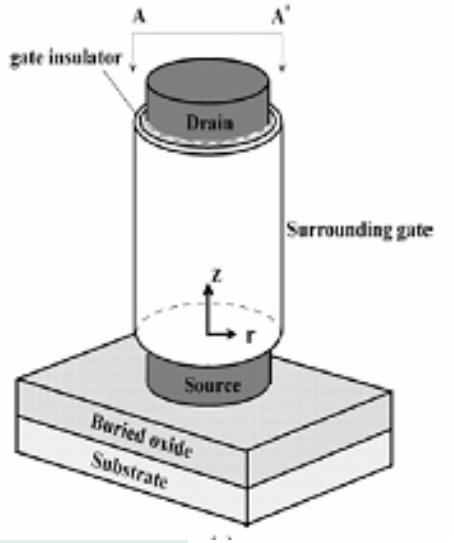
Necessity for still increasing the complexity (# devices AND functionality) is still a reality.

How:

- **downsizing: not for sure because of cost and acceptance. Anyway reaching a limit sooner or later.**
  - **+ practical: power density, temperature, variability, leakage power, analog design,…**
  - **+ money-making time for a generation is lengthening**
  - **+ costs: cost of fabs, cost of manufacturing if not in (very) large volumes, cost of design**

+ “it should be pretty clear to everybody that Moore’s law, if it is not dead already, is going to die” [MAXIM’s CEO]
+ fundamental: thermodynamics, quantum mechanics, electromagnetics,…

- larger die sizes, possibly on not the most possible advanced processes (current-generation geometries)
- 3D gates, e.g. Surrounding Gate Transistor (SGT)
- going manycores: the number of transistors is still increasing, but the source of performance increase is no more coming from the clock speed, power, instruction-level parallelism:



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3D (packaging, process)

- mixed-technology integration:
  best native process for each part (layer),
  e.g. 65nm digital, 180nm analog

- heterogeneous integration, e.g. silicon, III-V

- cost: use of current-generation geometries

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3D: Si + TSVs

In addition:

- interconnects: shorter, so power savings, increased performance

- I/Os: less I/Os, so less power (e.g. 8051 + memory stack: up to 90% power reduction

- increase the level of modularity and reusability: dedicated TSV slices in various technologies

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but:

- no power savings if use of current-generation geometries

- CAD software including TSVs

- keep out distance (no transistor around TSV)

- partitioning level

- thermal issues
  - + increased density, so potentially hot spots, electromigration acceleration
  - + thermal management theory: multiple sources [M.N. SABRY]
  - + thermal resistance of TSVs
  - + thermal vias [S. SAPATNEKAR]

3D organic electronics: 3D Si plus

- cheap

- large area

- mixed applications: electronics, sensors, RFID, PV, batteries,… as in 3D Si

- folded, stacking of layers

- flexible

- biocompatible for BioMed applications

- minus: speed (but research ongoing to transfer Si ICs from wafer to flexible substrate)

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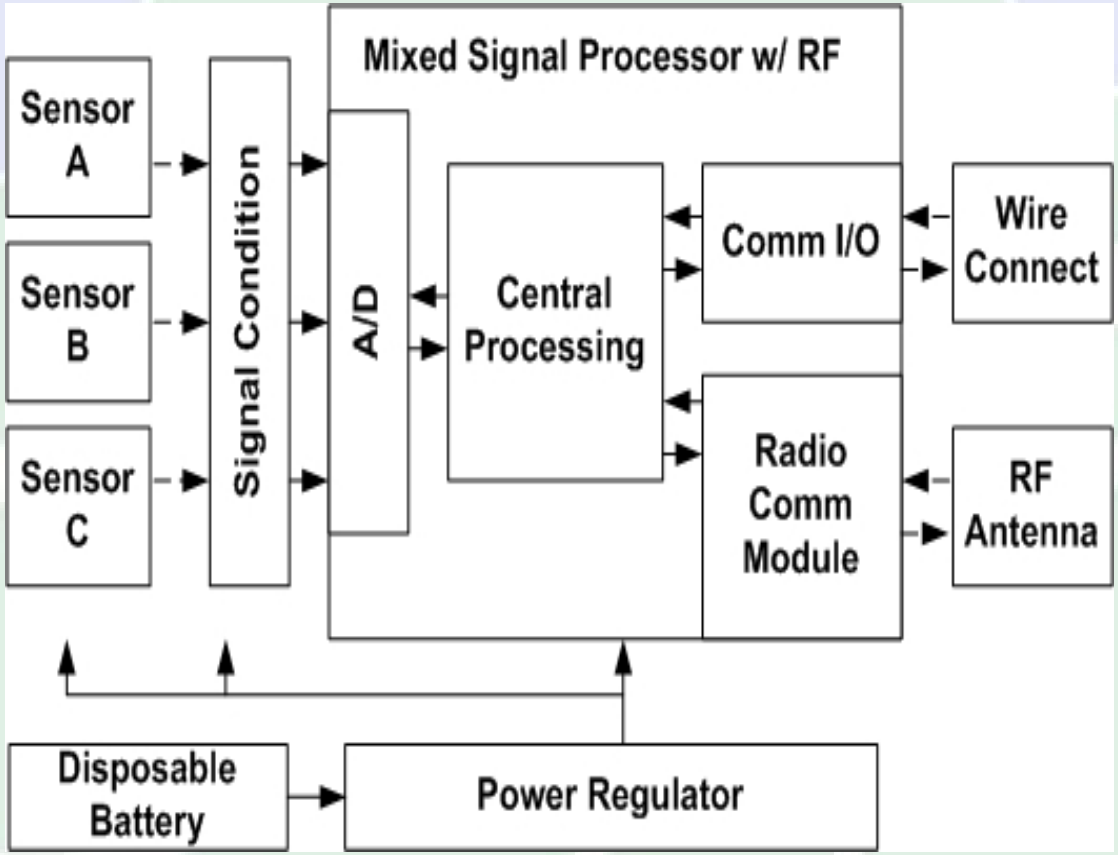
Example: multilayer polymer microsensor system

B. KAMINSKA et al, SFU, Canada

IEEE Trans. on BIOCaS



[courtesy of B. KAMINSKA]

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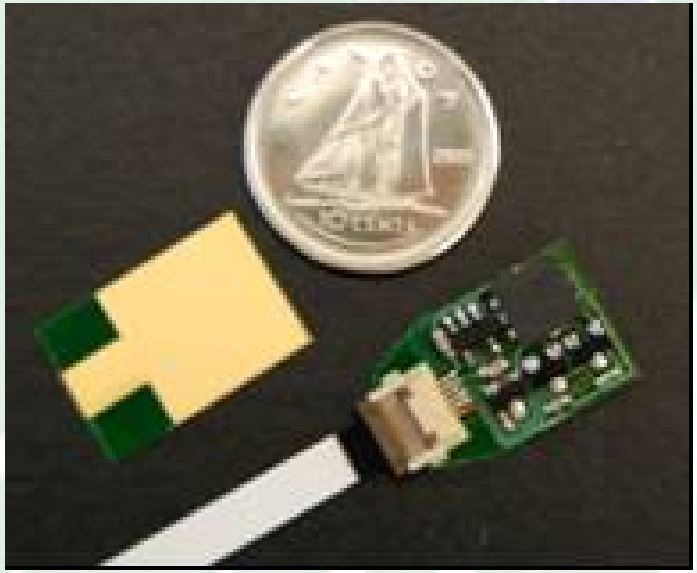
Prototype: ECG and body positioning



Flexibility: skin tissue conformity

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3D @ CMP

1st run at TEZZARON 2009 including 5 Labs France, 6 Labs Italy, 1 Lab USA plus CMP (private run)

Later:

+ TEZZARON (Chartered)

+ LETI (STMicroelectronics plus Austriamicrosystems)

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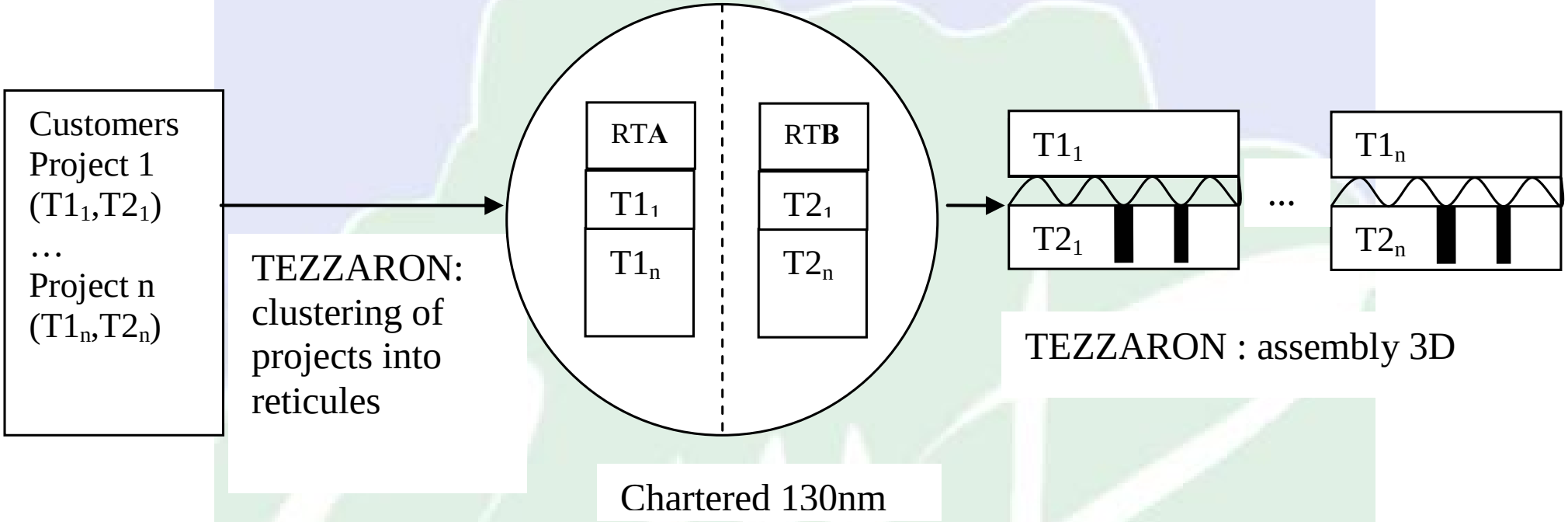
TEZZARON



- same wafer: homogeneous process
- interconnect technology: tungsten

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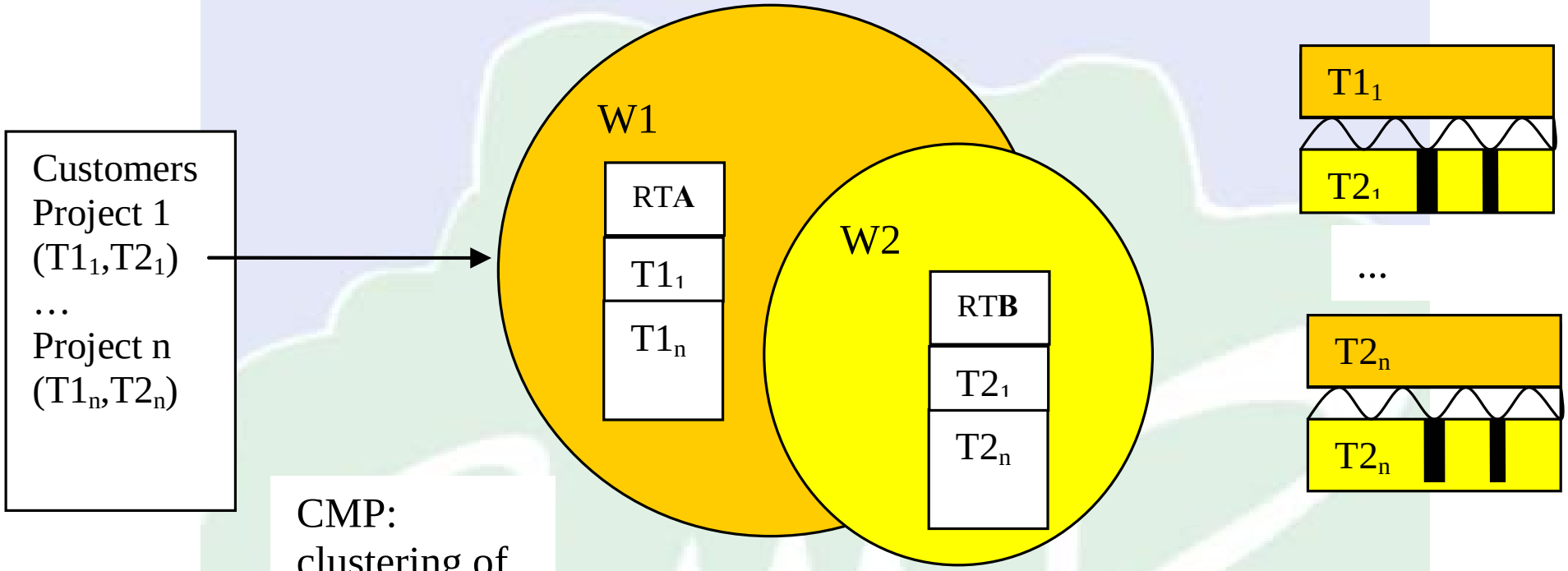
CMP / LETI



CMP:
clustering of projects into reticules

LETI :
assembly 3D

STMicroelectronics 65nm
Austriamicrosystems .35 µ

- **Different wafers: heterogeneous process**
- **interconnect technology: copper**

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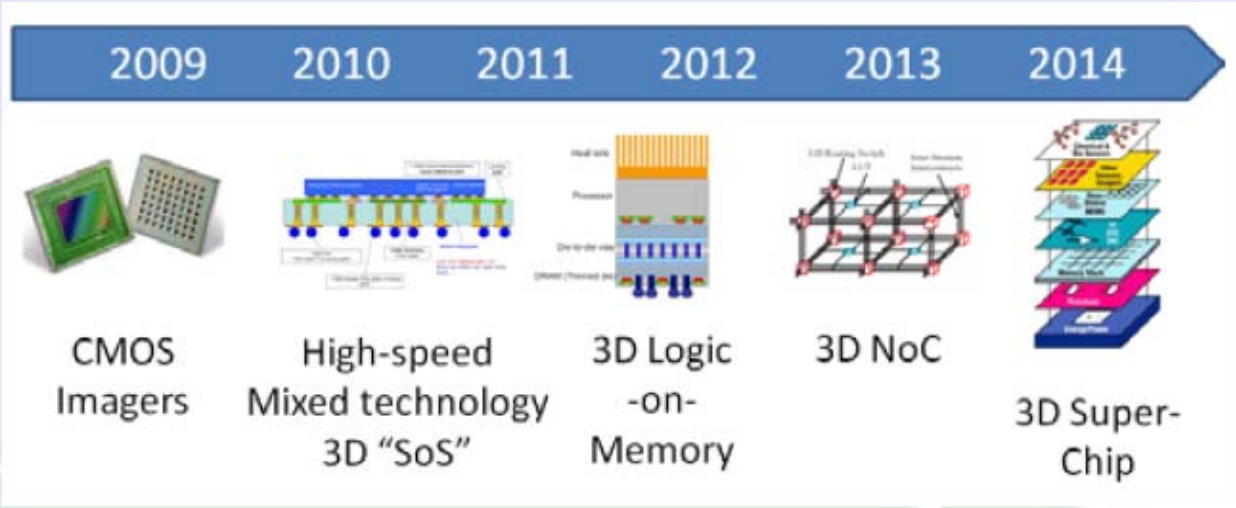
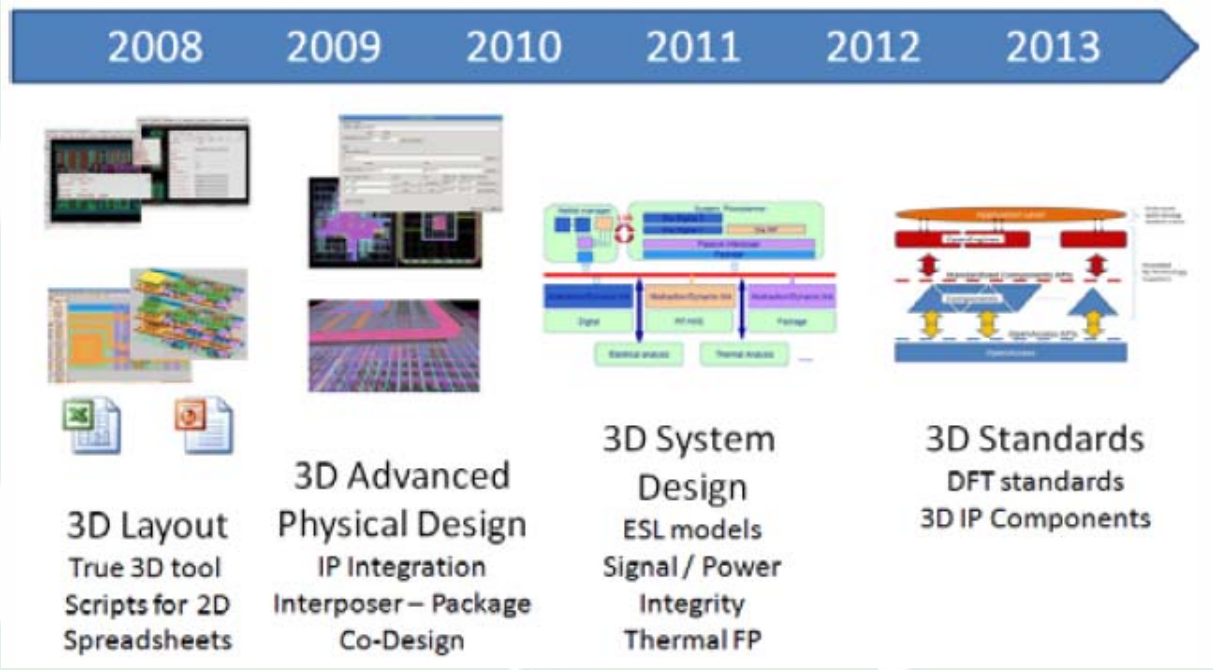
Roadmaps



Products



EDA tools

[L. McIlrath, R3Logic]

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Ultra Low Power: Magnetic Logic Circuits

Background

Applications

@ CMP

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Background

Magnetic circuits: a long way to go....

- magnetic bubbles 70s?
- arithmetic circuits 1968, U. of Washington...
- GMR
- MTJ

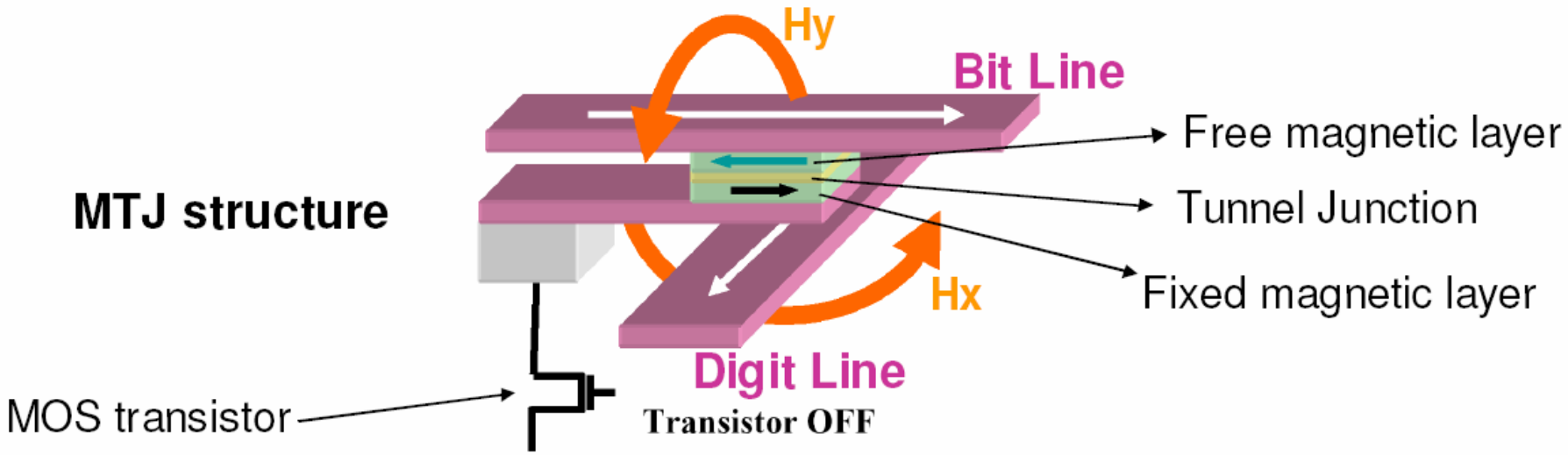
MTJ, Magnetic Tunnel Junction

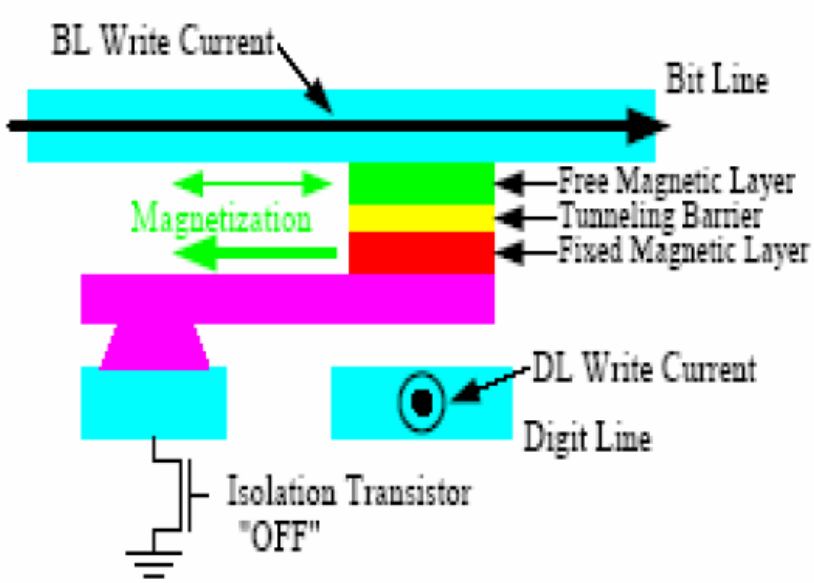
load of the electron → spin of the electron

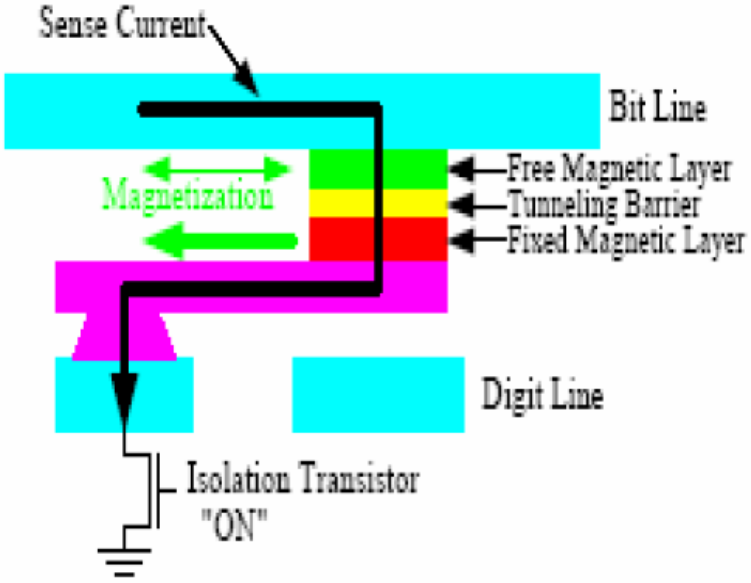
2 ferromagnetic layers:

- parallel magnetization directions: low resistance R_P
- anti-parallel magnetization directions: high resistance R_{AP}

CMOS - MTJ Process







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Applications

MRAM

MRAM above CMOS

Logic-in-Memory

M-FPGA

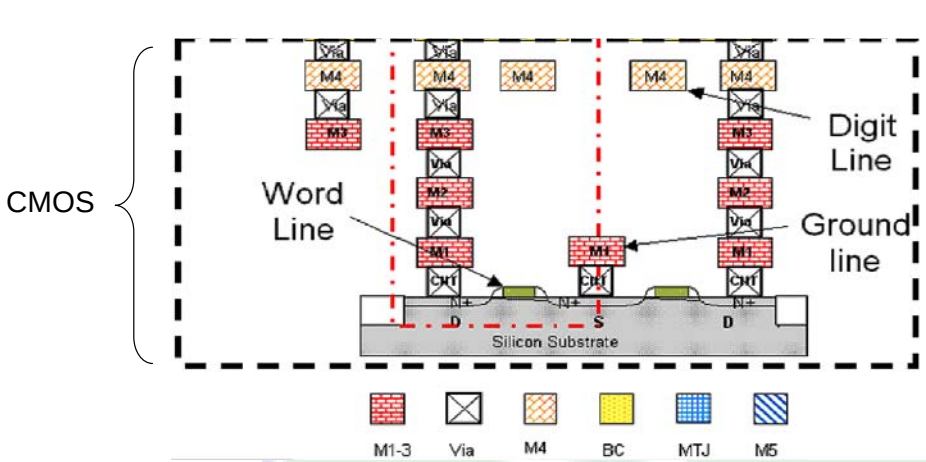
M-TCAM

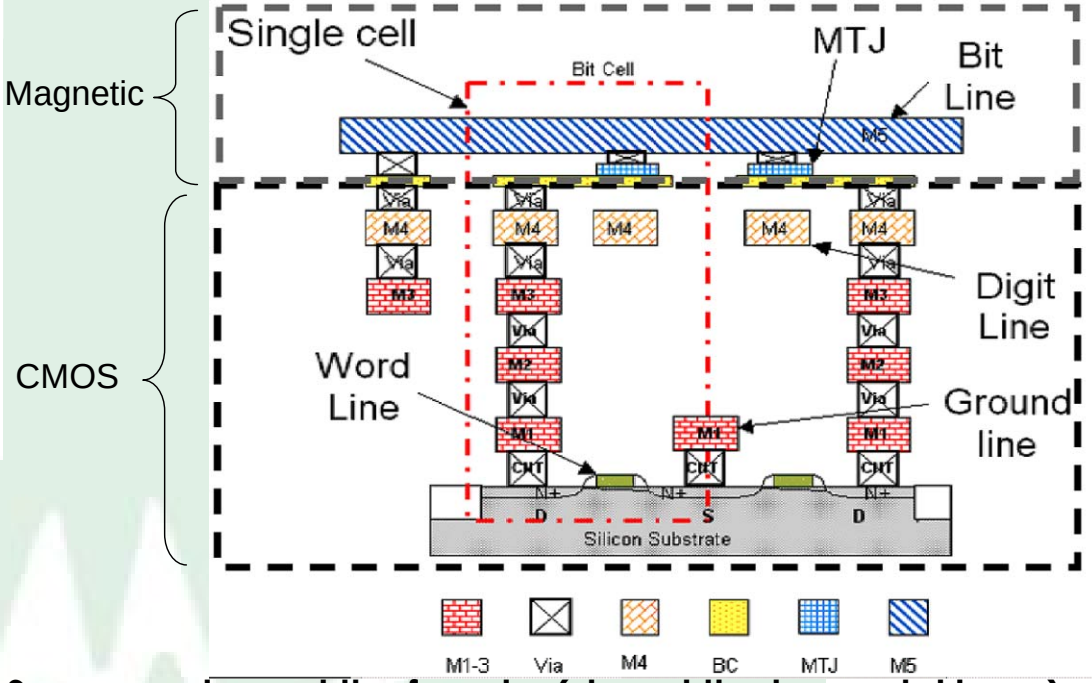
MRAM

- static (SRAM)
- very dense
- very fast (35 ns)
- very low power

MRAM above CMOS

CMOS process done at the foundry (stop at the top metal layer)





CMOS process done at the foundry (stop at the top metal layer)

Magnetic post-process + metallization + passivation + pad openings

high density

short interconnections

important because the % of eRAMs in SoCs is increasing dramatically (90% in 2010?)

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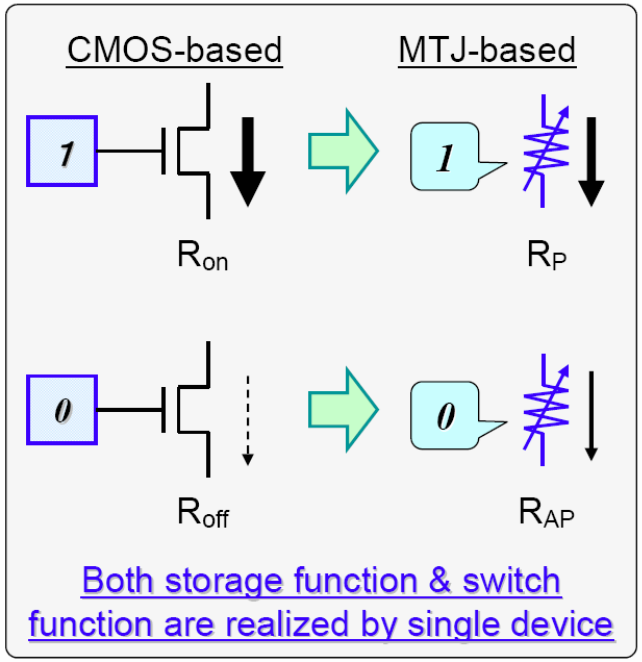
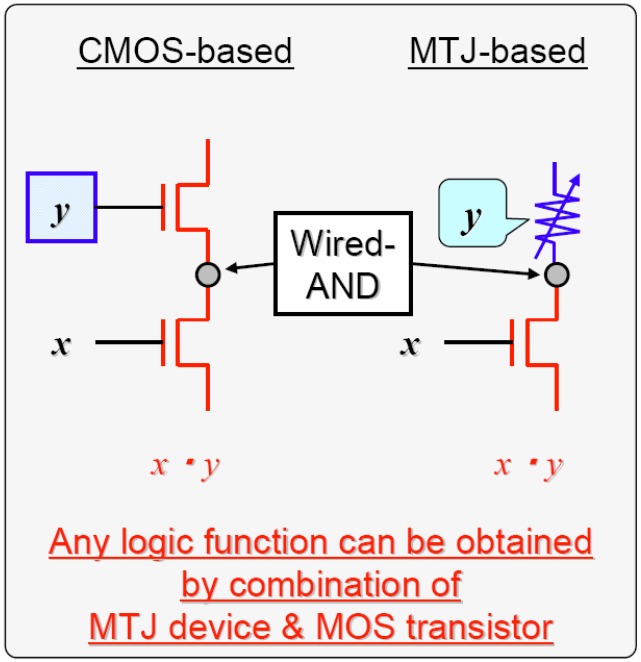
Logic-in-Memory: MCMOS

Non volatile memory elements over logic circuitry.
- **ultra low power: no power consumption if no state change**
- **keep the state if power disappears: no need to reboot from mass memory**

Logic function using MTJ device





Combination of MTJ devices & MOS transistors realizes logic/arithmetic function compactly

[from Tohoku Univ.]

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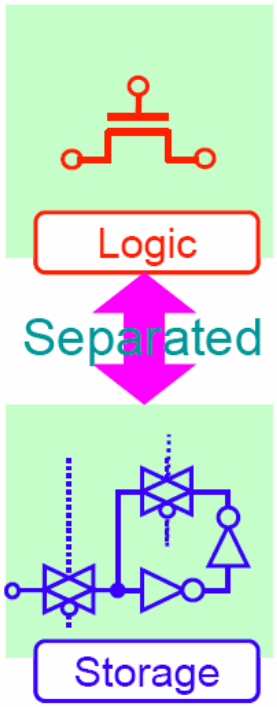
CMOS logic vs. MTJ logic

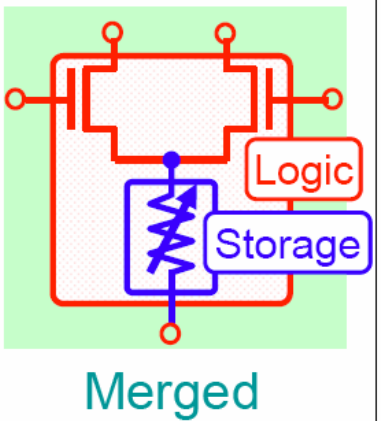
CMOS logic



◆Logic & Storage by **electric charge**
◆Logic circuit is composed of *MOS transistors*.
◆MOS device itself has no storage capability.
◆Power supply is continuously applied for data storage.(**Volatile**)

MTJ logic

Example using MTJ device



◆Logic & Storage by **electric charge** & **magnet**
◆Variable resistance by magnetization directions
◆Logic circuit is composed of ***transistors*** and ***resistors***.
◆Magnetization directions are maintained under power-off state.
(**Nonvolatile**)

Combine MTJs with MOSs ⇒ High-performance & Multi-function

[from Tohoku Univ.]

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e.g. full adder, based on .18µ CMOS

- MTJs on top of M4
- manufactured
- CMOS vs. MCMOS

	CMOS	MCMOS
Dynamic power (@ 500 MHz)	71.1 µW	16.3 µW
Static power	0.9nW	0.0nW
Area	333 μm^2	315 μm^2
Device count	42 MOSs	34 MOSs + 4 MTJs

➔ Dynamic Current-Mode Logic

➔ V_{th} variation compensation

(➔ RF circuits, LED, ...)

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M-FPGAs

usual FPGAs:

- SRAM-based, volatile, reprogrammable
- anti-fuse, non volatile but not reprogrammable

trends:

- SRAM-based: dynamical/partial reconfiguration capabilities
- anti-fuse: embedded configuration memory but not on the same chip

M-FPGAs: non volatile, reprogrammable

- Iowa State University, 2000
- LIRMM, IEF, Spintec, France

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Context

FPGAs often used as an alternative to ASICs.
But, new trends :

- Some SRAM based FPGAs feature dynamical/partial reconfiguration capabilities
- Some Flash based FPGA propose non volatile embedded configuration memory (configuration ready at power up)

These features are not yet available on a same chip.
Major difference between these FPGAs : memory type

- Flash is slow
- SRAM is volatile

⇨ **need to use new memory technology**

MTCAM

- non volatile
- ternary CAM: 0, 1, X (don't care) matches
  SPINTEC Lab, France
- CMOS 5M 1P, 130 nm
- 1 cell 1x2 MTCAM: 300 F^2, 1 µW
- CMOS vs. MCMOS: 16 MOSs vs 6 MOSs+ 2 MTJs

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MCMOS @ CMP

CILOMAG Project: IEF Lab, SPINTEC Lab, LETI, LIRMM Lab, CROCUS Technololgy, CMP

Silicon foundries: Austriamicrosystems 0.35 µ CMOS
STMicroelectronics 130 nm CMOS

MRAM postprocess: LETI

DK on .35 µ CMOS

- Design-Kits on Austriamicrosystems 0.35um CMOS :
- Electrical model developed by SPINTEC (Grenoble) (Spectre model and Verilog-A model)
- Layout, DRC, LVS, P-cell developed by CMP (Grenoble) (DRC / LVS on Assura)

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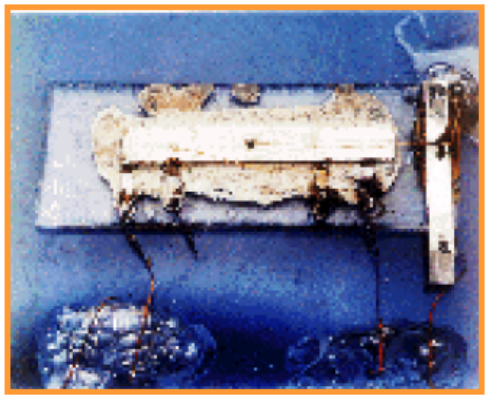
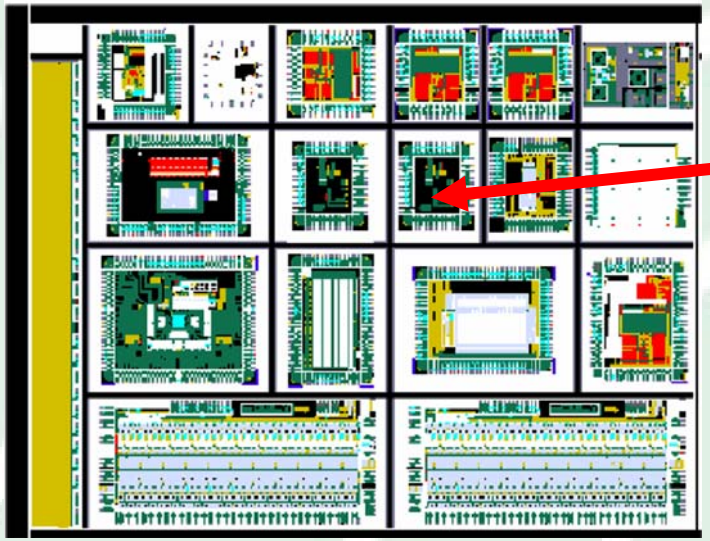
CMOS-MTJ: First Prototype

- Designer : LIRMM (Montpellier)
- Application : Non Volatile FPGA prototype.
- CMOS process : Austriamicrosystems 0.35um CMOS
- CMP MPW run : A35C7-2
- MRAM Post-Process : INESC (Portugal)

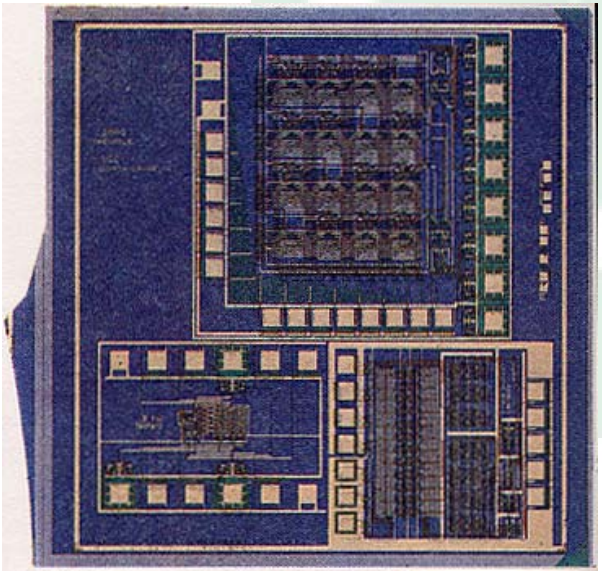
First Point Contact Transistor (1947)



First Integrated Circuit (1958)



First MCMOS Prototypes ever made in a MPW run CMP (2008)



First MPW CMP (1981)

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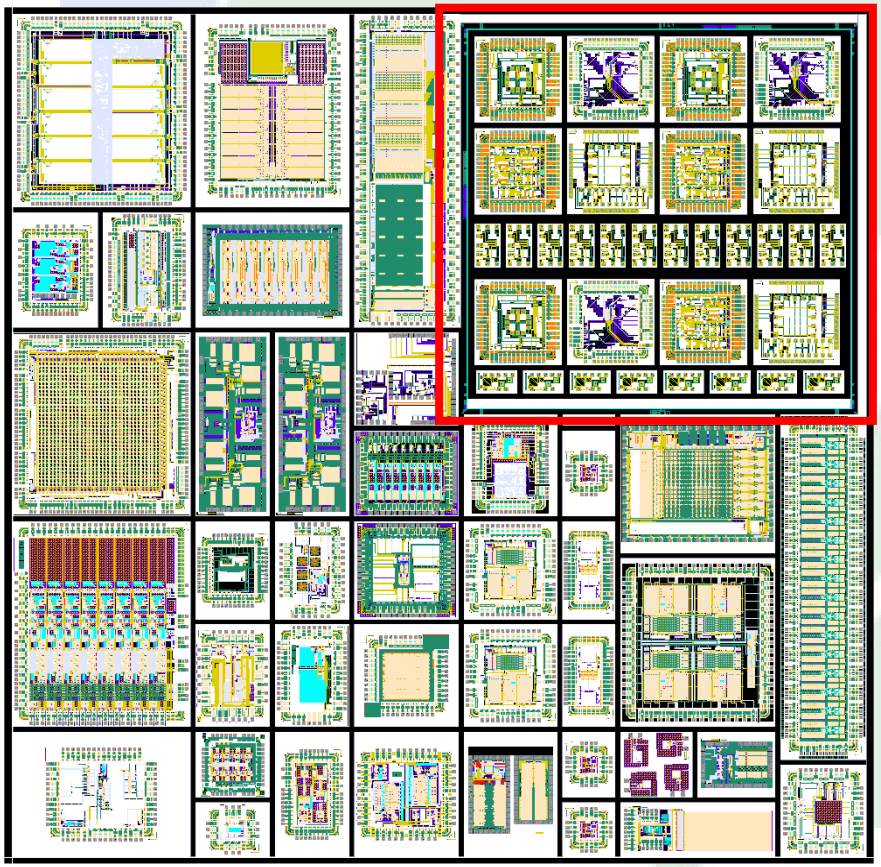
CMOS-MTJ Second Prototype

- Designers : All CILOMAG partners
- Application : Different block architectures.
- CMOS process : Austriamicrosystems 0.35um CMOS
- CMP MPW run : A35C8-2
- MRAM Post-Process : LIMN / LETI (Grenoble) Delivery : Q1 2009



Embedded CMOS MTJ MPW
in a CMOS MPW

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CMOS-MTJ Third Prototype

- Designers : All CILOMAG partners
- Application : Different block architectures.
- CMOS process : STMicroelectronics 130nm CMOS
- CMP MPW run : S13C9-2 (April 2009)
- MRAM Post-Process : LIMN / LETI (Grenoble) Delivery : Q4 2009

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Address other Communities: e.g. BioMed

Why BioMed applications?

- **better health for everybody**
- **aging of the population**
- **ICs and MEMS can bring a lot**

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ICs and MEMS for BioMed

- All possible kinds of BioMed applications: NO
- Examples of applications using standard processes
  - no custom process
  - design only
    * CMOS for Neurosciences
    * CMOS for prosthesis
    * Bulk micromachining (ORL)
    * MUMPS
      blood sampling
      microgripper for cell manipulation
      CardioMEMS
      PillCam
    * ASIMPS
      bone stress sensor
    * System view: science and beauty

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CMOS ICs for neurosciences

- to interface neurons
- to mimic neurons: ANN

CMOS ICs for prosthesis

- retinal prosthesis

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CMOS ICs for interfacing nerve cells and brain tissue

Coupling ion channels and transistors of chips

ions in liquid water-electrons in solid silicon

EOS capacitors: activation of the ion channels

EOS FET: detection of open channels

EOS: electrolyte / oxide / silicon

P. FROMHERZ, Max Planck Institute, Munchen

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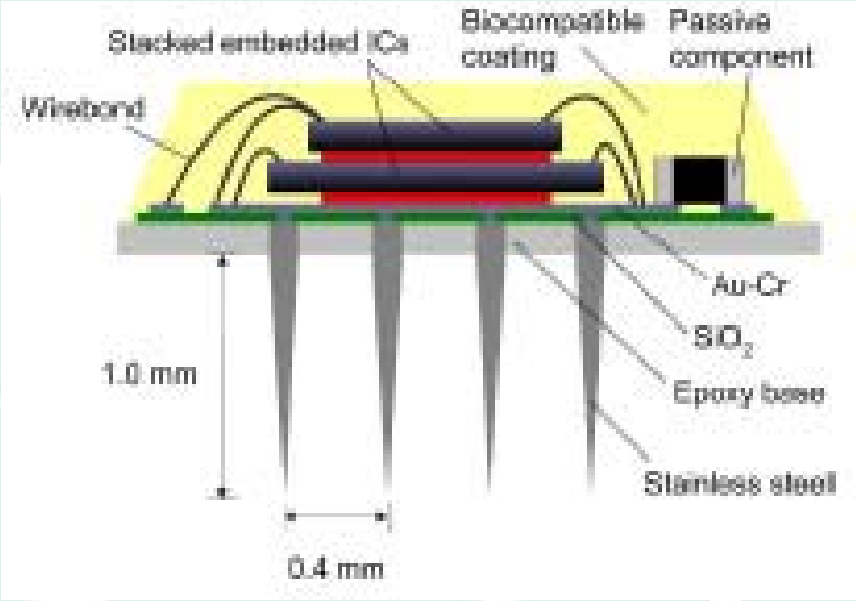
CMOS ICs in vivo for neural interfaces

M. SAWAN et al., Ecole Polytechnique de Montreal

Sensing and stimulating cortical areas (prosthetics applications)

Pb: minimize size of implant, maximize spatial resolution



Flip-chip connection between post-processed stainless steel array of electrodes and chips vertically integrated (to avoid inflammation and cerebral oedema)

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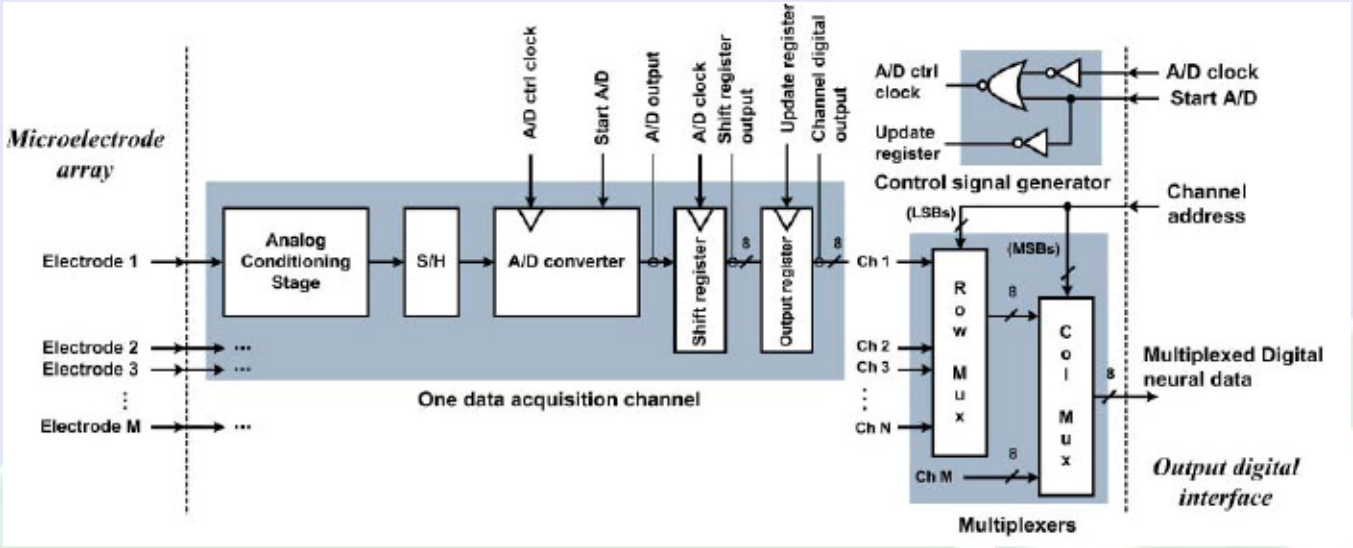
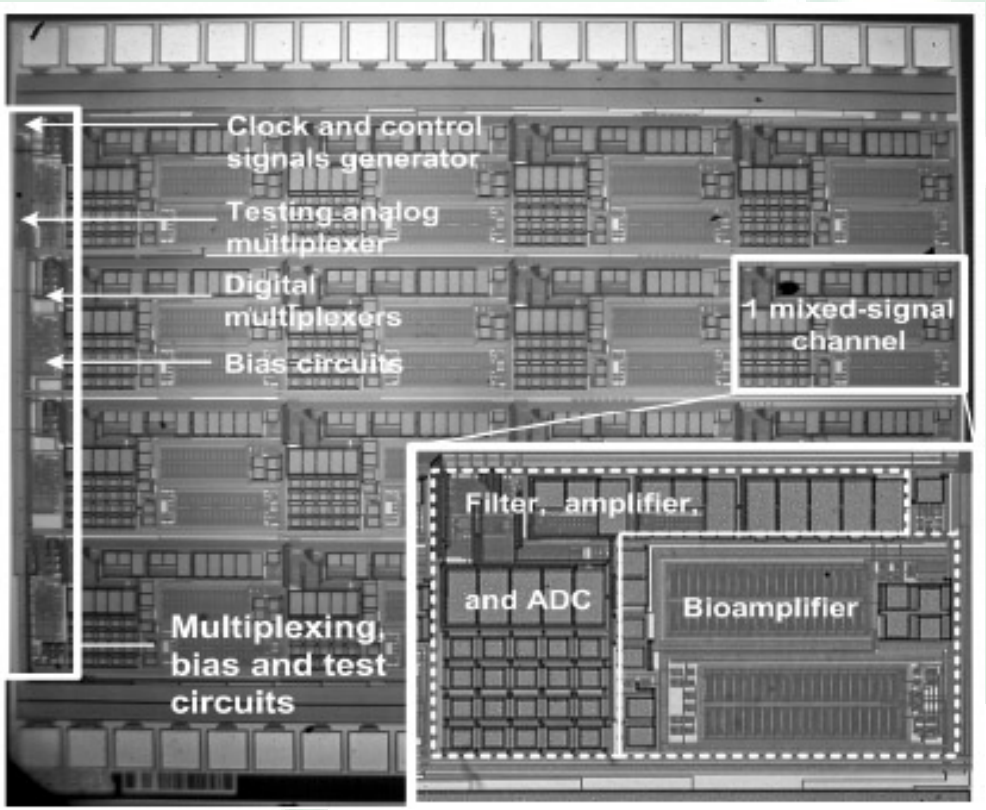
each channel: data acquisition, signal conditioning





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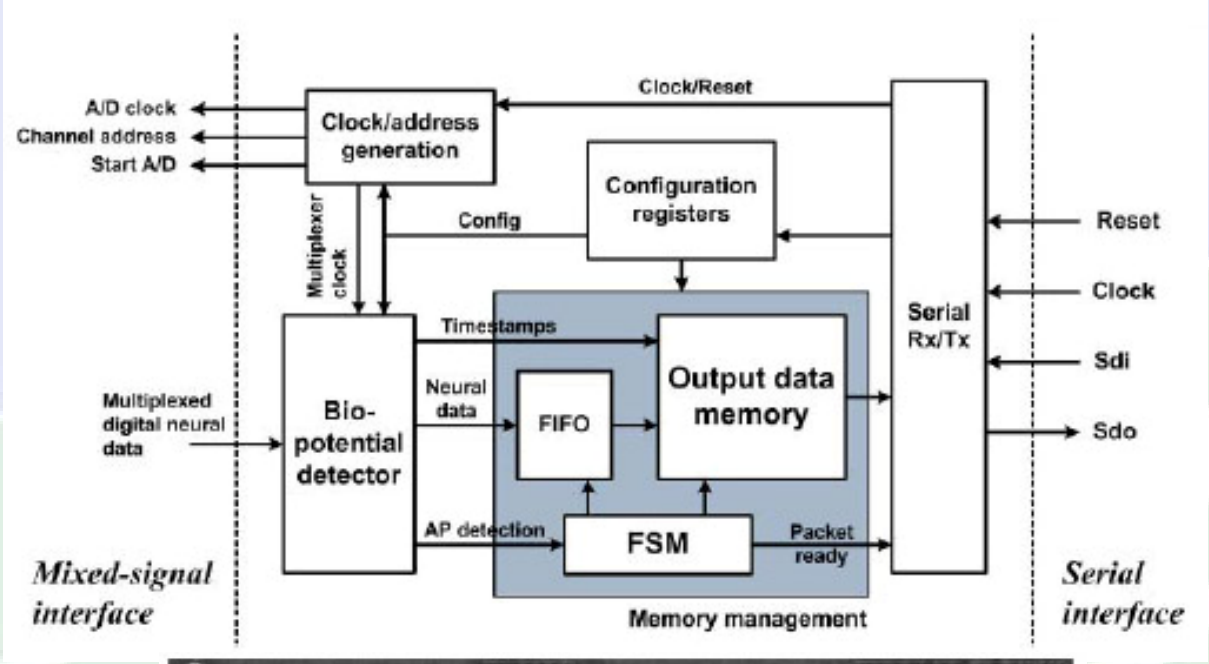
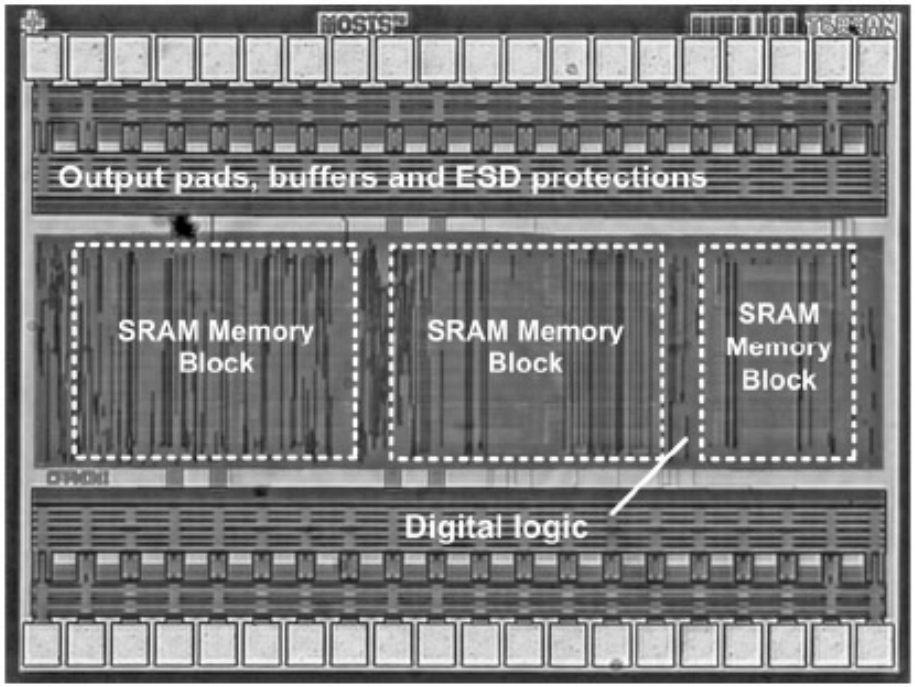
digitization, action potential detection, serial communication to host interface





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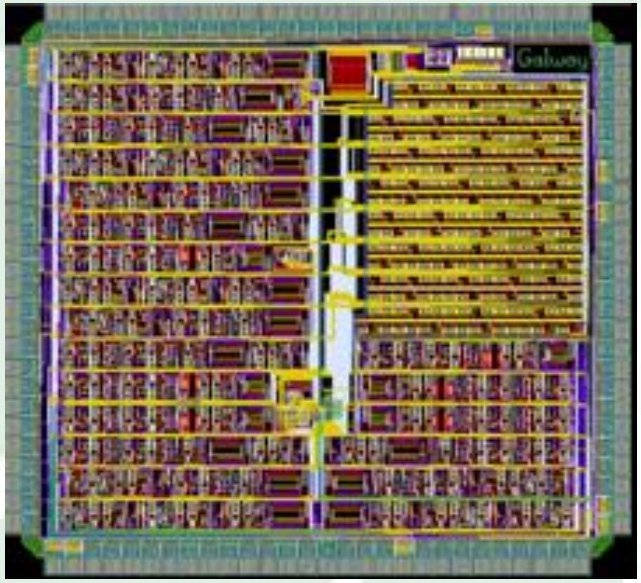
CMOS ICs to mimic neurons

artificial neuron networks

computing techniques

hybridization with a real neuron

Sylvie RENAUD, Univ. of Bordeaux, France



Neuromimetic circuit, 5 neurons

[courtesy of Univ. of Bordeaux]

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FACET project

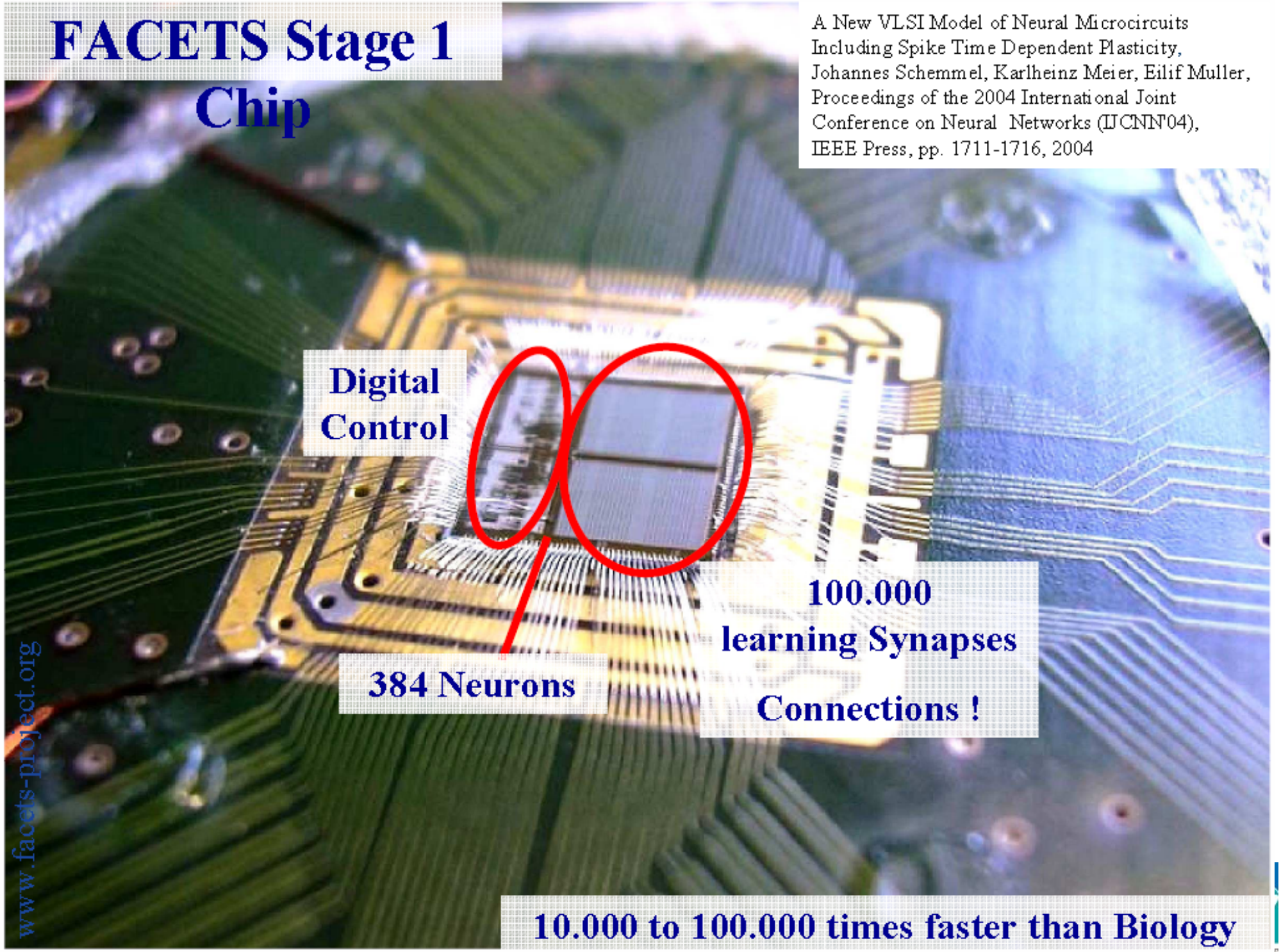
Karlheinz Meier

Ruprecht-Karls-Universität Heidelberg

FACET 1: 384 neurons, 100,000 synapses

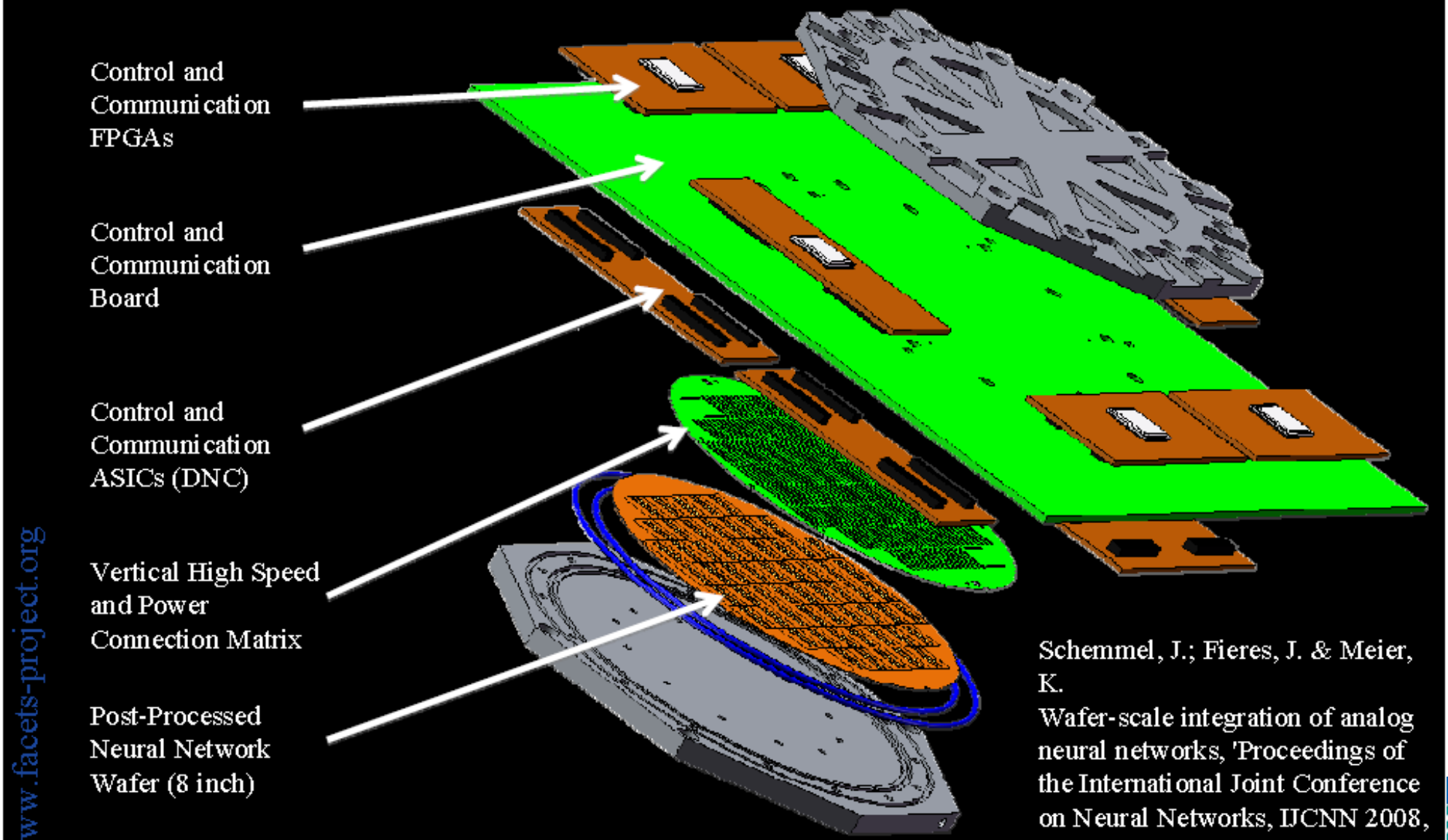
FACET 2: 200,000 neurons, 50 M synapses

FACETS Stage 1 Chip



A New VLSI Model of Neural Microcircuits Including Spike Time Dependent Plasticity, Johannes Schemmel, Karlheinz Meier, Eilif Muller, Proceedings of the 2004 International Joint Conference on Neural Networks (IJCNN'04), IEEE Press, pp. 1711-1716, 2004

Neural Processing Unit, up to 200.000 Neurons, 50.000.000 Synapses
Separate Neural Circuits and Monitoring/Readout/Control



Schemmel, J.; Fieres, J. & Meier, K.
Wafer-scale integration of analog neural networks, 'Proceedings of the International Joint Conference on Neural Networks, IJCNN 2008, pp. 431-438.

www.facets-project.org

CMOS ICs for prosthesis: Retinal prosthesis

E. DRAKAKIS et al., Imperial College, London, UK

- High-dynamic range CMOS image sensor
- Each pixel = independent oscillator, frequency proportional to local light intensity
- Experimental retina: 9x9 pixels

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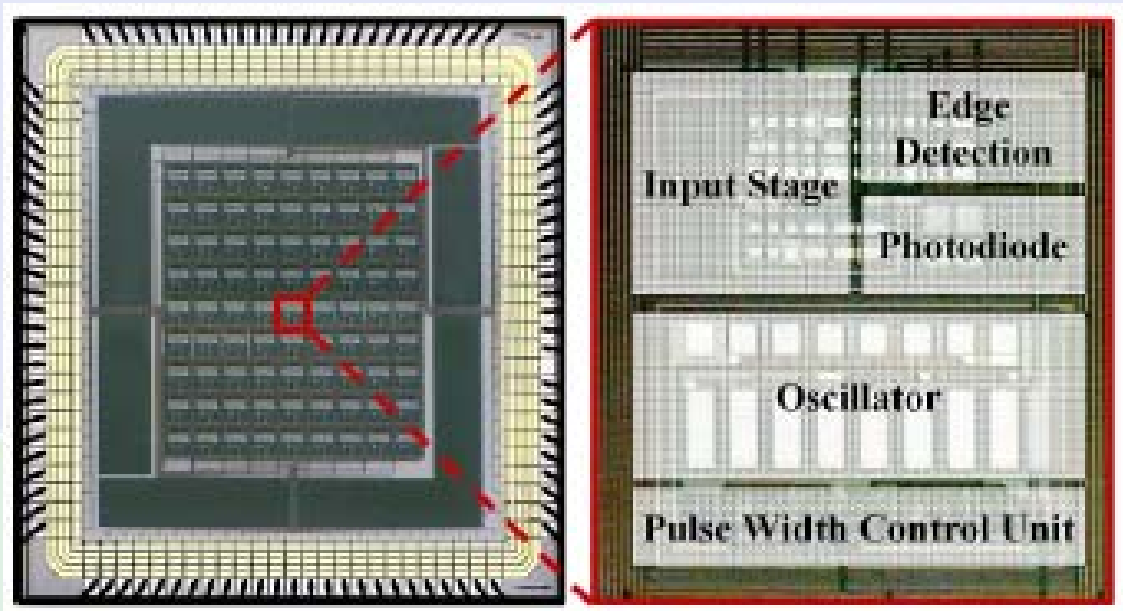

9x9 pixels, AMS CMOS .35 µ Opto process

[courtesy of E. DRAKAKIS et al.]

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Bulk Micromachining for BioMed

Example: Apparatus for in-situ monitoring during the middle-ear surgery
Acoustic sensor for ORL surgery
ongoing at TIMA Labs, Grenoble, Libor Rufer et al.

Problem: middle ear surgery, to correct hearing loss or disease by re-connection between tympanic membrane and oval window: ossicular chain reconstruction
per-operatory monitoring, otherwise…. redo
➔ vibration sensor, audible frequency, to check the sound transfer in real time

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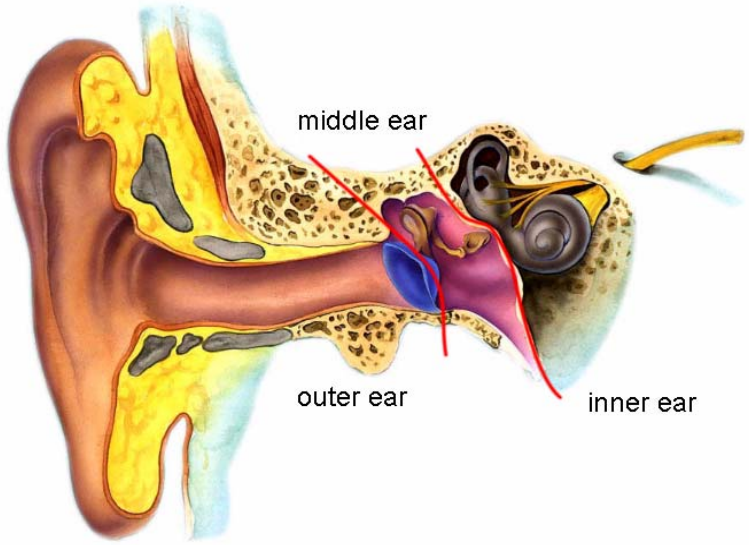
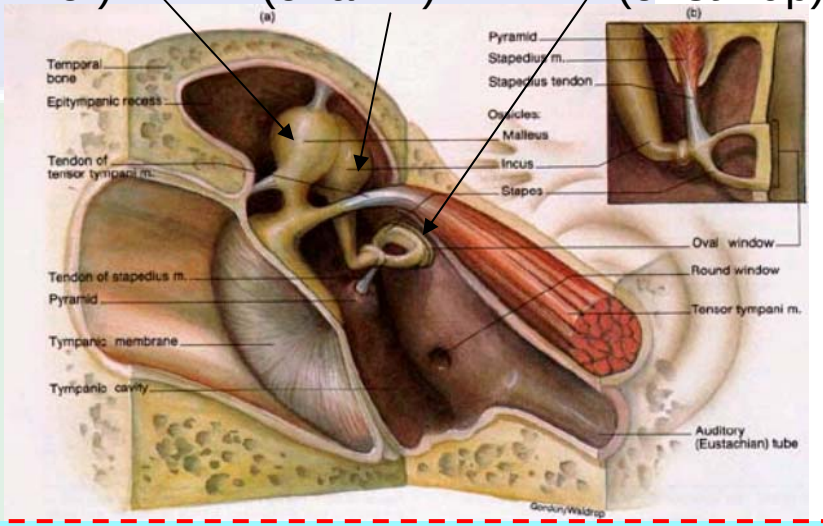


Malleus (or hammer)

Incus (or anvil)

Stapes (or stirrup)

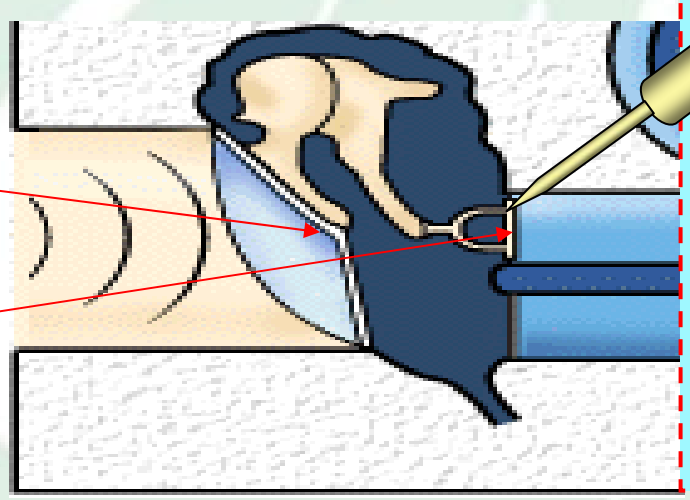


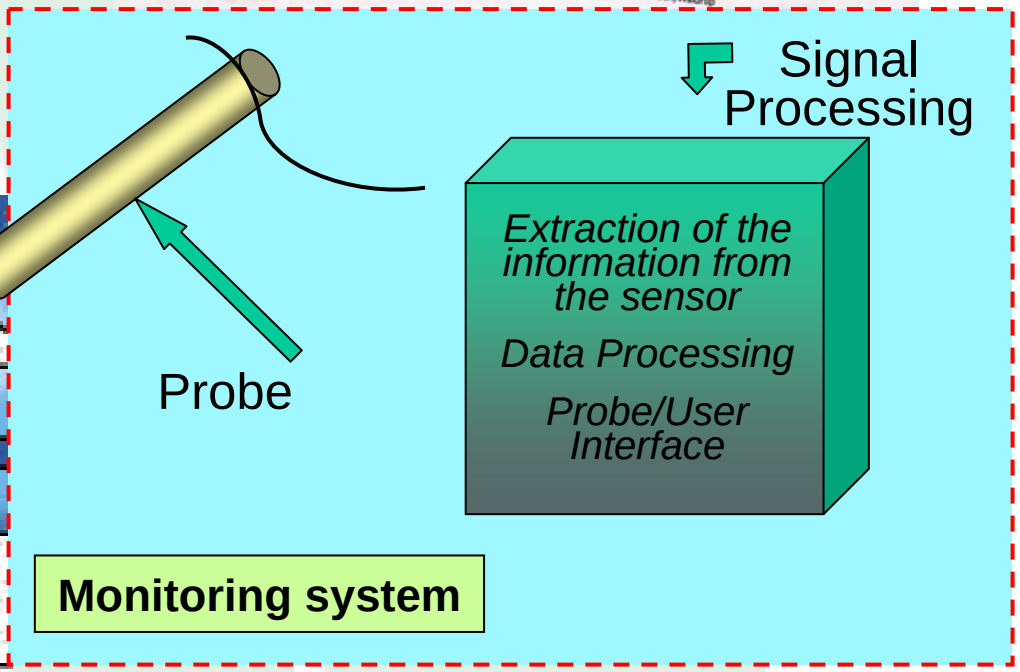
Simplified Function of the middle ear:

Sound Energy Transfer:

From Eardrum

To Oval Window





Human ear and basic principle [courtesy from TIMA Labs]

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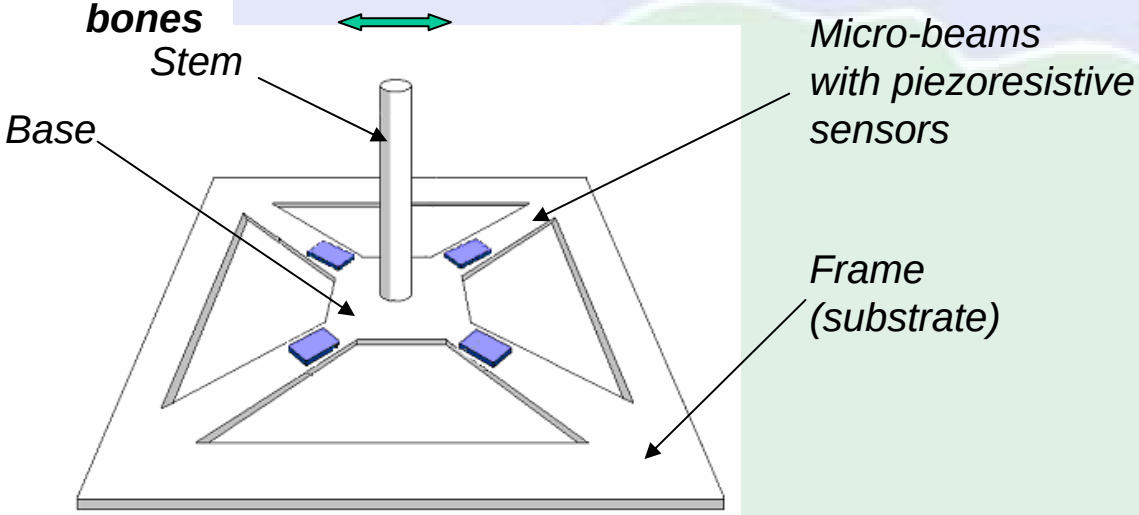
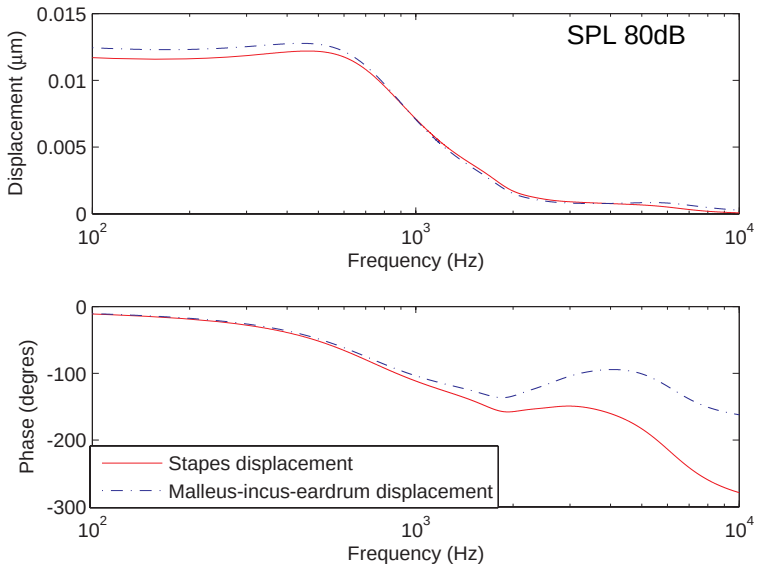
Basic idea:

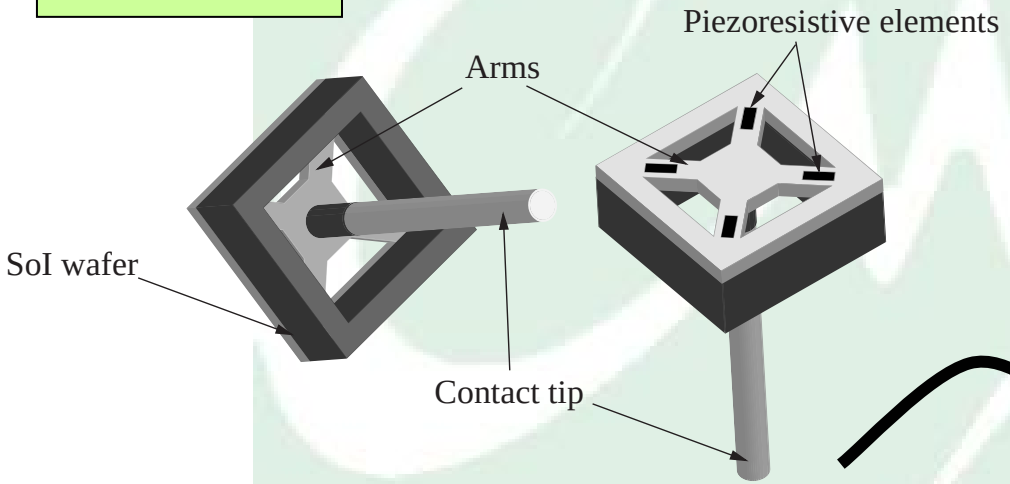
Movement induced by ear bones



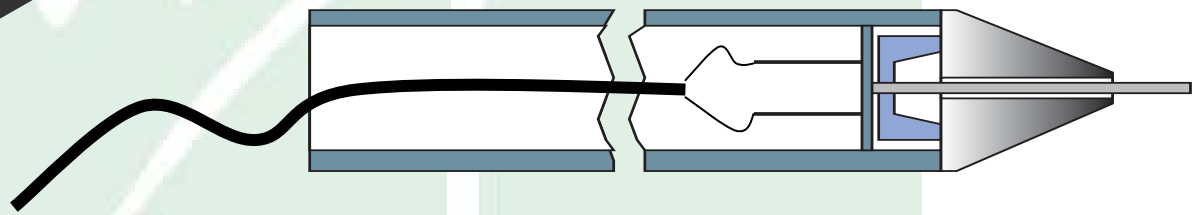
Modeling:



Realization:



Packaging:



Sensor structure [courtesy from TIMA Labs]

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MUMPS for BioMed

2 research examples from CMC

U. of Calgary, Karan Kaler, Martin P. Mintchev
Electronic Mosquito™

Dalhousie University, Ted Hubbard et al.,
microgripper for cell manipulation

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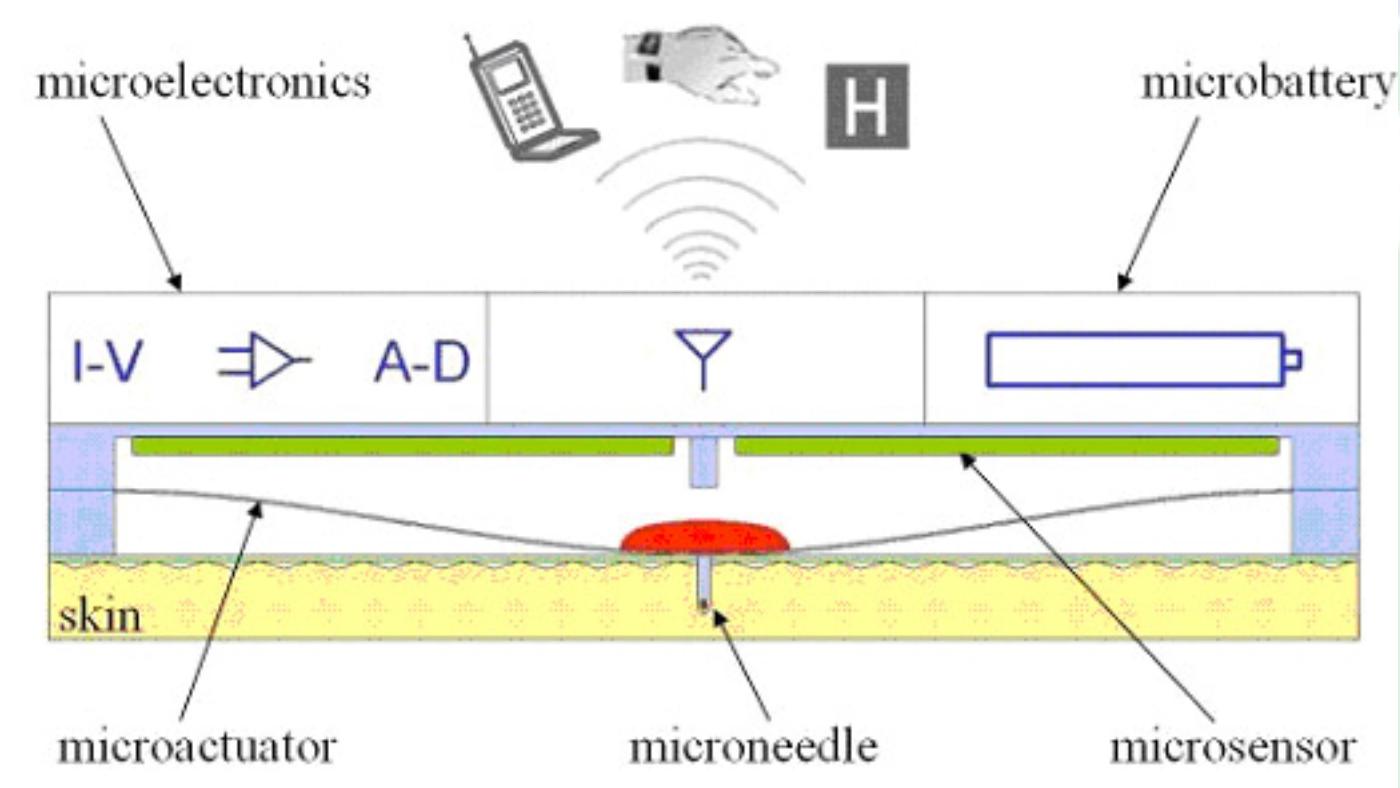
Electronic Mosquito™

Semi-invasive MEMS for blood sampling and analysis

➔ **analyze, transmit to wireless device, control insulin infusion pump, for glucose balance of a diabetic patient**



e-Mosquito™ [courtesy from the University of Calgary]

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small volume blood

single-use, disposable

array of 180 e-Mosquito cells: one week,
monitoring every hour.

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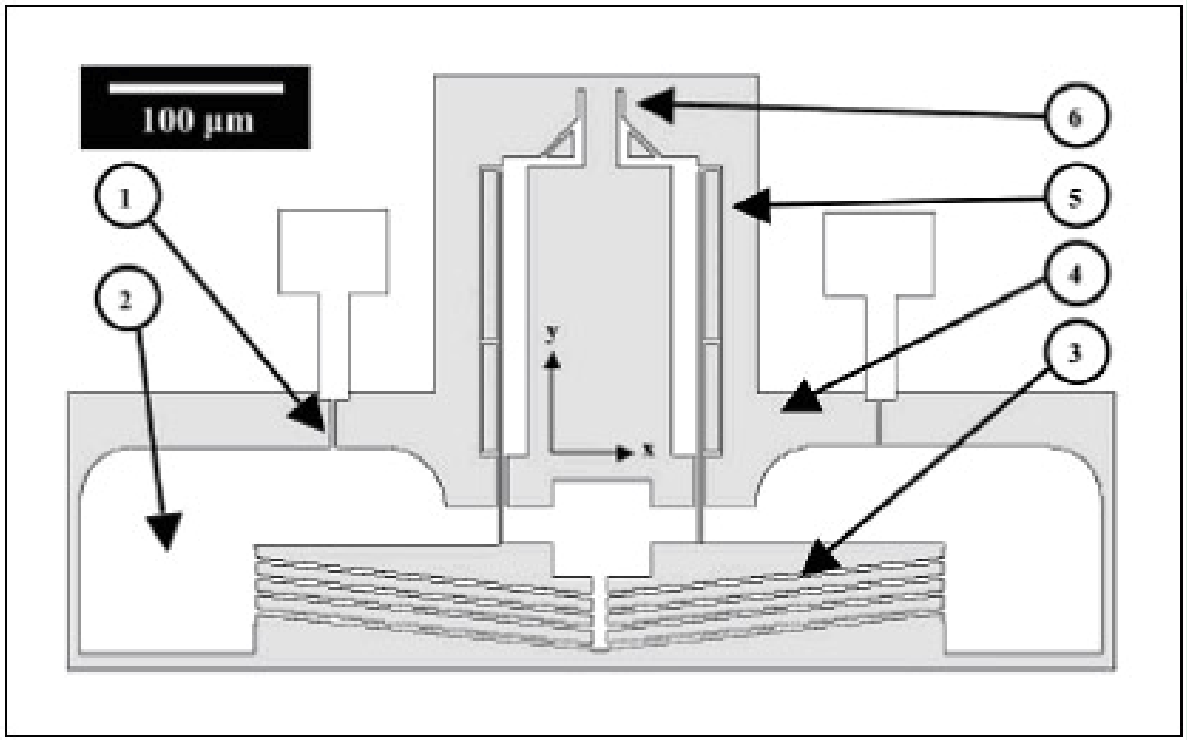
Microgripper

➔ mechanical testing of cells and bacteria, cell manipulation, medical screening,…

initial design on MUMPS, next on Microgem, SOI MEMS process from Micralyne (CMC)



Microgripper: (1) breakable tether; (2) bonding pad; (3) chevron actuator; (4) cavity; (5) amplifiers; (6) jaws [courtesy from the Dalhousie University]

5 µ spheres

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MUMPS for BioMed

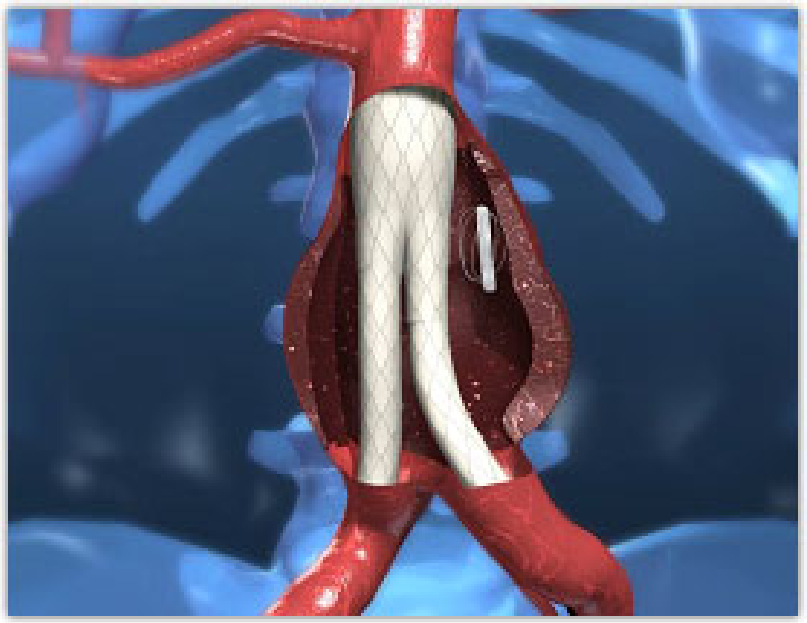
2 commercial examples

- CardioMEMS
- Given Imaging

MUMPS have served as initial test vehicles for the MEMSCAP components inside

CardioMEMS

Wireless Pressure sensor manufactured by MEMSCAP for CardioMEMS inserted during minimally invasive repair of abdominal aortic aneurysms (AAA) or thoracic aortic aneurysms (TAA), via catheter, into a patient's aneurysm sac lifetime



Wireless AAA pressure sensor from CardioMEMS

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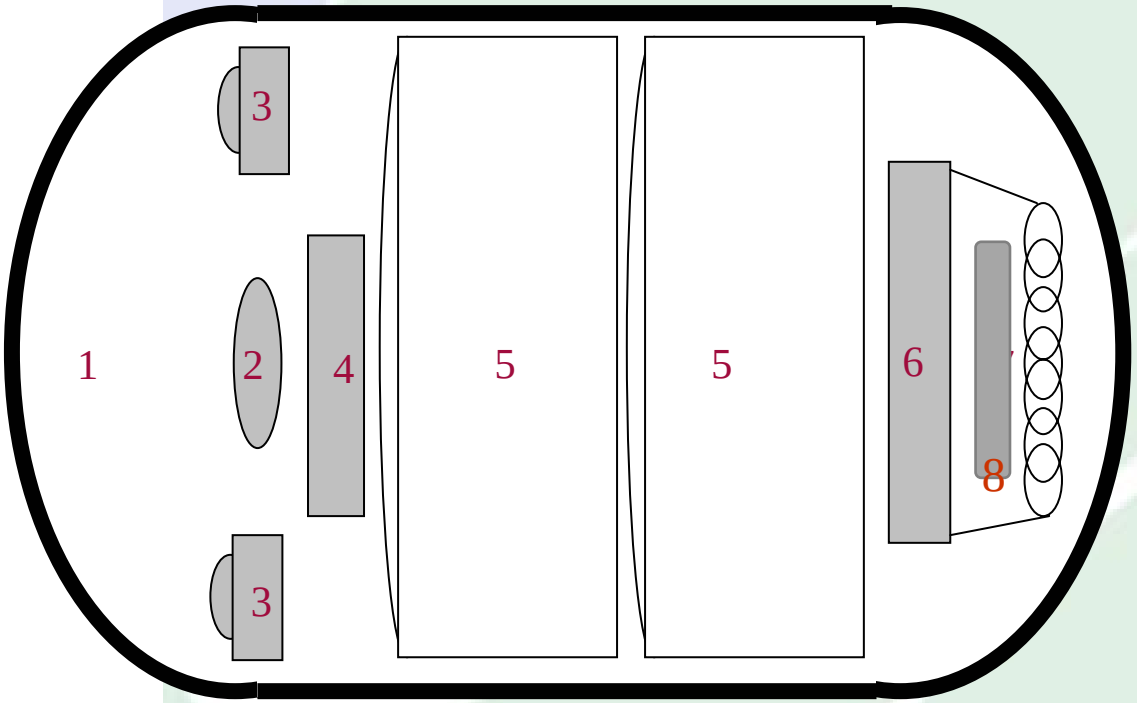
Given Imaging

Wireless imaging system in a capsule for endoscopy. Camera in a capsule captures images as it travels Images to a computer, physician can view and make a diagnostic.



1. Optical dome
2. Lens
3. Illuminating LEDs
4. CMOS imager
5. Battery
6. ASIC transmitter
7. Antenna
8. Switch

Basic structures [courtesy from Given Imaging]

PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

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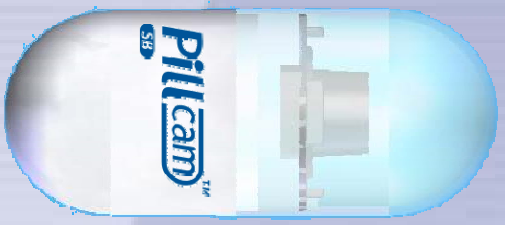
PillCam™ Products

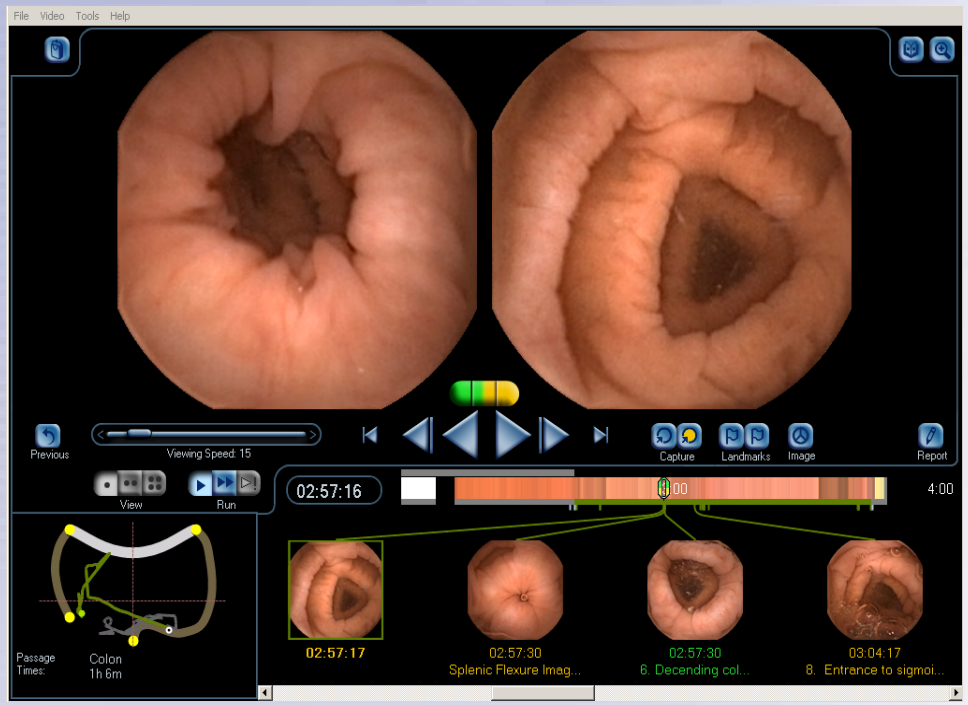


PillCam
SB

PillCam
ESO

PillCam
COLON

Agile



Proprietary Software

GIVEN IMAGING

PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

PillCam SB (small Bowl)

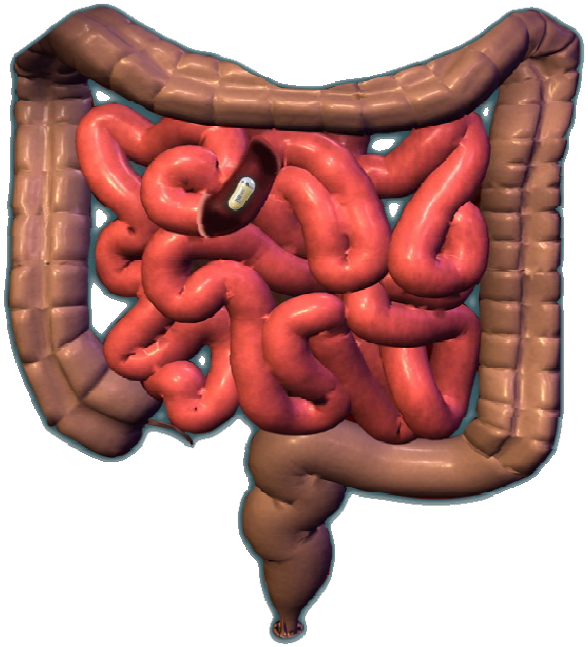
A non-invasive tool to visualize the entire small intestine

Diseases of the SB: Bleeding, Crohns, Celiac, Tumors, IBS, IBD, IDA, NSAIDS damage

PillCam SB – FDA clearance in 2001

> 8-hour operational time

Captures > 50,000 images



PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

GIVEN IMAGING

PillCam ESO (esophagus)

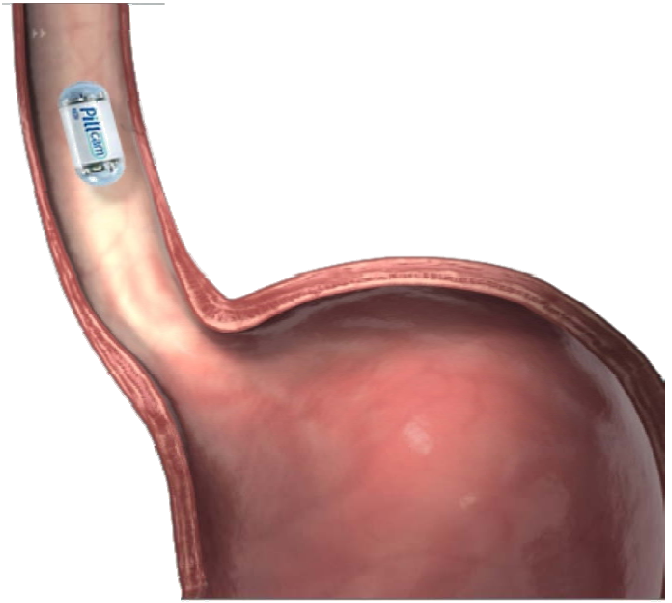
A non-invasive tool to visualize the entire esophagus

Diseases of the ESO: Heartburn, Varices, GERD, Barretts, cancer

PillCam ESO – FDA clearance in 2004

20 minute operational time

Captures ~ 11,000 images



PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

GIVEN IMAGING

PillCam COLON

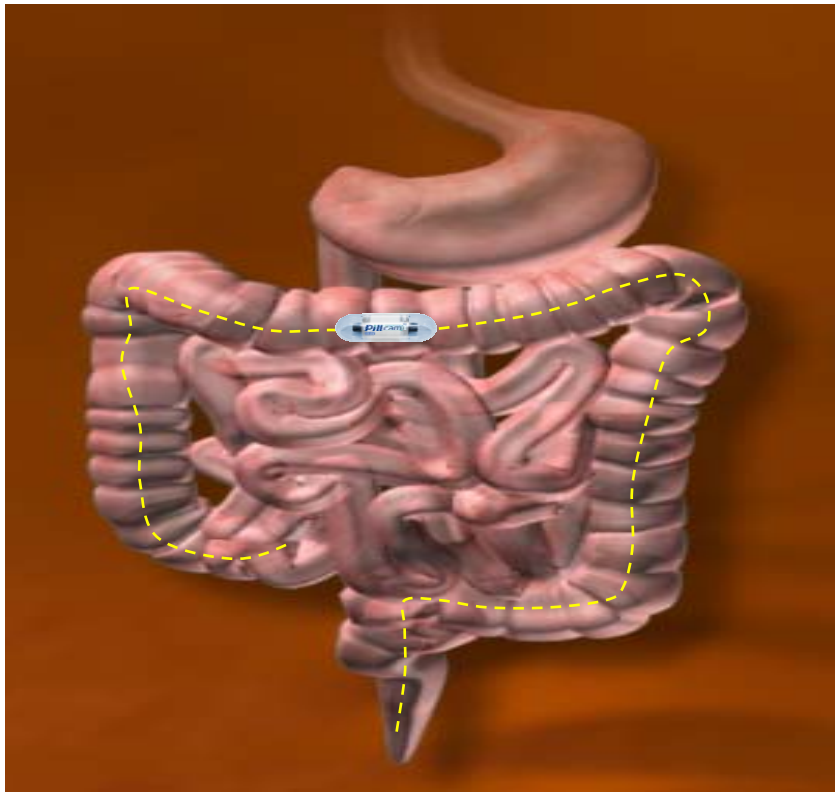
A non-invasive tool to visualize the entire colon

Diseases of the COLON: Colitis, Polyps, Diverticular Disease, Cancer

PillCam Colon – Marketed in EU and some of Pac Rim (FDA tbd)

> 10-hour operational time

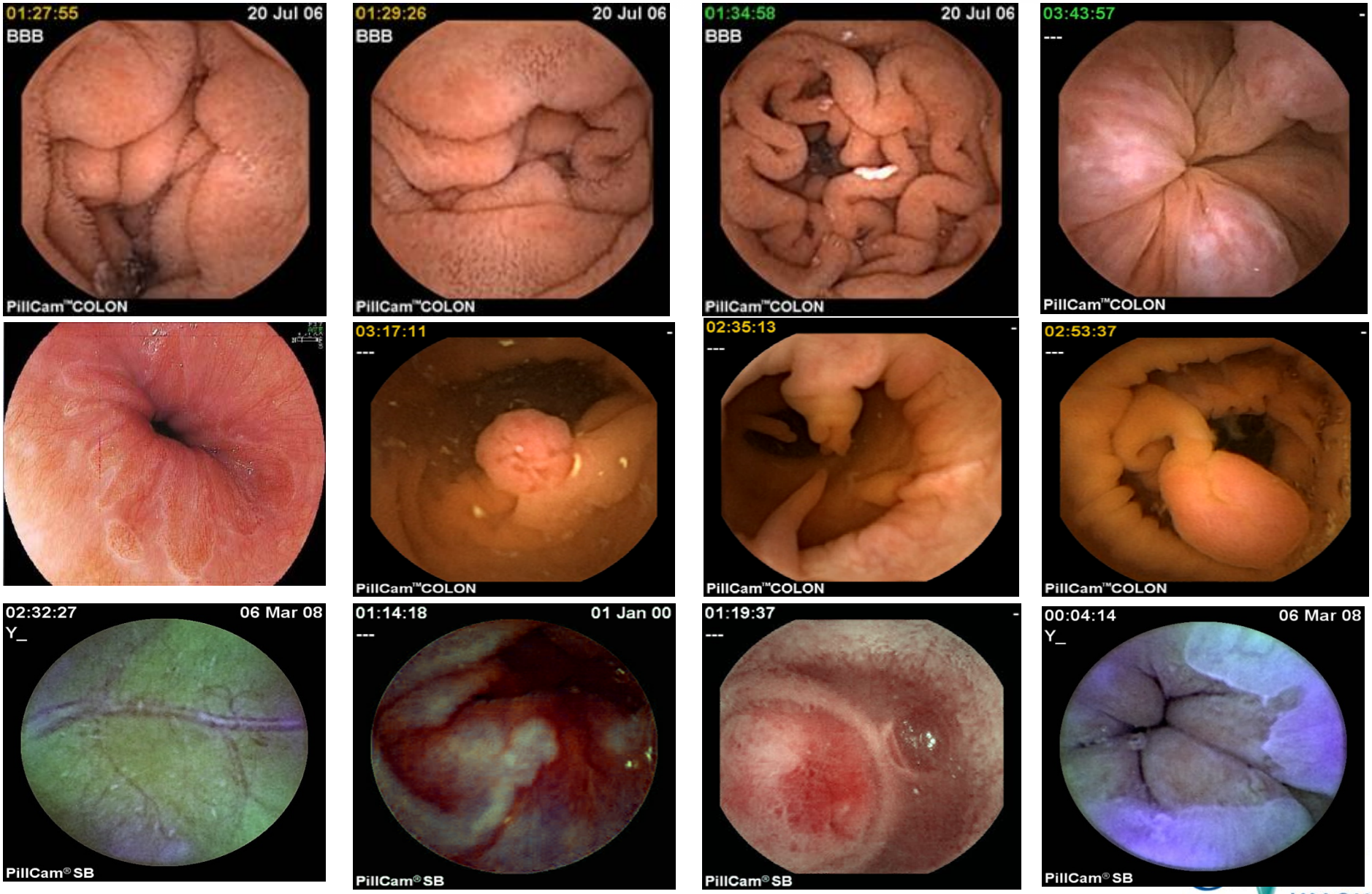
Captures > 140,000 images



PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

GIVEN IMAGING

Capsule Images of Intestinal Tract



PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

IMAGING

The Future

Helping patients and saving lives

MEMS can enable:

-Propulsion

-Therapy

-New applications

GIVEN IMAGING

PillCam® Colon is not cleared for marketing or available for commercial distribution in the USA

ASIMPS for BioMed

Post-process from Carnegie-Mellon University

Base: CMOS, BiCMOS, ST (Jazz)

Example: bone implantable stress sensor

Usually: imaging of bone quality due to trauma or disease

Problem: bone strength vs. image intensity

Solution: measure bone strength in-situ

How: piezoresistive sensor “pixels”, detect stress across interfacial area between bone and chip

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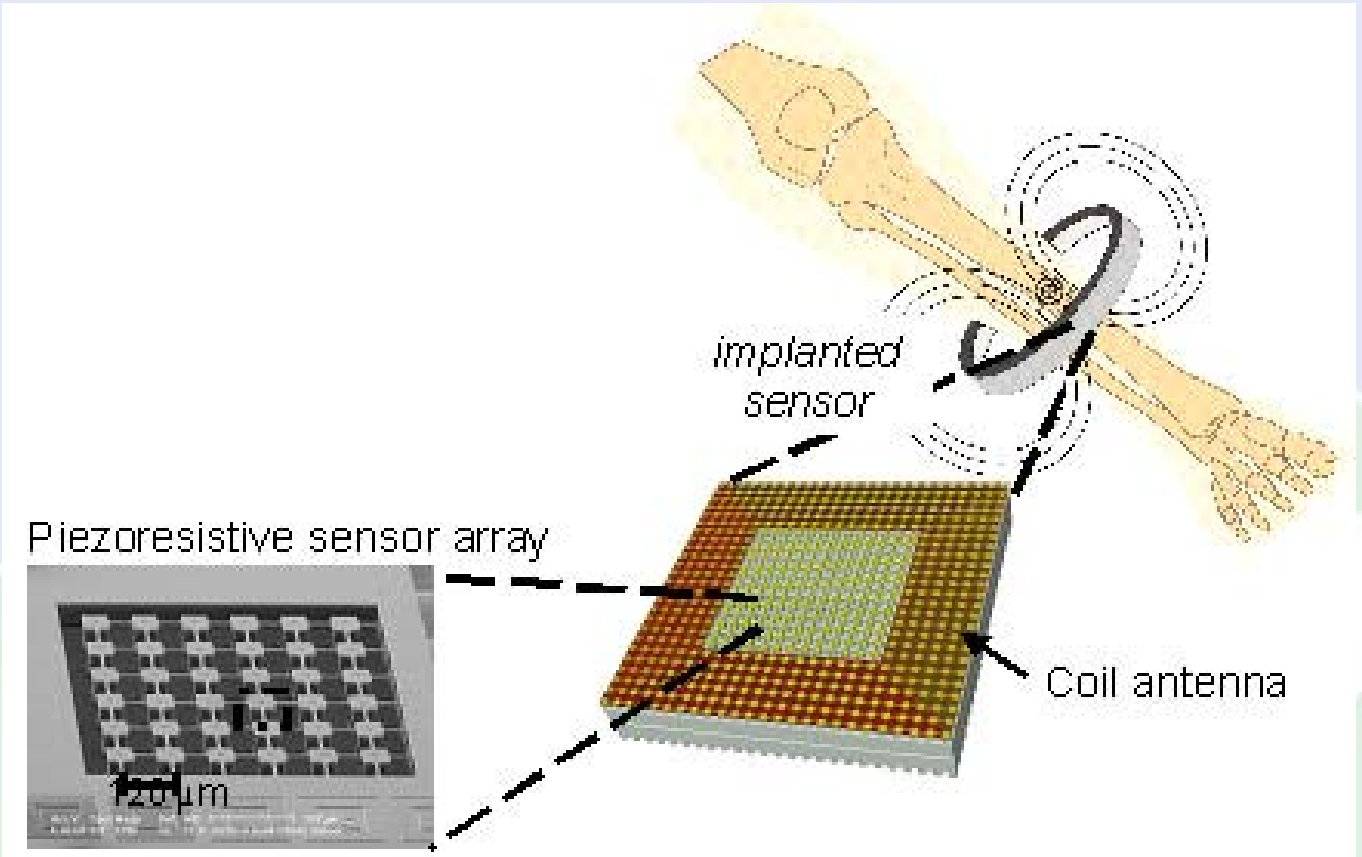

Bone Implantable Stress Sensor

[courtesy from Carnegie-Mellon University]

Goal: timely information for treatment management options, including drugs, fixation, surgical intervention, etc.

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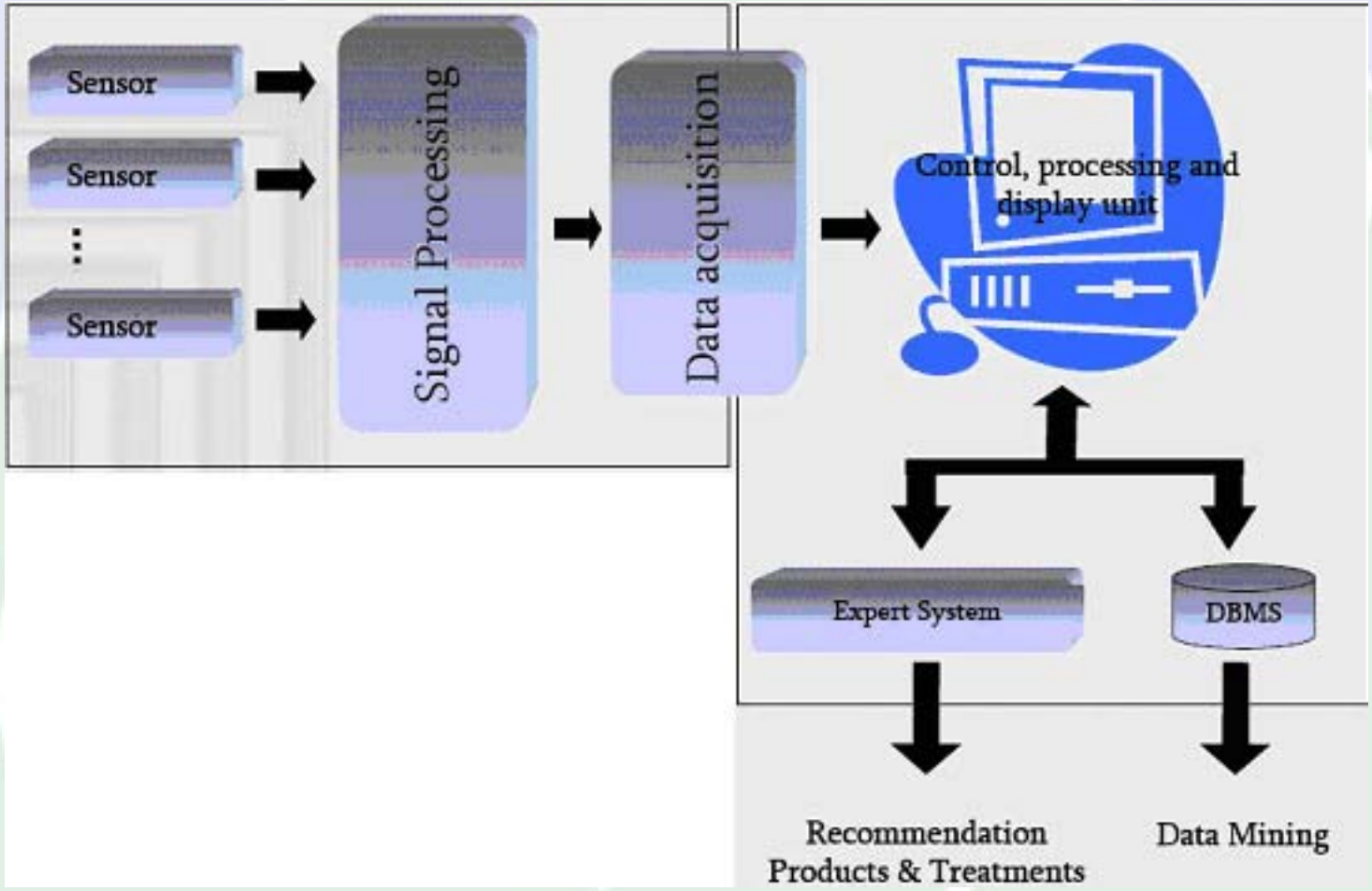
System view: BioMed science and beauty

System: sensor, ASICs, data acquisition, expert systems, ….

Example: skin care technology from IntuiSkin (MEMSCAP)



IntuiSkin general concept

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2 probes:

- Visio probe

  wrinkles, sebum, hairiness, dark spots, clogged pores / bacterial infection

- Physio probe

  hydration, trans-epidermal water loss, temperature

The probes and examples of measured parameters

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Medical market

Practicians needs in cure and detection, and specific treatments (peeling, injection, fillers,….)

Clinicians in pre and post surgical support, by skin specialists, dermatologists, dermato-cosmeticians, plastic surgeons.

Beauty market

Measuring the 7 main dysfunctions of the skin: hydration and UV damage, fine lines, wrinkles and elasticity, redness, bacterial infection, sebum, dark spots

➔ recommendation of the best treatments by aestheticians

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Other example: Sensicards

Goal: optimize the use of cosmetic products

Systems: sensors, micro-electronics, data displays, batteries, communications,…
credit card size

UV-Sensicard: skin protection against the sun

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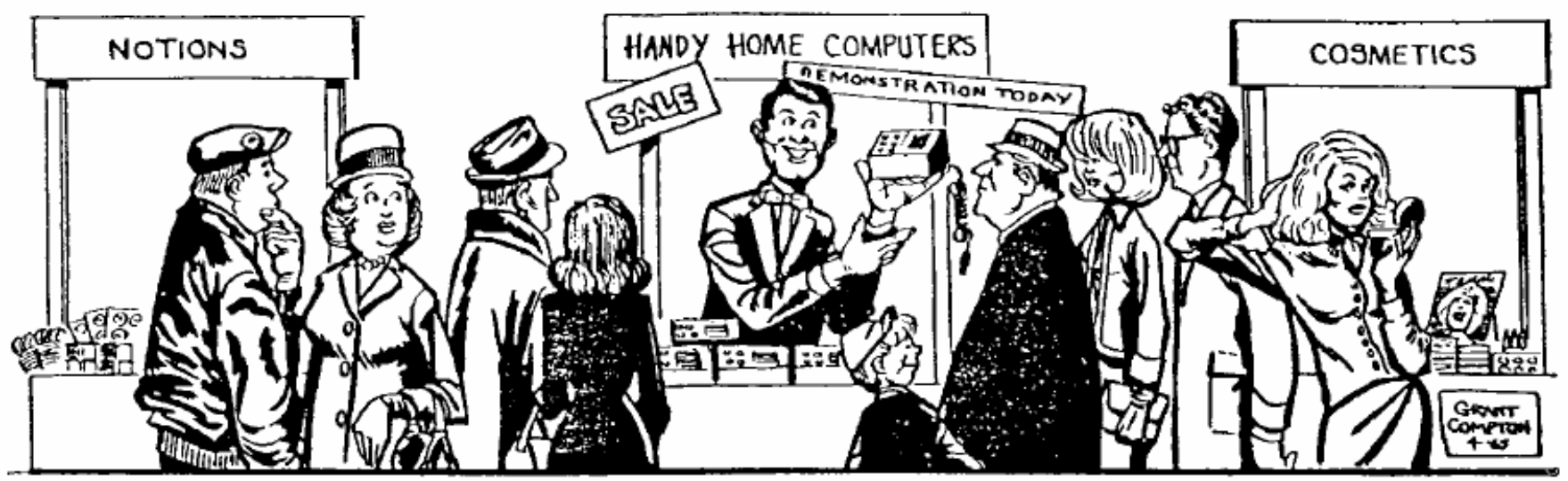

From G.E. MOORE,
Cramming more components onto integrated circuits,
Electronics, Volume 38, Number 8, April 19, 1965

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Conclusions on BioMed

Labs mixing electronics and biomed: a few examples

- Polystim, Montreal
- CEBE, Tallinn
- CiBER, Vancouver
- INSA, Lyon
- .....

Many kinds of BioMed applications: neurosciences, surgery aids, endoscopy, skin treatment, etc.

Many others will come, from emerging markets, e.g. "cosmetofood" or "nutricosmetics"

- DANONE: yoghurts "nourishing the skin"
- L'OREAL: food "fighting skin aging"
- efficiency can be measured.
- (but markets possibly not yet ready....)

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What is important for the BioMed community?

EE, CS, early 80s: infrastructures for ICs manufacturing
decoupling process – design ➔ VLSI revolution

BioMed: take advantage of similar infrastructures,
Education, research
low cost
not any kind of applications
standard processes: many applications, no process involvement needed
interface decoupling electronics-biomed knowledge

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Address important application areas: e.g. energy management

- **Health, Environment, Security,...**
- **Energy**
  - **+ low-power ICs (mobile devices, data centers,....)**
    examples [SAMSUNG]
    - **replace all worldwide servers with DDR3 (double data rate three synchronous DRAM): 38% power**
      ➔save 82 Trillion Wh per year, 11 nuclear plants
    - **replace 4B mobile CPU from 65G to 45LP**
      ➔save 4.9 Trillion Wh per year
  - **+ how SCs can address energy issues?**

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Introduction

Energy / climate issues very important

Electronics in general, SOC, SIP, much needed

How SC industry can address energy issues: generation, conversion, use, storage?

[Sources: IEA "Energy efficiency policy recommendations", 2008,

R.P. de VRIES/NXP keynote at ISSCC 2009 (RPdV),

Ch. BELADY/Microsoft keynote at ICCD 2008, and SEMITHERM 2010

A. SHAKOURI/UC Santa Cruz]

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Some facts

Worldwide oil consumption 2008

USA	19.4	Million barrels/day
China	8.3	
Japan	4.8	
India	2.9	
Russia	2.8	
Germany	2.5	
Brazil	2.4	
South Korea	2.3	
Canada	2.3	
Saudi Arabia	2.2	
France	1.9	
.....		
Worldwide	84	

Minus.... 0.6% over 2007....

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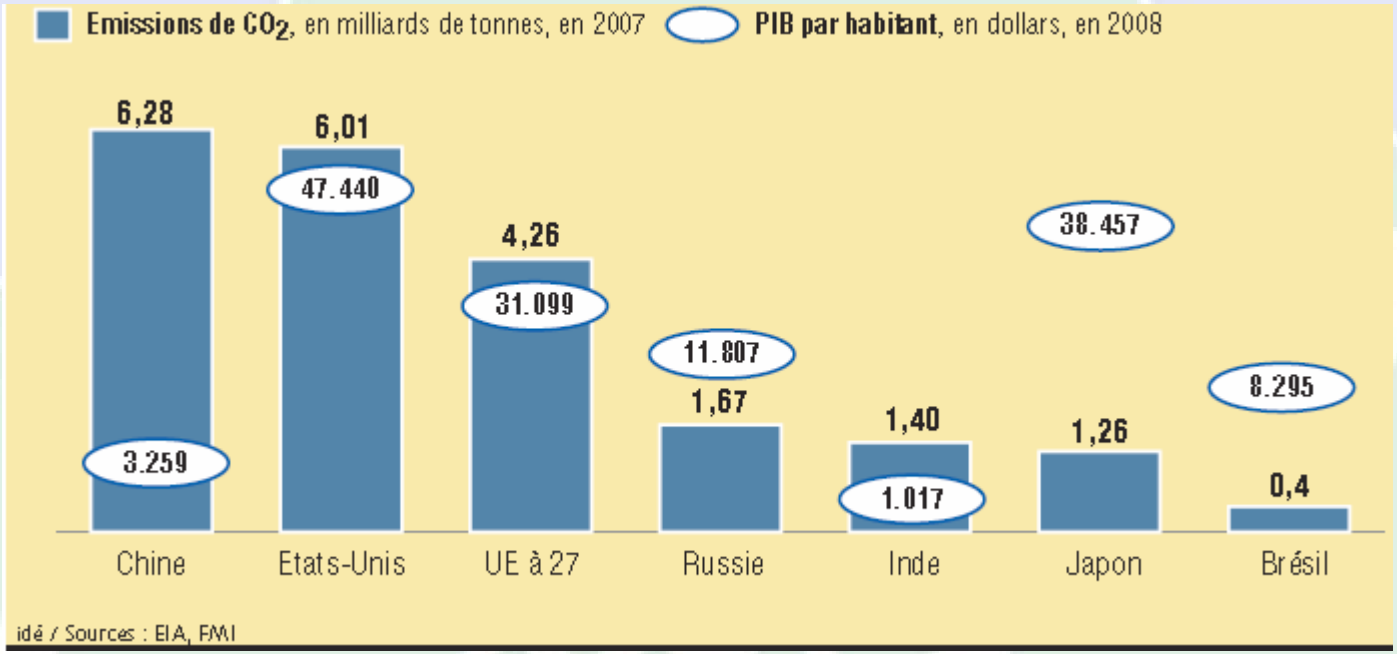
CO_2 vs GNP



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In France, over the XXth century:

- population: x 1.5
- GNP: x 10
- electric power consumption: x 1,500

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Recommendations

- Lord Nicholas STERN

  today: 435 ppm CO_2

  +2.5 ppm/year

  2100: ➔ 750 ppm

  +5°C....

  beyond +2°C: unpredictable climate consequences

➔
- 20 $GtCO_2$ instead of 40 $GtCO_2$ in 2050
- absolute targets instead of percentages, that are based on 1990 emissions
- growth targets:

  if +2.5% for US, Europe, Japan

  +7% for China, India

  +5% Brazil, Indonesia

  ➔all divide by 4 the CO_2 emitted by 1% of growth

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- **IEA**

  IEA to G8 policy recommendations: save 20% of total energy by 2030.

  ➔ **reduce global CO_2 emissions by 20% per year by 2030 (≃ 8 $GtCO_2$)**

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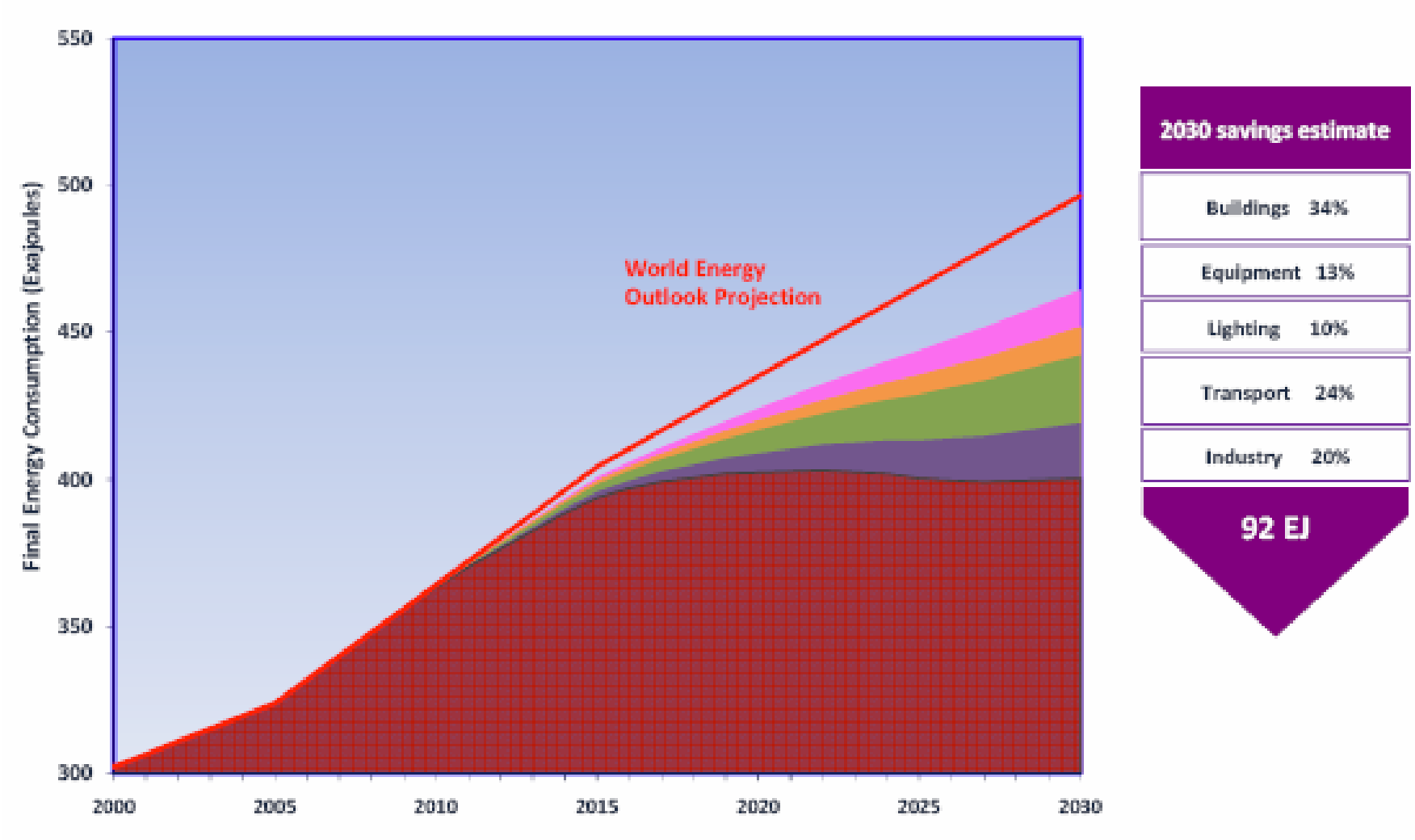

IEA Energy Efficiency Policy Recommendations, 2006-2008.
Impact on World Final Energy Consumption

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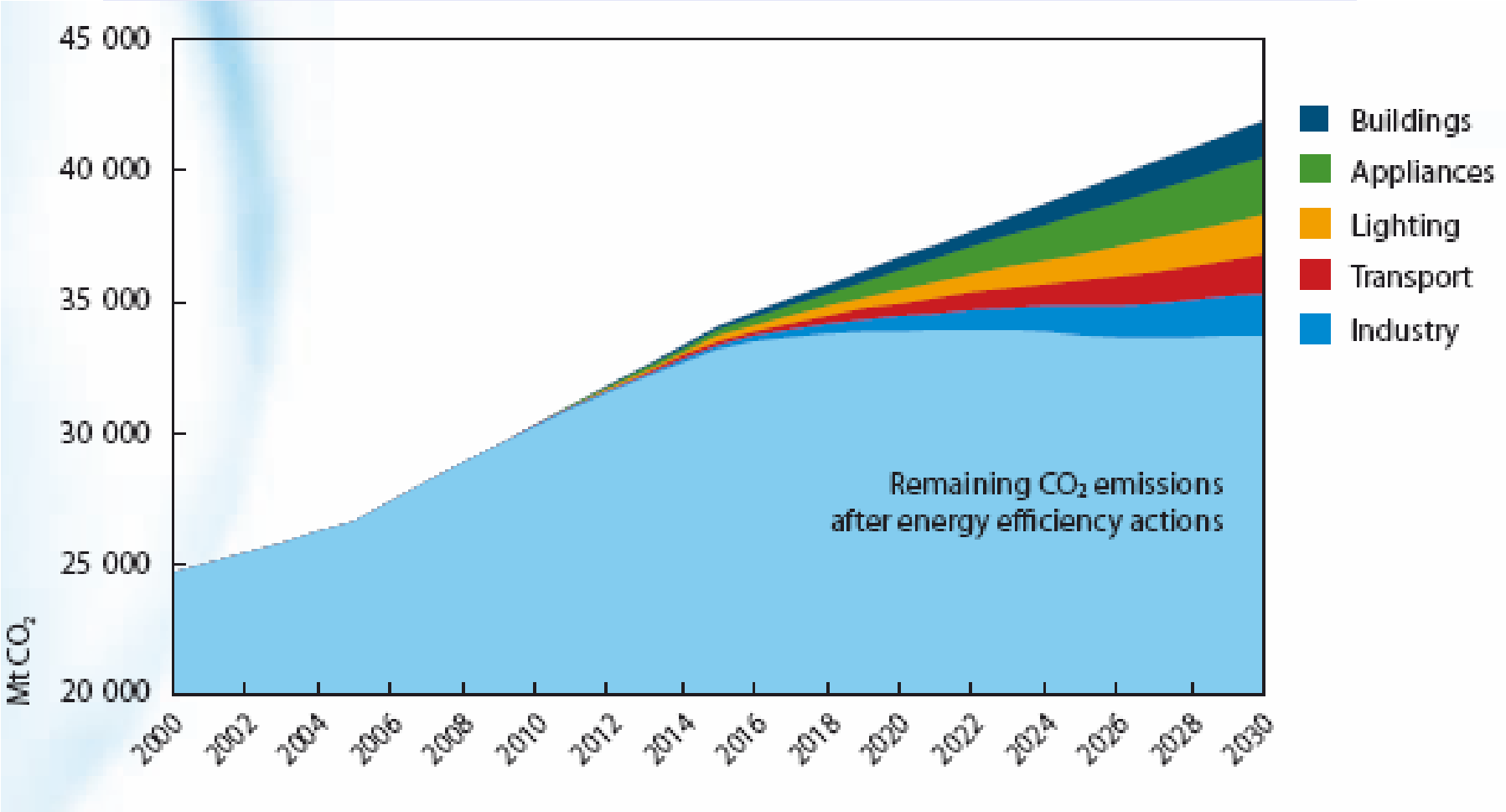

IEA CO_2 savings potential from energy efficiency recommendations

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Buildings	:	1.4 $GtCO_2$
Equipment	:	2.2 $GtCO_2$
Lighting	:	1.2 $GtCO_2$
Transport	:	1.4 $GtCO_2$
Industry	:	1.6 $GtCO_2$

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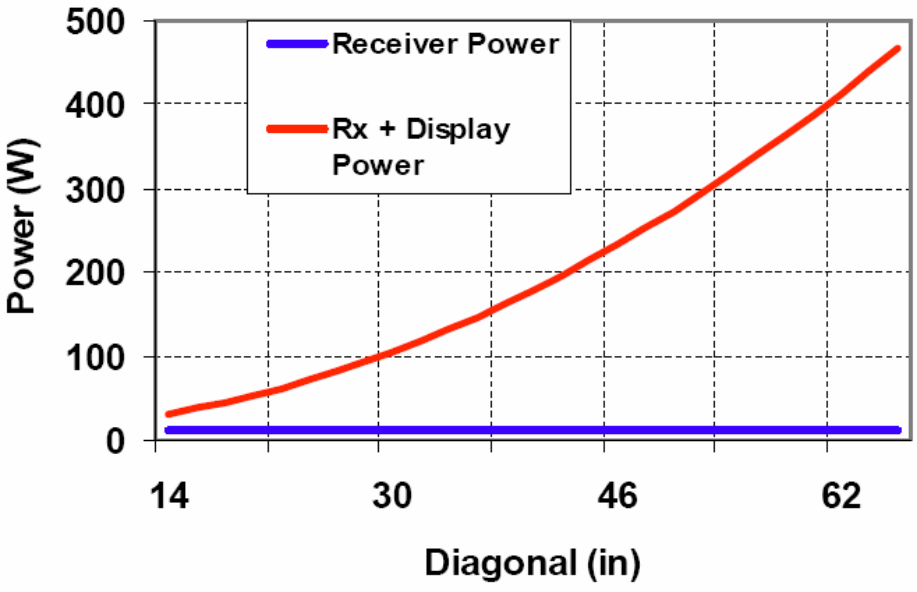
Electronic equipment

standly mode in home appliances:
5% to 10% of total home power consumption
EU regulation 2008:
- ≤ 2 W 2010
- ≤ 1 W 2013
(except internet boxes (telephone))
➔50 TWh presently in EU, down 75% in 2020
operational mode: TV displays consume 120 W in 32", 460 W in 66"....
3 M homes move to home cinema: 1 power plant.....



TV power vs. screen size [RPdV]

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actually:

- power consumption frequently not displayed in shops...
- picked up by chance: 470 W for 46'' 635 W for 58" (major brand....), some even do not post the power...
- plasma consumes much more than LCD, while plasma is recommended for very large screens...
- old cathodic display: around 100 W....
- objective in 2020: 1 W per inch (40 W for 40'')

hope:

- MEMS-based devices to replace LCD, plasma, OLED? TMOS (Time-Multiplexed Optical Shutter), DMS (Digital Micro Shutter), iMoD (interferometric MoDulator)? For small sizes only probably

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high-tech equipment: (TV, computers, set-top boxes, etc.):

2% of worldwide CO_2 (but savings on the 98% because of new life styles, e.g. virtual meetings, e-commerce, etc.)

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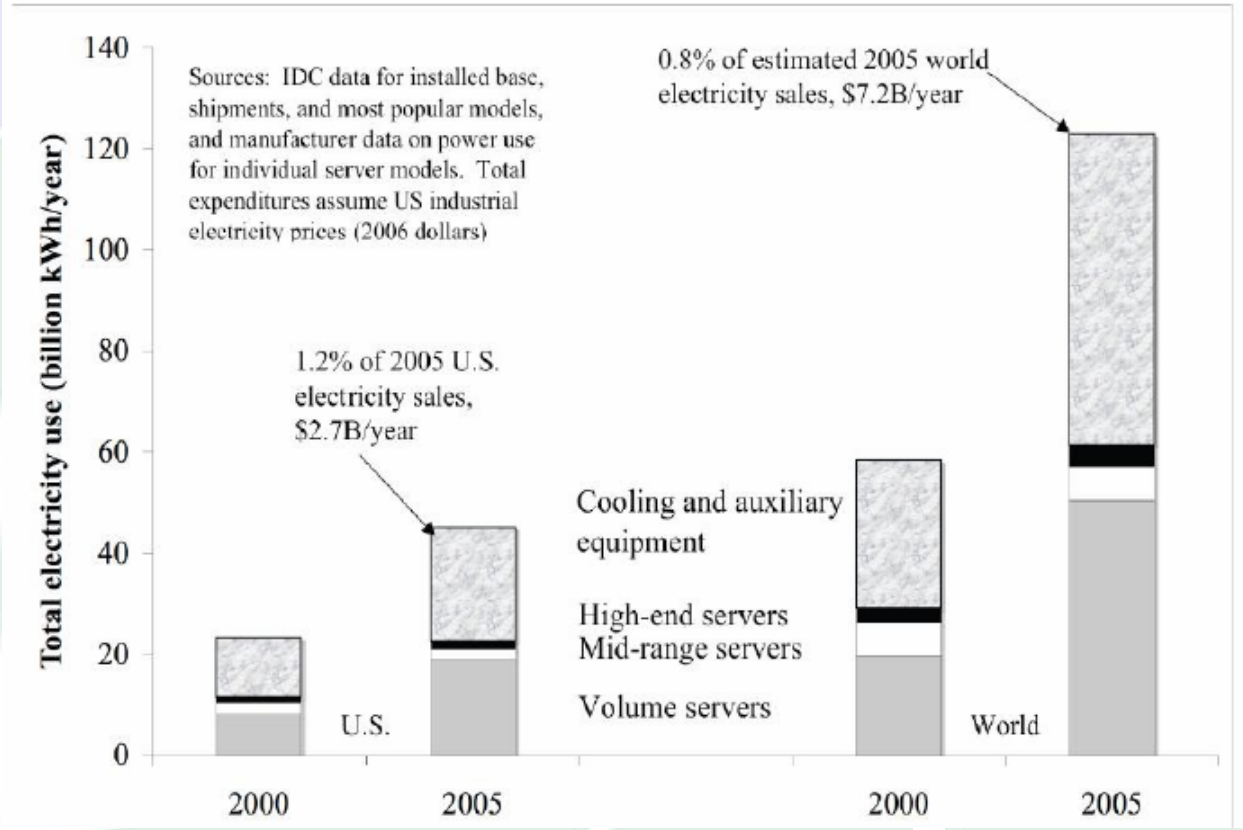
data centers: 1.2% of total consumption in USA in 200

Figure ES-1: Total electricity use for servers in the U.S. and the world in 2000 and 2005, including the associated cooling and auxiliary equipment



expected to be 2.5% of total power consumption in USA (30 power plants) in 2010, 10% in 2020
at this time: CO_2 from US DCs = CO_2 from US planes

in Europe: 40 B kWh, 80 B in 2012

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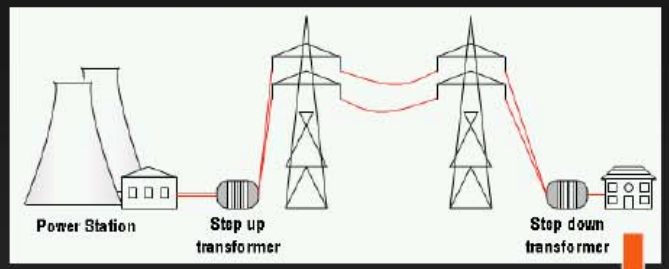
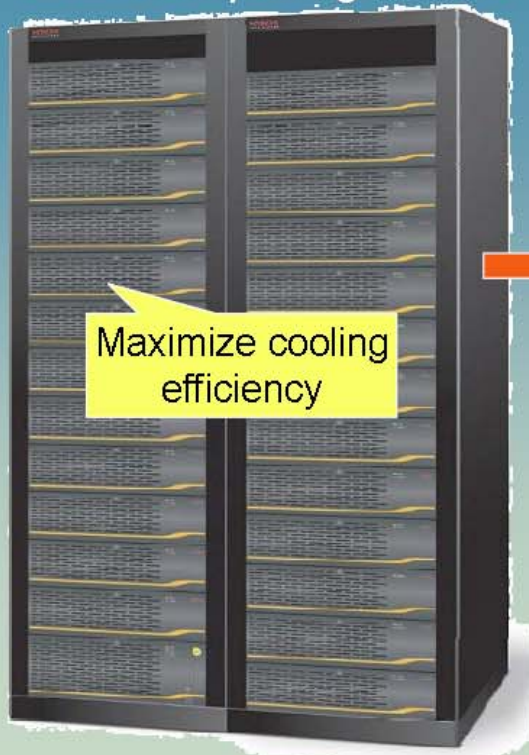
Where Data Center Power is Consumed

Power Service: 3%

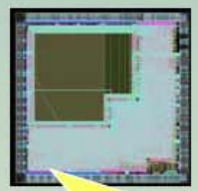


Computing: 52%



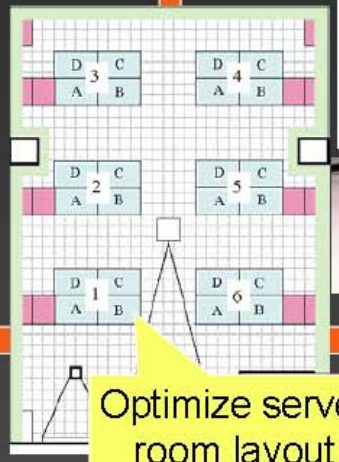
Low power Board design

Maximize cooling efficiency



Low power chip design

Minimize cooling needs



Optimize power distribution

"Green" cooling

HVAC Power

Cooling: 38%

Optimize server room layout

Server Power

UPS/PD 6%

Ted VUCUREVICH

cadence

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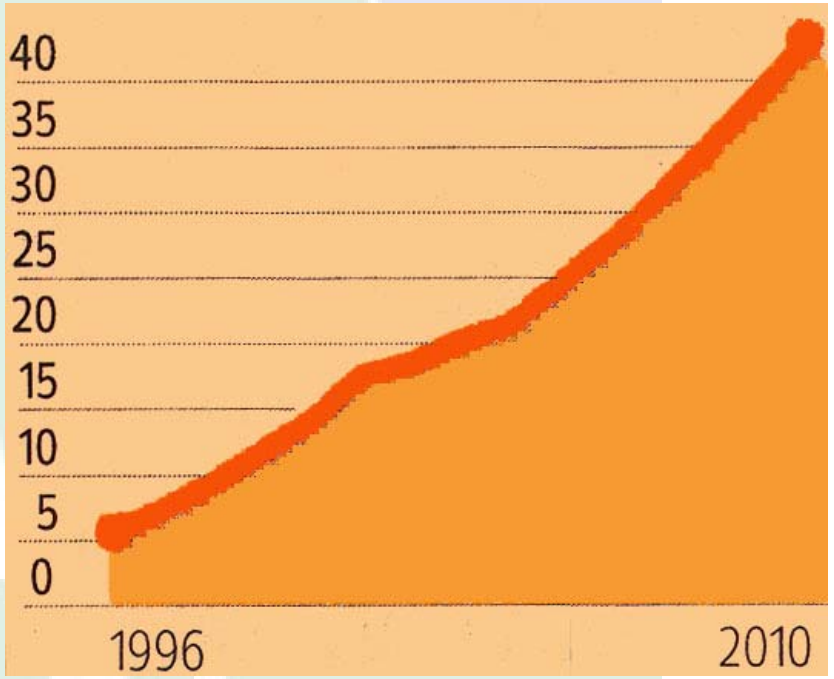
Why so much power needed?

Demand:

Total number of servers worldwide (millions)



Google™: 1M?

Second Life: 4,000 in 2007

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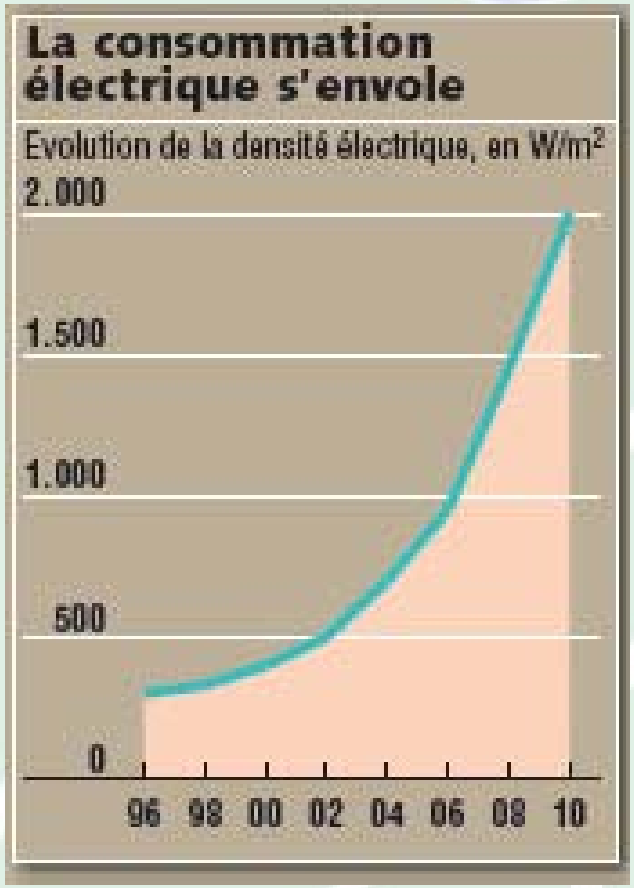
Cooling: W/m² in data centers



Les Echos, 12 April 2010

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data center: 100,000 servers, 11 times the size of a football field, every W in the die translates into $3 to $4 in support cost (100,000 servers ➔ $300 K to $400 K for 1 W...)

Servers come in containers (≃ 2,000 servers), ≃ 100 containers in a data center, 3 pipes: power, water, data

Generation 3 Microsoft (Chicago DC): 17 times the size of a football field

Cost of a DC: 500 M$

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What are Containers?

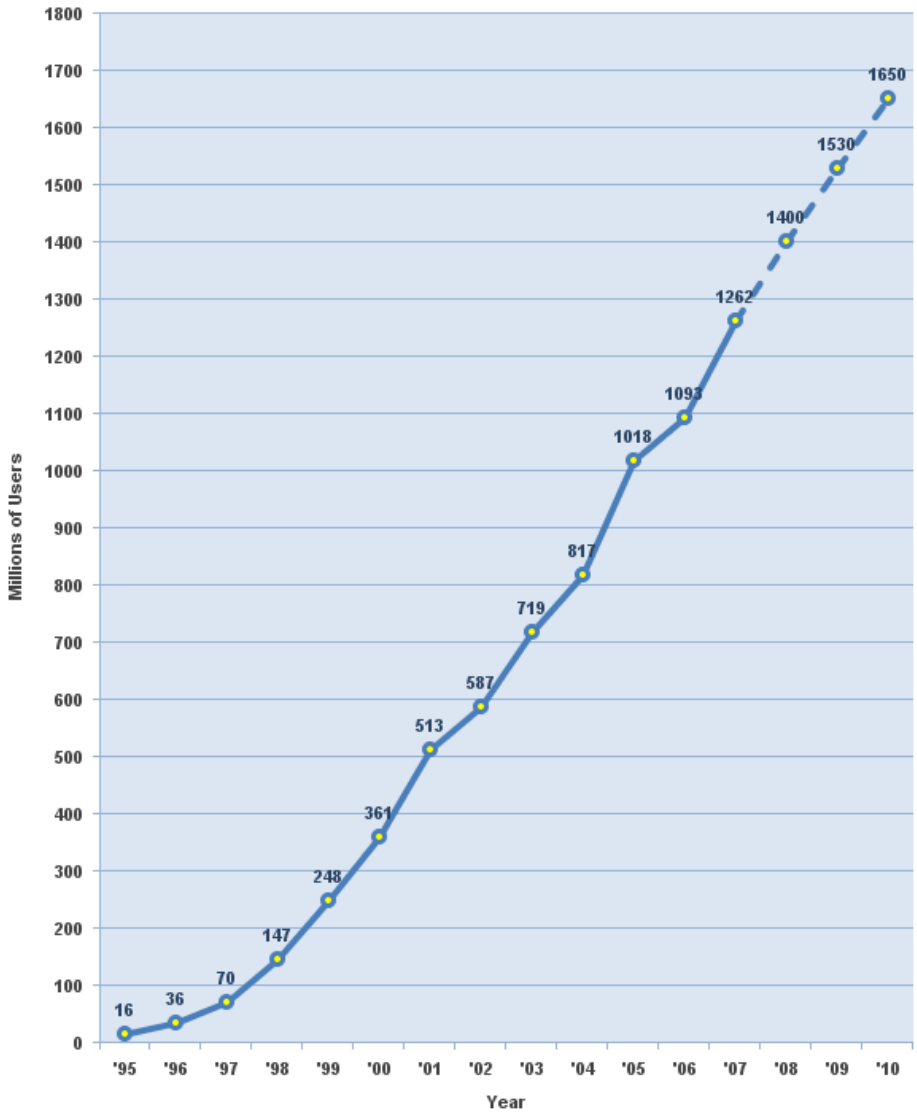
- Use either standard ISO shipping container or similar size
  - 40',20',10' x 8 x 8'6"
- Many New Applications emerging…

CBlox Computing

perf/W is going up (16X in 10 years), but demand goes up....

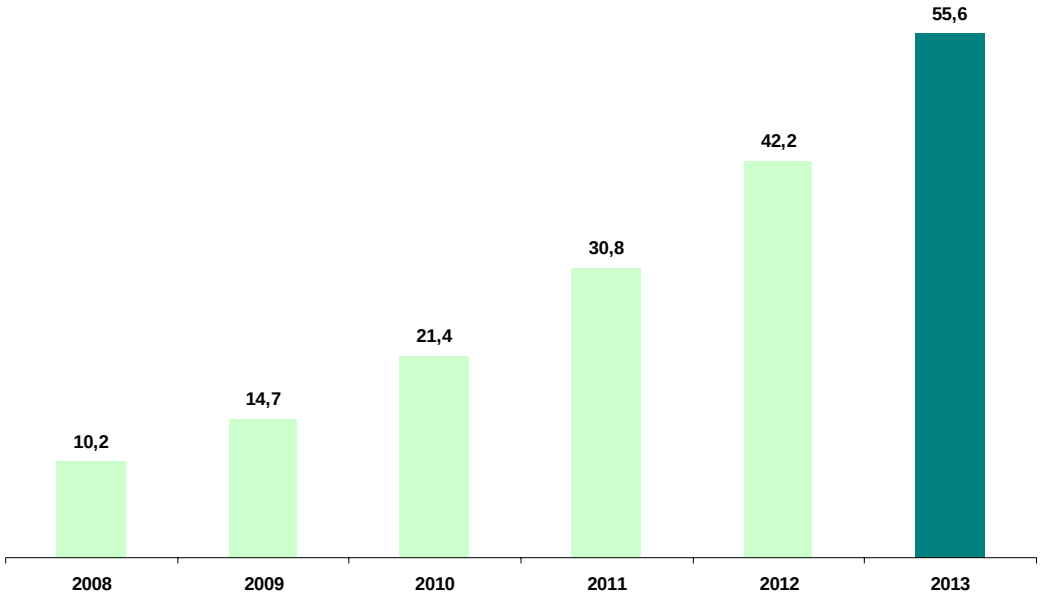
Internet Users in the world

Growth 1995-2010



Source: www.internetworldstats.com - January, 2008

Internet traffic in the world



facebook : 400 millions members....

YouTube alone uses as much bandwidth today as the entire Internet did in 2000

200 Tbytes of traffic daily = 10 x entire US Library of Congress holdings

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cloud computing (rental of hardware resources (plus possibly software)): will it help?

possibly: less (too) big server farms

Automotive

- 60% of world oil consumed in transport
- road vehicles: 80% of total transport energy consumption
- 35% decrease in oil consumption per car over the last 30 years

  50% more reduction by 2030

  and 50% more for light-duty vehicles
- How?: electronic control!

  $ value of electronics: +3% per annum, to increase rapidly

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- Electric cars will help on oil consumption on the roads, but they need an electrical source... (if all cars in France: +25% to +50% electrical consumption....)
  total process may be not very efficient
  $ value of batteries: ~ 30%, $ value of electronics... 70%
  power stations to recharge... ???

- Various types of hybrid cars can save oil consumption with stop-start, use of electrical power for acceleration, regenerative braking, electrical transmission,... Many DC-DC converters needed, DC-AC needed, etc.

- Conventional cars: replacement of wiring by electrical networks save weight, hence consumption, replacement of the lighting by LEDs,....

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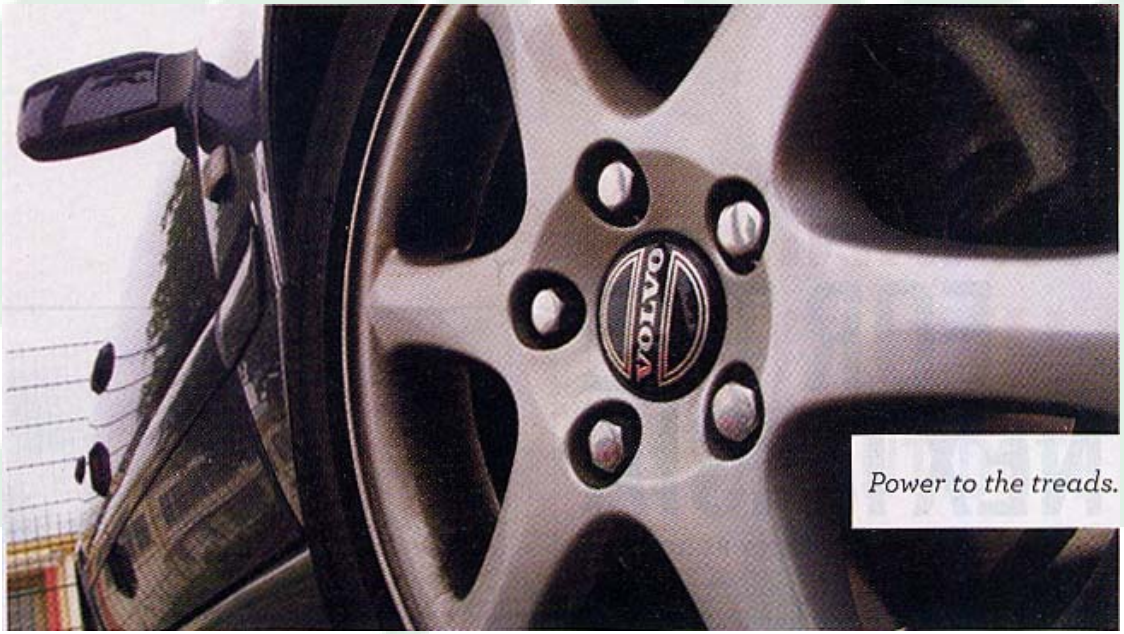
- **A promising technology for electric (EV) / hybrid (HEV) cars: wheel motors?**

  electric cars still destroy 60% of energy because of mechanical parts.

  wheel motors use electromagnets and pulses of electricity

  200 cars, buses, trucks already in test

  MICHELIN: plus suspension and brake



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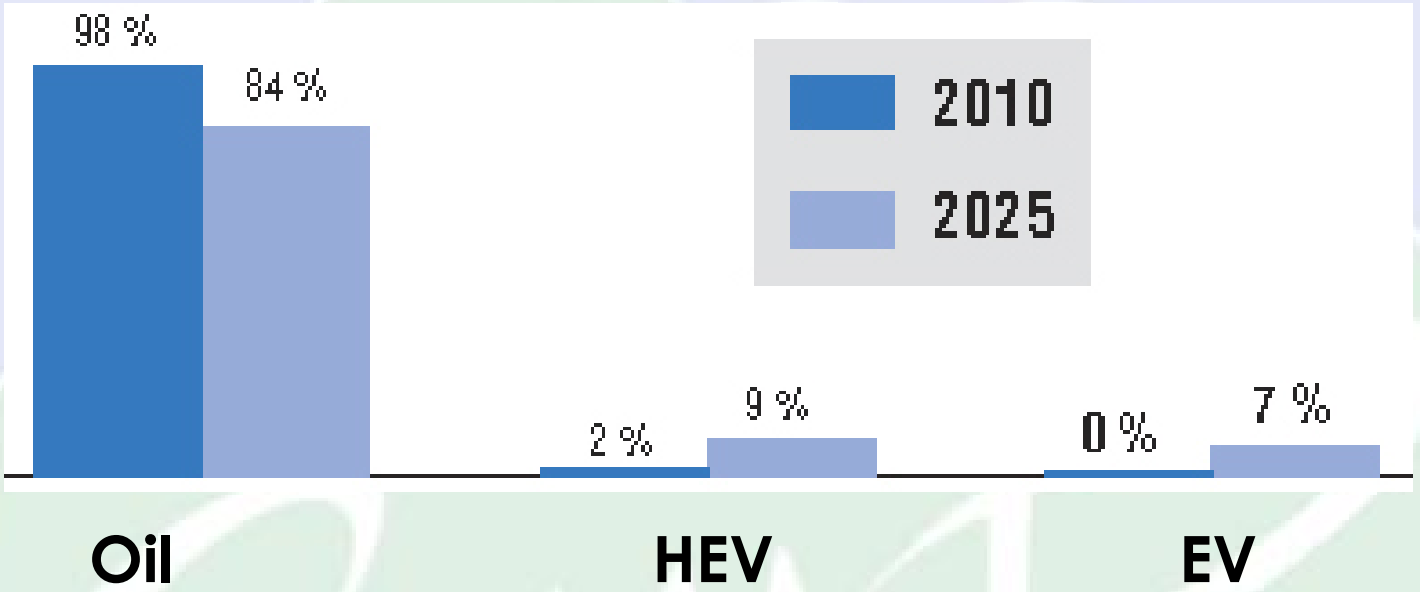
Market



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Lighting

- 20% of total electricity produced... replacement of incandescent lamps by fluorescent or tube lights can save 80%. In EU:

  + 100W : 1 Sept. 09

  + 75W : 1 Sept. 10

  + 60W : 1 Sept. 11

  + all others : 1 Sept. 12

- Move from discrete power components to integrated solutions for the drive electronics

- In addition: occupancy detection....

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Buildings

- Heating, ventilation, air-conditioning, lighting,....
- Metering allows the shaving of peaks (hence of the total capacity), by powering off some devices. Many sensors required.
- Metering allows power providers to get information (but traffic on internet....)

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PV (the earth receives nearly 100K times more energy than required worldwide)

- Several PV technologies
  - crystalline (high conversion efficiency, high cost)
  - thin film (lower, lower)
- Very important: power output maximized when cell operated at an optimum voltage, dependent on temperature and irradiance...
- Installed capacity: +20% to +40% per annum, to increase with the increasing competitiveness of PV (price of PV generation vs. grid price)

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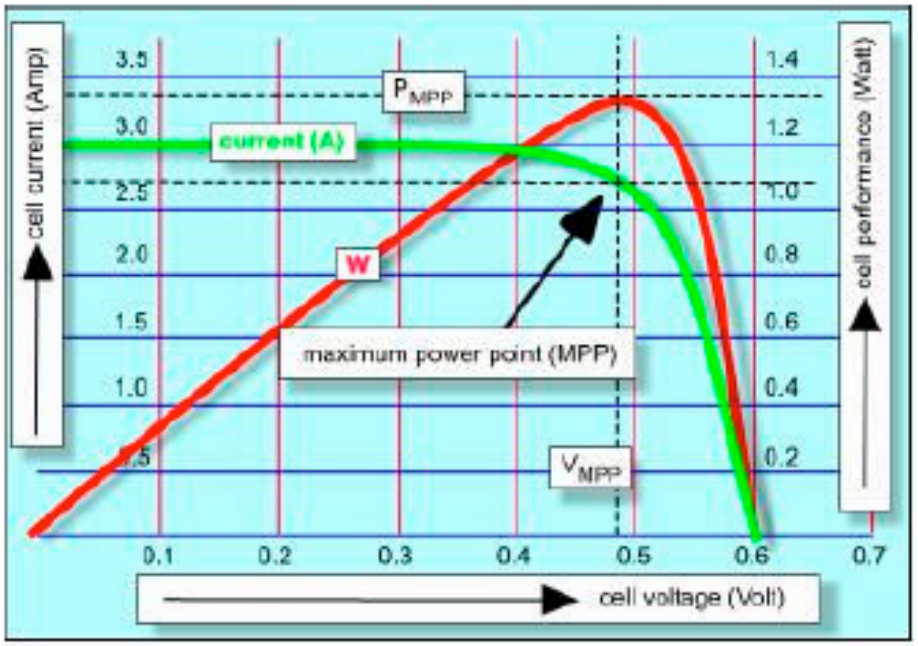
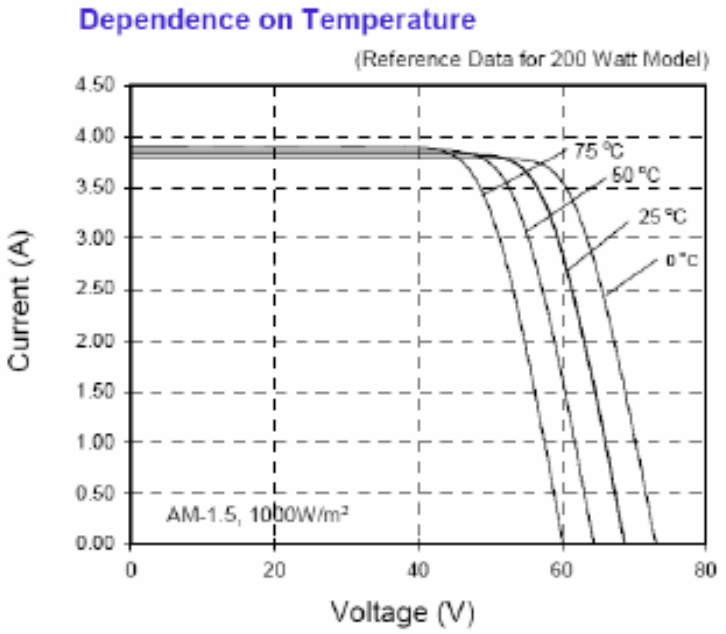
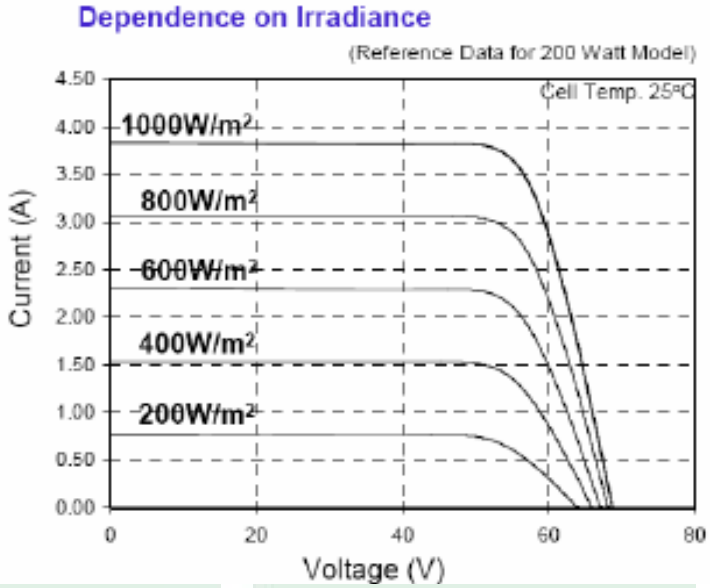


Optimum Load for Single Photovoltaic Cell (National Semiconductor)





Temperature and Irradiance Dependence of a PV Module (National Semiconductor)

➔ electronic control! (local)

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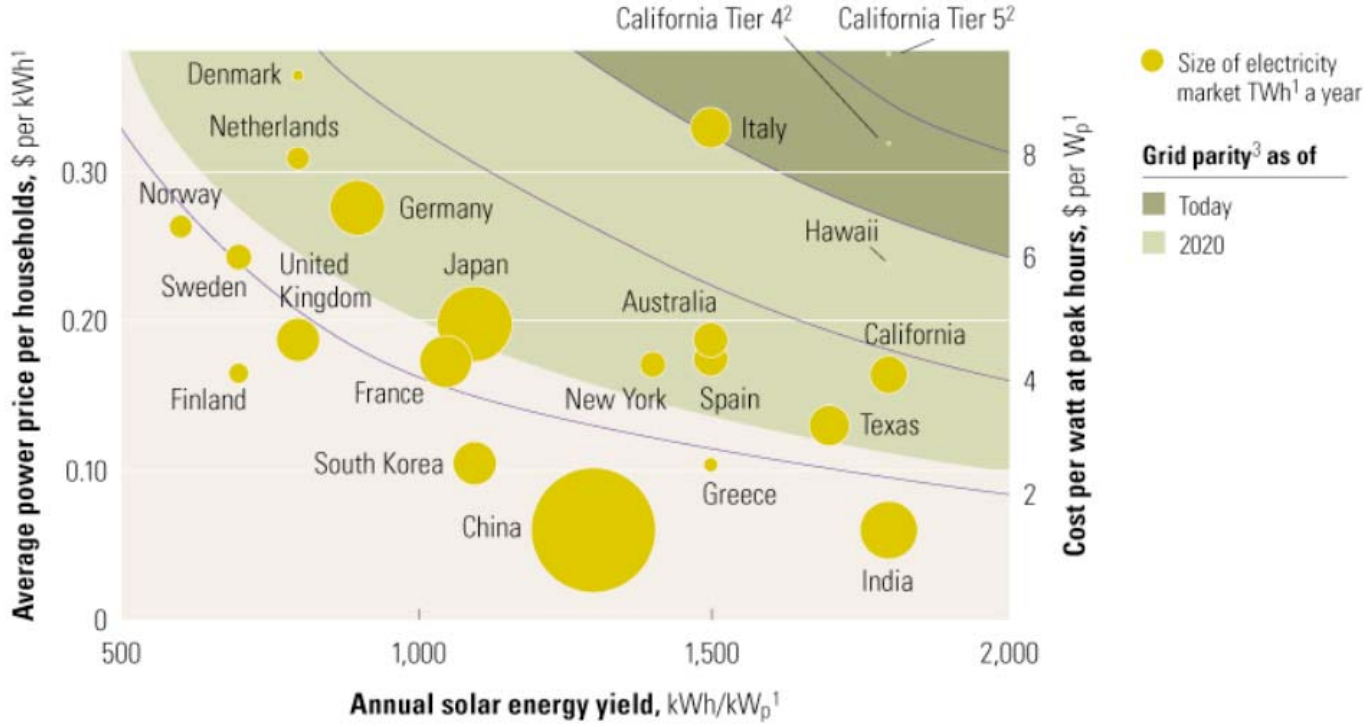
Moving competitiveness of PV (with price of PV decreasing)



¹kWh = kilowatt hour; kW_P = kilowatt peak; TWh = terawatt hour; W_P = watt peak; the annual solar yield is the amount of electricity generated by a south-facing 1 kW peak-rated module in 1 year, or the equivalent number of hours that the module operates at peak rating.
²Tier 4 and 5 are names of regulated forms of electricity generation and usage.
³Unsubsidized cost to end users of solar energy equals cost of conventional electricity.

Source: CIA country files; European Photovoltaic Policy Group; Eurostat; Pacific Gas & Electric (PG&E); Public Policy Institute of New York State; McKinsey Global Institute analysis

to compare to ….

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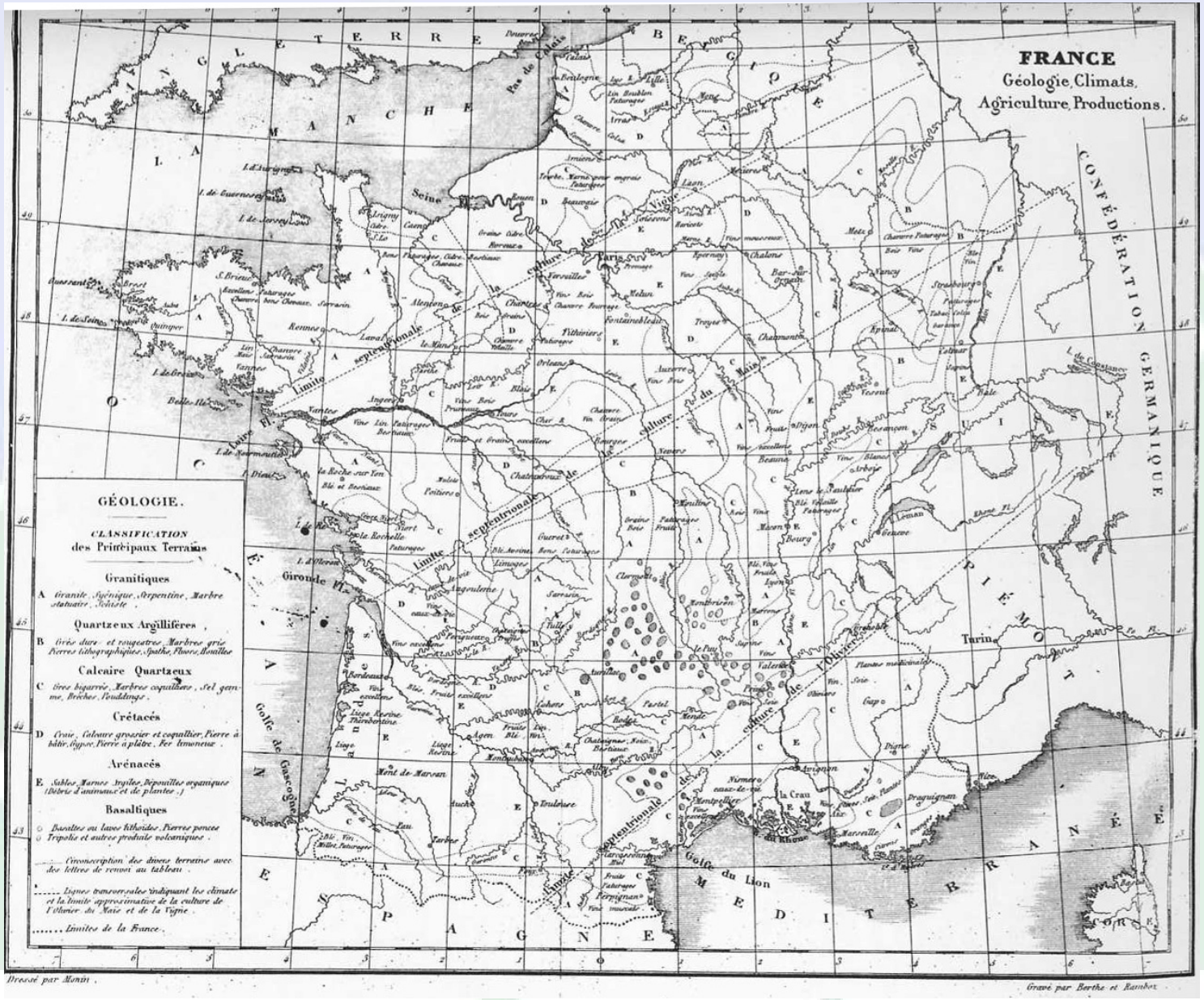
Moving limits of wine culture with global warming



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Concrete examples: zero energy building

ZEB building in Dijon, France

1,600 sensors, 550 sqm PV

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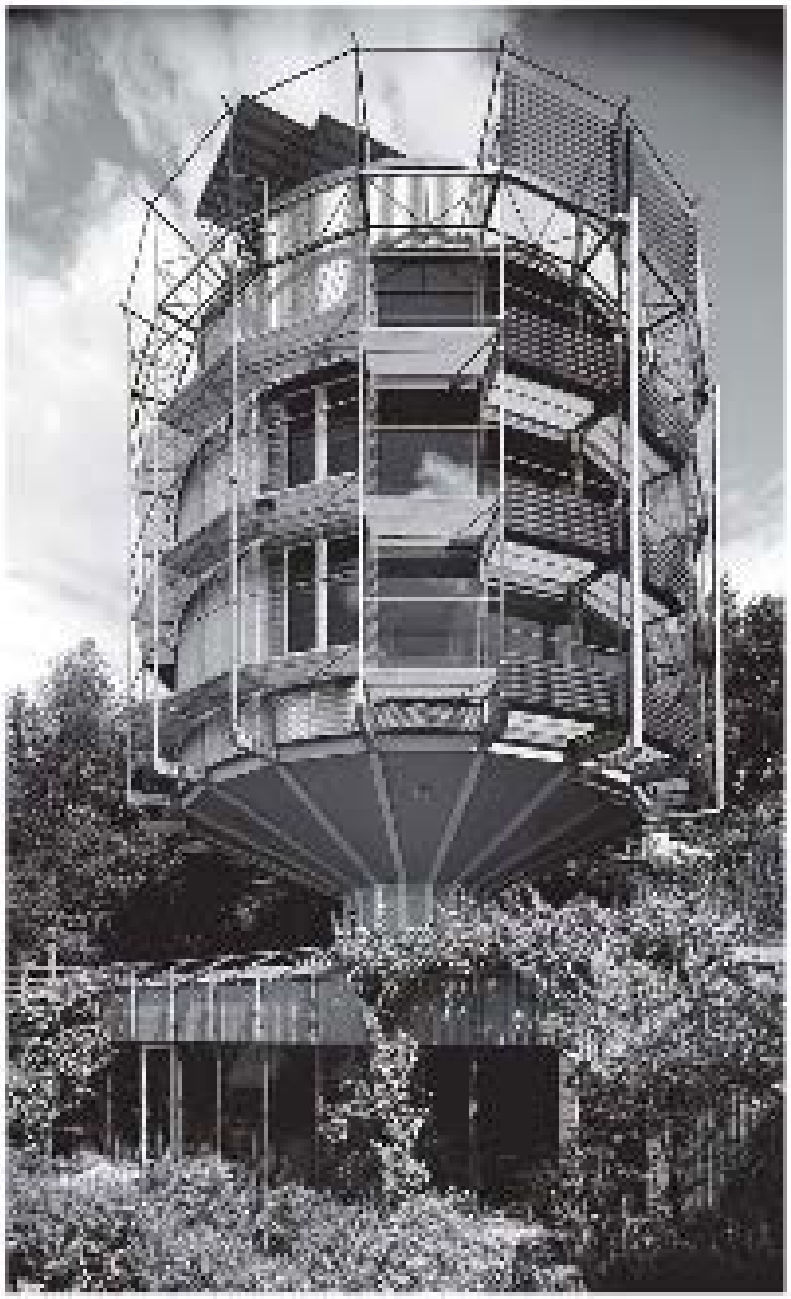
Rotating solar building



Freiburg, Germany

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Turning Torso Tower in Malmö: part of the city where the energy was supposed to be produced locally, from renewable sources.

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How about CO_2 for electric cars...?

Zero emission....?

NO!

CO_2 emissions moved to plants, to generate the energy for the batteries....

Some examples (small car, averages, next slide)

Also: recycling the batteries (2 years lifetime)

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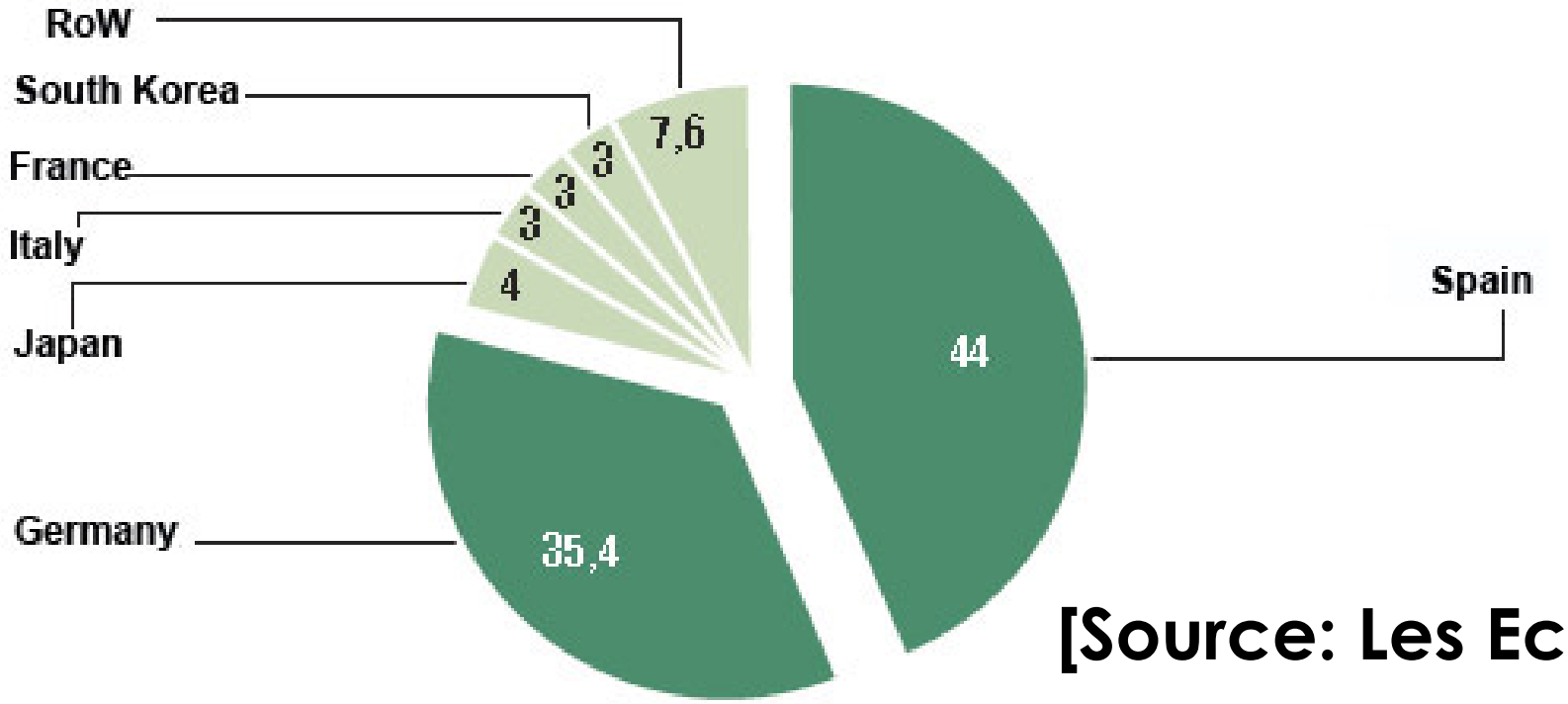
PV market

- 2008 PV market in various countries, in %



[Source: Les Echos]

- Investments for PV manufacturing > investments for SC manufacturing in 2010
- $ 800 M in 2008 SC for alternative energy systems (solar, wind, fuel cells), expected to rise to $ 2 B in 2012

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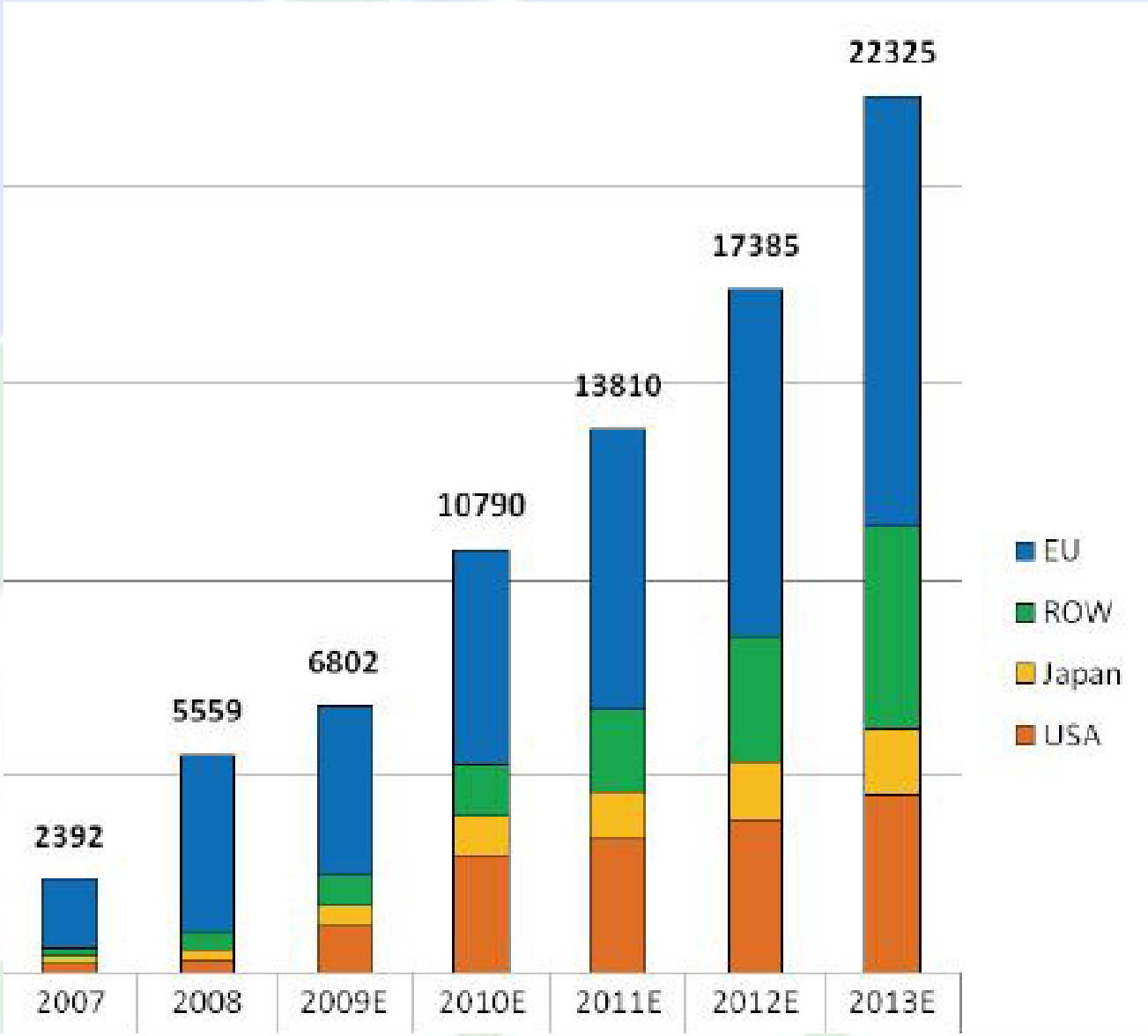
PV worldwide market: 6802 MW peak in 2009



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CO_2 savings: an excuse for disputable projects

- 60 t trucks; “2 trucks instead of 3”....

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- **PV plant in a park, 200,000 sqm in total, by deforestation, in Lans en Vercors....**

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Conclusions on SC/energy

Technology

- Focus on low overall power consumption thanks to ICs in addition to low-power ICs
- More technology developments away from Moore law towards better control and management of energy, improved power generation and storage
- Energy harvesting
- Central role of sensors, PV, electronic control

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Further longer term research

- Artificial photosynthesis (replace chlorophyll by molecules that capture photons, then transfer the electrons)

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Conclusions

More “more than Moore” than “more Moore”

Other than Moore communities, e.g. BioMed

Key application areas, e.g. energy management

Others:
- environment
  water quality sensing
  air quality sensing
  etc.
- security
  many projects ongoing, cf. Homeland security in the USA

Mixing technologies / communities
- magnetics + CMOS
- .....

Be aware of globalization

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Advanced processes @ CMP

as of 2009

130 nm	2003	:	300 ICs
90 nm	2004	:	279 ICs
65 nm	2006	:	115 ICs
45 nm	2008	:	4 ICs
40 nm	2009	:	
	Total	:	698 ICs to date

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130 nm

Institutions	Town	Country	Institutions	Town	Country
U. Catholique de Louvain	Louvain La Neuve	BELGIUM	I.N.F.N. Genova	Genova	ITALY
Faculté Polytechnique de Mons	Mons	BELGIUM	Politecnico di Milano	Milano	ITALY
Technical U. of Denmark	Lyngby	DENMARK	U. of modena and reggio emilia	Modena	ITALY
VTT Information Technology	Espoo	FINLAND	INFN	Pavia	ITALY
Helsinki U. of Technology	Helsinki	FINLAND	U. degli studi di Pavia	Pavia	ITALY
U. of Turku	Turun Yliopsito	FINLAND	INFN - Pisa	Pisa	ITALY
CIM PACA	Biot	FRANCE	ETRI	Gwangju	KOREA
IMS	Bordeaux	FRANCE	U. of Malta	Msida	MALTA
CEA	Bruyères le Chatel	FRANCE	Catena Holding B.V.	Delft	NETHERLANDS
ENSEA	Cergy Pontoise	FRANCE	Delft U. of Technology	Delft	NETHERLANDS
U. de Bourgogne	Dijon	FRANCE	Philips Research	Eindhoven	NETHERLANDS
Centre Micro. de Provence-Georges Charpak	Gardanne	FRANCE	U. of Oslo	Oslo	NORWAY
SUPELEC	Gif sur Yvette	FRANCE	Nanyang Technological U.	Singapore	SINGAPORE
CMP	Grenoble	FRANCE	U.de Barcelona	Barcelona	SPAIN
ENSERG	Grenoble	FRANCE	Balearics Islands U.	Palma de Mallorca	SPAIN
iROC Technologies	Grenoble	FRANCE	U. of Cantabria	Santander	SPAIN
LETI/CEA	Grenoble	FRANCE	Instituto Microelectonica Sevilla	Sevilla	SPAIN
TIEMPO	Grenoble	FRANCE	U. of Seville Escuela Sup. de Ing.	Sevilla	SPAIN
TIMA	Grenoble	FRANCE	Chalmers U.of Technology	Gothenborg	SWEDEN
L2MP Polytech	Marseille	FRANCE	Linköping U. - ISY	Linköping	SWEDEN
ENST	Paris	FRANCE	ETH Zentrum IIS	Zurich	SWITZERLAND
UPMC Paris 6	Paris	FRANCE	Imperial College of Science	London	U.K
ENSSAT	Rennes	FRANCE	U. of Southampton	Southampton	U.K
IMS	Talence	FRANCE	U. of Massachusetts	Amherst	USA
LAAS	Toulouse	FRANCE	UC Berkeley - BWRC	Berkeley	USA
Heinz Nixdorf Institute	Paderborn	GERMANY	U. of Virginia	Charlottesville	USA
U. of Paderborn, High Frequency Elect. Dept	Paderborn	GERMANY	U. of Texas at dallas, Dept of EE	Dallas	USA
U. of Stuttgart	Stuttgart	GERMANY	Stanford U.	Stanford	USA
National Technical U. of Athens	Athens	GREECE	SiBeam Inc.	Sunnyvale	USA
U. di Bergamo	Bergamo	ITALY			
TOTAL: 59 Institutions from 17 countries					

Institutions having submitted circuits 130nm CMOS

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90 nm

Institution	Town	Country
U. of Calgary	Calgary	CANADA
U. of Waterloo	Waterloo	CANADA
Carleton U.	Carleton	CANADA
Dalhousie U.	Halifax	CANADA
University of Guelph	Guelph	CANADA
University of Saskatchewan	Saskatoon	CANADA
U. of British Columbia	Vancouver	CANADA
U. of Toronto	Toronto	CANADA
Ecole Polytechnique de Montréal	Montréal	CANADA
McGill U.	Montréal	CANADA
CMC Microsystems	Kingston	CANADA
U. of Alberta	Edmonton	CANADA
U. of Macau	Macau	CHINA
Technical U. of Denmark	Lyngby	DENMARK
VTT Information Technology	Espoo	FINLAND
U. of Turku	Turun Yliopisto	FINLAND
ISEN	Lille	FRANCE
IMEP	Grenoble	FRANCE
THALES	Palaiseau	FRANCE
U. of Stuttgart	Stuttgart	GERMANY
U. of Paderborn	Paderborn	GERMANY
RWTH Aachen	Aachen	GERMANY
U. degli studi di Pavia	Pavia	ITALY
Politecnico di Milano	Milano	ITALY
U. degli studi di Pisa	Pisa	ITALY
U. of Perugia	Perugia	ITALY
U. of Parma	Parma	ITALY
U. of Modena	Modena	ITALY
Istituto Nazionale di Fisica Nucleare	Pavia	ITALY
U. of Oslo	Oslo	NORWAY
Norwegian U. of Sc. & Techno	Trondheim	NORWAY
Novelda as	Kviteseid	NORWAY
U.of the Philippines	Quezon City	PHILIPPINES
U. Politechnica de Catalunya	Barcelona	SPAIN
Instituto Microelectronica Sevilla	Sevilla	SPAIN
Linköping U. - ISY	Linkoping	SWEDEN
ETH Zentrum IIS	Zurich	SWITZERLAND
University of Neuchatel	Neuchatel	SWITZERLAND
CERN	Genève	SWITZERLAND
Imperial College London	London	U.K
U. of Southampton	Southampton	U.K
SUN Microsystems	Montain View	USA
UC Berkeley - BWRC	Berkeley	USA
U. of Michigan	Ann Arbor	USA
Stanford U.	Stanford	USA
Massachusetts Inst. of Technology	Cambridge	USA
UCLA	Los Angeles	USA
Achronix Semiconductor LLC	Ithaca	USA
U. of Texas	Dallas	USA
Georgia Institute of Technology	Atlanta	USA
U. of Virginia	Charlottesville	USA
U. of Washington	Seattle	USA
TOTAL	**52 Institutions from 14 countries**	

Institutions having submitted circuits 90nm CMOS

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65 nm

Institution	Town	Country
Katholieke Universiteit	Leuven	BELGIUM
U. of Calgary	Calgary	CANADA
U. of Alberta	Edmonton	CANADA
McGill U.	Montréal	CANADA
U. of Toronto	Toronto	CANADA
U. of British Columbia	Vancouver	CANADA
U. of Waterloo	Waterloo	CANADA
U. of Macau	Macau	CHINA
Centre Micro. de Provence-Georges Ch	Gardanne	FRANCE
LETI/CEA	Grenoble	FRANCE
ISEN	Lille	FRANCE
ENST	Paris	FRANCE
IMS	Talence	FRANCE
LAAS	Toulouse	FRANCE
U. of Stuttgart	Stuttgart	GERMANY
U. of Wuppertal	Wuppertal	GERMANY
Politecnico di Milano	Milano	ITALY
U. of Tokyo	Tokyo	JAPAN
Delft U. of Technology	Delft	NETHERLANDS
Nanyang Technological U.	Singapore	SINGAPORE
U. of Pretoria	Pretoria	SOUTH AFRICA
Universitat Politechnica de Catalunya	Barcelona	SPAIN
Linköping U. (ISY)	Linköping	SWEDEN
SP Devices AB	Linköping	SWEDEN
Lund U.	Lund	SWEDEN
ACREO AB	Norrkoping	SWEDEN
Ericsson AB	Stockholm	SWEDEN
U. of Massachusetts	Amherst	USA
U. of Michigan	Ann Arbor	USA
Georgia Institute of Technology	Atlanta	USA
UC Berkeley - BWRC	Berkeley	USA
U. of Virginia	Charlottesville	USA
U. of California	Davis	USA
U. of Minnesota	Minneapolis	USA
Columbia U.	New York	USA
Arizona State U.	Tempe	USA
TOTAL: 36 Institutions from 13 countries		

Institutions having submitted circuits 65nm CMOS

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By geographical area

	130nm	90nm	65nm	45nm
CANADA	-	76	9	
EUR	267	98	74	
USA	29	102	21	4
RoW	4	3	11	
TOTAL	**300**	**279**	**115**	**4**

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By the time

	130nm	90nm	65nm	45nm
2003	1			
2004	37			
2005	60	31		
2006	61	57	1	
2007	58	86	23	
2008	34	68	33	4
S1 2009	49	37	58	
TOTAL	**300**	**279**	**115**	**4**

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Globalization

Every country or continent is a high cost country or continent to another one at the time of global markets. Moving dynamically and quickly.

- ➔ **Keep students, researchers, industrialists ahead of others**
- ➔ **Train on advanced processes and design methods, go for challenging issues**

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Nobody is safe…

ADIDAS will move manufacturing from China to India, Laos, Vietnam,… [Le Monde, August 2008]

Production costs: USA vs China, +36% in 2006, +17% in 2008

India: outsourcing the outsourcing

CNRS INPG UJF

Herald Tribune – 25 September 2007

India outsources its own outsourcing

Pioneer nation fends off new rivals

By Anand Giridharadas

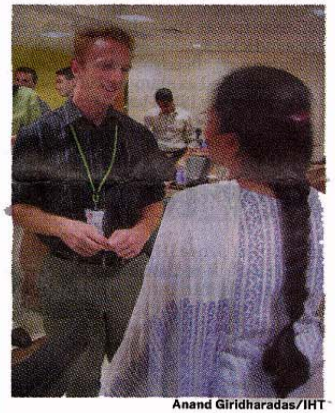
MYSORE, India: From across India, thousands of recruits report to the Infosys Technologies campus here in the deep south of India. Amid the manicured lawns and modern buildings, they learn the finer points of software programming.

But lately, packs of foreigners have been strolling the campus. Many are Americans, recently graduated from college. Some had been pursued by coveted employers like Google. Instead, they accepted a novel assignment from Infosys, the Indian technology giant: Fly here to learn programming from scratch, then return to the United States to work in the Indian company's back office.

Now India is outsourcing outsourcing.

One of the constants of the global economy has been companies moving tasks — and jobs — to India, where they could be done at lower cost. But rising wages for programmers here, a strengthening currency and companies' need for workers in their clients' time zones or for workers who speak languages other than English are challenging that model.

India is facing increased competition from countries seeking to emulate its success as a back office for wealthier neighbors: China for Japan, Morocco for France and Mexico for the United States, for instance.



Anand Giridharadas/IHT

Oliver Carter, an American hired by Infosys, talking with Vaishali Raoke, an instructor, in Mysore, India.

Looking to beat back these new rivals, leading Indian companies are opening back offices in those countries, outsourcing work to them before their current clients do.

Many executives in India now concede that outsourcing, having rained most heavily on India, will increasingly sprinkle tasks across the planet. The future of outsourcing, said Ashok Vemuri, an Infosys senior vice president, is "to take the work from any part of the world and do it in any part of the world."

In May, an Infosys rival, Tata Consultancy Services, announced a new back office in Guadalajara, Mexico; it already has 5,000 employees in Brazil, Chile and Uruguay. Cognizant Technology Solutions, with most of its operations in India, has now opened back offices in Phoenix, Arizona, and Shanghai. Wipro, another Indian company, has outsourcing offices in Canada, China, Portugal, Romania and Saudi Arabia, among others.

Last month, Wipro said it was opening a software development center in Atlanta that would hire 500 programmers in three years.

In a poetic reflection of the new face of outsourcing, the chairman of Wipro, Azim Premji, told Wall Street analysts this year that he was considering hubs in Idaho and Virginia, in addition to Georgia, to take advantage of "states which are less developed," Premji said.

Infosys is building an archipelago of back offices — in Mexico, the Czech Republic, Thailand and China, as well as in low-cost regions of the United States. The company wants to become a global matchmaker: Any time a company wants work done somewhere else, even just down the street, Infosys hopes to get the call.

It is a peculiar ambition for a company that symbolizes the flow of tasks from the West to India. Most of Infosys's 75,000 employees are Indians in India, and they account for most of the company's $3.1 billion sales in the year that ended March 31, from clients like Bank of America and Goldman Sachs Group. "India continues to be the No. 1 location for outsourcing," S. Gopalakrishnan, the company's chief executive, said in an interview by telephone.

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