Teaching Analog Design Concepts in Deep Submicrometric Technologies.

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Abstract—**In order to perform hand calculations in an analog design, the technological parameters involved in the square law equations of the MOSFET must be known for different widths and lengths, for both *n* and *p* transistors. Extracting this information from an advanced model such as BSIM4 is not a simple matter for the novel designer or under graduated student. This paper proposes the use of electric simulation combined with MATLAB functions to extract the required parameters for a first cut design.**

Keywords.- Education; Analog Design; Parameter Extraction; MOSFET Models.

I. INTRODUCTION

The electronic design is an iterative process. This task starts with a set of specifications, which are mapped into an electronic system aimed to meet the initial requirements. Simulation is used to verify the validity of the proposed design concerning the given needs. Analog circuit design uses a set of equations mainly based in the so called "square law model" to accomplish the mentioned mapping. Those equations proposed by Sah in 1962 [1] are simply and easy to use. These equations are also known as Level 1 model within SPICE. They give a first estimation of the transistor sizes in developing a basic building block such as a voltage comparator or an operational amplifier. However this model functions well for transistors with long channel length (*L*) and wide width (*W*) [2]. As technology improves and smaller transistors are being fabricated, advanced models for simulation in SPICE-like programs have been developed, for instance, the BSIM4 model is very popular for simulation of nano-metric devices [3]. This model includes, among others, the effects of velocity saturation present in deep sub-micrometric devices, which are neglected by the Sah model. This fact brings a consequent mismatch of more than 100%, if the size of a transistor is calculated to meet certain transconductance or output resistance requirement using the Level 1 model and simulating using the BSIM4 model [4]. This situation is quite confusing for students or novel designers when being introduced into the world of analog design with current technologies having an *L* under one micron, since the student does not feel, that she or he has "control" over the design. This circumstance brings besides confusion, frustration and a tendency to use the simulator as a "magic box" to obtain aspect ratios of transistors by means of parametric analysis changing *W* and *L* arbitrarily until the needs are found. This method does not give any feeling nor insight of the circuit under design and in many cases the students end the course with the wrong believe, that analog circuit design does not have an accurate approach more than trial and error. In this paper, a method to extract the parameters needed by the Level 1 model from electric simulations performed in SPICE is presented. Here, while in an electric simulator the BSIM4 model for nano-metric devices is used, functions of MATLAB are handled to find out the values of the square law model parameters. Sah model parameters are important because, although the majority of the literature concerned with CMOS analog circuit design includes a chapter regarding sub-micrometric devices [4,5,6] uses the simple model to derive the behavior equations of both the transistors and basic building blocks typical of analog systems. Therefore, Level 1-based equations are the starting point to perform hand calculations in analog circuit design. The presented approach has been used with success, last year in analog circuit design courses in two universities in Mexico. The paper is organized as follows: Next section presents an overview of the courses organization, after that, the proposed approach is presented in detail. Section 4 shows a basic building block designed by students who attended the course, using the information found in section 3. Finally some conclusions are given.

II. COURSES OVERVIEW.

The courses in both universities were organized in 12 weeks, six hours per week. They comprised the typical themes of a basic Analog CMOS Circuit Design course, namely, MOS transistors, Single Stage Amplifiers and Differential Amplifiers, two topics were included: Short Channel Effects and Technology Characterization, The course structure was the following:

- Introduction
- MOS transistors and Models
- Short Channel Effects
- Technology Characterization
- Single Stage Amplifiers
- Differential Amplifiers

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They only comprised electric design, no layout aspects were covered, since they are left for a second course.

III. Extracting Sah's Model Parameters in Matlab from Electric Simulations

A. The Square Law Model

The well known simple model relating the drain current and the applied voltage between gate and source in a MOSFET, when operating in its linear region, is given by:

$$i_D = \frac{K'_{LIN} W}{L}\left[\left(v_{GS} - V_T\right) - \frac{v_{DS}}{2}\right] v_{DS}\left(1 + \lambda v_{DS}\right) \quad (1)$$

The parameters involved in this equation are defined as follows:

K'_{LIN}.- Intrinsic transconductance parameter in the linear region.

V_T.- Threshold voltage of the device.

λ.- Channel length modulation parameter.

The quantities v_{GS} and v_{DS} are the voltages applied between gate and source and drain to source respectively. This region of operation finds limited application in CMOS analog circuit design as for example in a voltage controlled resistor. Of more interest is the saturation region, in which eq. (1) becomes:

$$i_D = \frac{K'_{SAT} W}{2L}\left(v_{GS} - V_T\right)^2\left(1 + \lambda v_{DS}\right) \quad (2)$$

Here, K'_{SAT} is the intrinsic transconductance parameter in saturation, which is usually smaller than K'_{LIN}. Since a bulk to source voltage (v_{SB}) usually appears in stacked devices, in the simple model V_T is defined as follows:

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right] \quad (3)$$

Where, γ is the bulk threshold parameter and ϕ_F the strong inversion surface potential. As it will be shown γ is easily found and can be used to estimate V_T in a cascode-connected device. From eq. (2), the small signal transconductance and output resistance are derived as:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{K'_{SAT} W}{L}\left(v_{GS} - V_T\right) \quad (4)$$

$$r_O = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1} = \frac{1}{\lambda i_D} \quad (5)$$

These last equations reflect the importance of having values of K'_{SAT}, V_T, λ and γ to calculate the aspect ratio of a transistor which has to meet certain g_m or r_O. However, due to short and narrow channel effects present in deep submicrometirc devices, the value of the mentioned parameters is dimension dependent. For this reason it is necessary to do several simulations for the different channel dimensions prospective to be used thorough the designs.

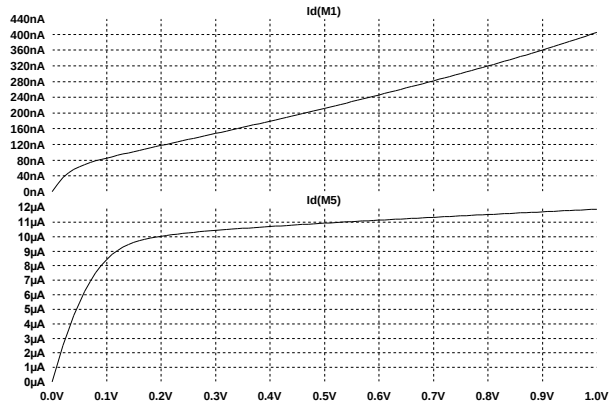

Figure 1. I_D-V_{DS} Curves of MOS transistors with aspect ratio of 3 and L=100nm (up) and L=2μm (down).

B. Electric Simulations

Figure 1 shows the simulated response of the drain current of two MOS transistors, both having a W/L=3 but one with L=100nm and the other with L=2μm. In these simulations, the BSIM4 model of the IBM 9RF technology with feature size of 90nm available through MOSIS were used [7]. From this curve K'_{LIN} and λ can be determined once the (v_{GS}- V_T) quantity, also known as over drive voltage (V_{OV}) has been chosen [2]. Figure 2 shows the so called transconductance characteristic of the MOSFET for different values of v_{SB}, from them, K'_{SAT}, V_T and γ will be obtained. Again, the response of large and short channel devices is plotted.

C. Parameter Extraction through MATLAB

Now, enough data to be used for the estimation of the above mentioned parameters has been collected. If the *i-v* data got in the simulations are exported in a text file, they can be used to apply numerical techniques such as linear regression in order to compute, with in certain error margin, the value of the searched quantities.

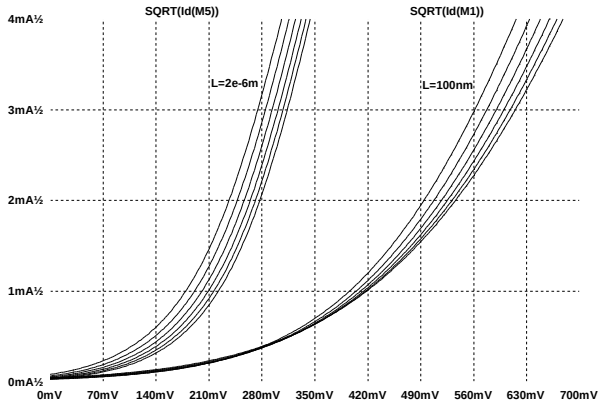

Figure 2. Transconductance characteristic for short and long channel devices.

At this point, any programming language such as "*C*" could be used, but for simplicity, the *MATLAB* program was chosen, since an easy and quick way to determine the information in question was seek, besides, the objective was to have values of the parameters suited to start hand calculations in a required design, not to exercise programming techniques or numeric methods. As known, *MATLAB* has an extended library of functions to perform linear regression and curve fit. The function `polyfit` [8] acts over a data set and returns the coefficients of a polynomial of order *n* which best fits the given function. For instance, the following code lines take the data stored in the vectors `id` and `vds` and approximate their relation with a polynomial function of order one (a straight line) the resulting coefficients are stored in the vector `coef`:

```
coef=polyfit(id, vds, 1)
m=coef(1,1) % slope
b=coef(1,2) % y-intercept
```

If the vector `id` contains the drain current data in the saturation region, the value of the parameter λ is obtained by dividing `m` by `b` as indicated in the chapter 4 of [2]. This approach was used taken as input vectors the *i-v* pairs obtained in electric simulations. A simple program in *MATLAB* was written by the students in order to organize the information into the regions of interest, i. e.: drain current in linear region, drain current in saturation and so on, for the different chosen transistors. The mentioned function was applied to the input vectors and the resulting coefficients were used to obtain the desired values. Finally the information was organized into tables. Figure 3 shows some of the results for K'_{SAT}, and V_T of a short channel device.

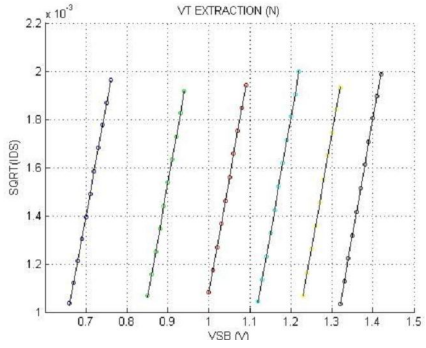

Figure 3. Simulation Data and Fit Line obtained in MATLAB for NMOS Transistors.

IV. Case Study of a Design: The Flipped Voltage Follower

As a case study, the electric design of a voltage follower using the topology proposed in [9] was carried out by the students at the end of the course. The schematic diagram of this circuit is depicted in figure 4.

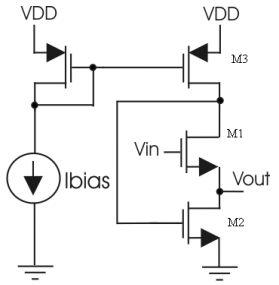

Figure 4. A Flipped Voltage Follower.

This circuit acts as a non inverting voltage follower well suited for low voltage applications. It has almost unitary voltage gain and an output resistance given by

$$r_{OUT} = \frac{2}{g_{m1} g_{m2} r_{O1}} \tag{6}$$

With the parameter values found and collected in table 1 for NMOS transistors, a flipped voltage follower was designed to have a voltage gain of one and to drive a capacitive load (C_L) of 0.5pF at 100MHz. This load capacitance requirement was chosen in order to preserve stability of the circuit following the condition:

$$\frac{C_L}{C_{DM3}} < \frac{g_{m1}}{4 g_{m2}} \tag{7}$$

Where, C_{DM3} is the capacitance seen from the drain of M3 to ground. Figures 5 and 6 are showing the simulated results of the DC transfer curve of the circuit and its transient response respectively. Recall that electric simulations were done using the BSIM4 model of the IBM 9RF technology and 1V of power supply. A similar characterization work for PMOS transistors was done, although it is not reported here.

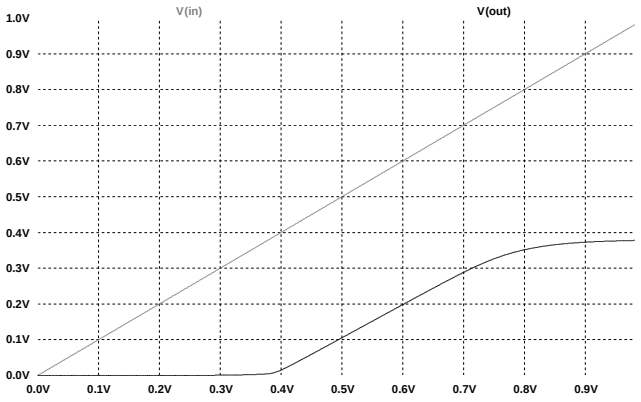

Figure 5. DC transfer response of the designed flipped voltage follower.

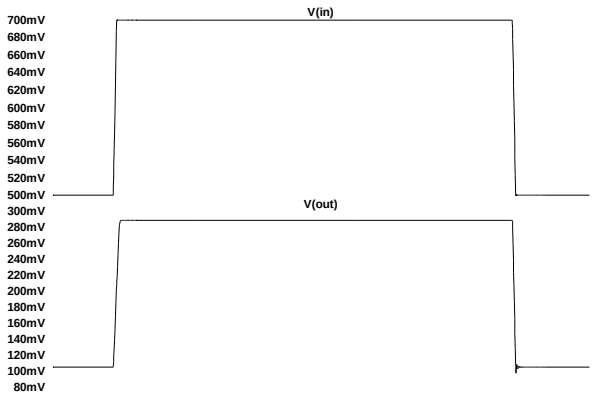

Figure 6. Transient response of the designed flipped voltage follower at 80MHz with a C_L=0.5pF.

TABLE I. ESTIMATED PARAMETER VALUES FOR NMOS TRANSISTORS

W/L	K_{LIN} (A/V^2)	K_{SAT} (A/V^2)	V_T (V)	λ (V^{-1})	γ ($V^{1/2}$)
10μm/1μm	$3.96x10^{-4}$	$766x10^{-6}$	$205x10^{-3}$	0.1	0.41
200nm/2μm	$9.63x10^{-3}$	$535x10^{-6}$	$330x10^{-3}$	1.12	0.42

V. CONCLUSIONS

An easy and comprehensive method to extract the technological parameters in a deep submicrometric technologic process was presented. The so obtained results are useful in order to have a starting point when a basic building block is going to be designed and the equations describing the circuit characteristics were derived using the MOS simple model. The student or novel designer should always first characterize the technology in use in a similar way before starting to carry out any design, otherwise, large errors in the hand calculations will be obtained and any insight in the designed circuit will be gained. The proposed methodology has been used to teach analog circuit design concepts in post-graduate courses, using advanced MOS models for the electric simulation of deep submicrometric devices. Obtaining in such a way the values of the quantities involved in the square law MOSFET model is a very constructive experience and gives to students a good comprehension of the operation of MOS transistors.

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