An Educationnal Approach to Electromagnetic Compatibility of Integrated Circuits

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Abstract— **This paper presents the strategies used for effective teaching in integrated circuit (IC) design under Electromagnetic Compatibility (EMC) constraints. It presents the general context of EMC of ICs and details the EMC-aware IC design course given in companies and several institutes in France. Collaborations with industry have produced a set of learning resources and design tools to support the development of industry relevant EMC skills and lifelong learning skills. The courses enable students to learn about EMC measurements and modeling at IC level and their implications using a set of user friendly tools. The courses taught in university and in industry have consistently produced high levels of student/engineer satisfaction.**

Keywords: EMC, Integrated circuits, parasitic emission, susceptibility, standards, IEC, IBIS, modeling

I. CONTEXT

Electromagnetic compatibility (EMC) is considered to be the third cause of integrated circuit (IC) redesign after design errors and Electrical Overstress. EMC is a fundamental constraint that components must meet to ensure the simultaneous operation of all nearby electronic devices and the safety of users. Numerous courses and educational books have addressed EMC at system, cable [1] and printed-circuit board (PCB) levels [2]. However, semiconductor devices are often the source as well as the victim of electromagnetic interferences, as described in the research compilation [3]. Possible mechanisms for coupling of electromagnetic noise at integrated circuit (IC) level include the wire connections such as the supply lines, the coupling of the package leads to electric or magnetic field, or even the coupling of the induced interferences directly to the silicon chip (Fig. 1). Also represented in the figure are couplings through cables and PCB tracks.

Ensuring EMC at circuit level implies an effective reduction of noise sources and disturbance origins, in order to comply with EMC standards defined by the application of by the IC customers. Its modeling has become mandatory to ensure a predictive approach of EM-induced perturbation risk, which requires tools, models and specific EMC knowledge.

Until recently, no specific course focused on EMC of ICs has been made available, mainly because of the intrinsic complexity of the topic, which requires strong skills both in electromagnetism, electricity and microelectronics, the lack of expertise, and the high degree of confidentiality regarding EMC-related design issues. In this paper, we present what we believe to be the first 2-days course only focused on EMC of ICs, based on the latest research results available from the community of EMC-IC experts [4].

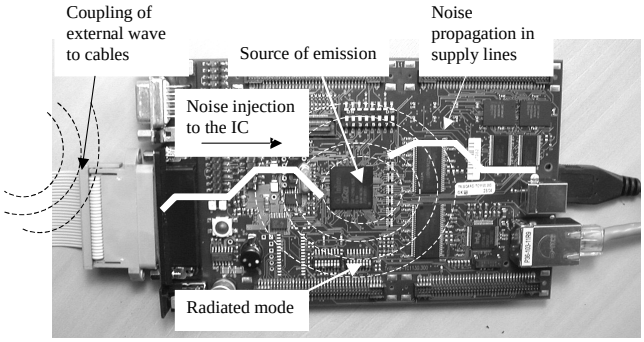

Figure 1. Illustration of electromagnetic compatibility at integrated circuit level (From [3])

II. EMISSION, IMMUNITY

A. Integrated Circuit Emission

Parasitic emission caused by the switching activity of integrated circuits (ICs) has increased in importance with the tremendous progress in Complementary Metal-Oxide Semiconductor (CMOS) technology. When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pluses provokes enormous current flows within the chip, close to 100 A in the latest generation of high performance micro-processors. The switching of internal gates induces transient current flow within the circuit and its surroundings, as shown on figure 2. Supply and bus wires can convert the transient currents into voltage drops on power and ground supplies. Parasitic inductances of interconnections are the main responsible of voltage drops [1-3]. Voltage drops may propagate to circuits sharing the same supply network, which provokes conducted and radiated emission.

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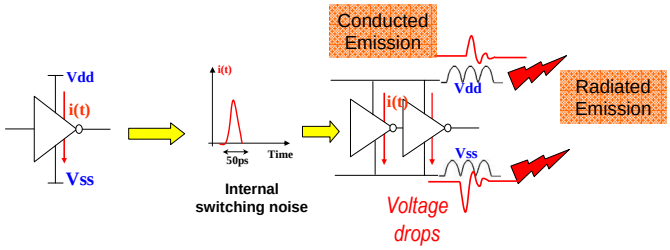

Figure 2. IC parasitic emission due to switching activity and parasitic power supply interconnections

There exists a diverging trend between, on one side, the customer pressure for low-emission IC, and in the other side, intrinsic emission levels which tend to increase and to broaden in frequency domain.

B. *Integrated Circuit Susceptibility*

The trend towards nano-scale devices has major consequences on integrated circuits (ICs) immunity. First, the constant supply voltage decrease reduces the static noise margin of electrical signals and thus increases the IC susceptibility to RFI. Also, as cut-off frequencies increase, circuits become sensitive to faster transient signals.

With the newest technologies, nearly one billion devices related to mixed analogue, digital and power technologies share the same piece of silicon. Some parts of the chip generate EMI (digital and power parts) while the others have very low sensitivities regarding the EMI level (analogue and RF parts). It is an issue to ensure that all the embedded functions are able to operate (auto-compatibility).

Meanwhile, IC customer requirements in terms of EMC tend to increase. These opposite trends require immunity design guidelines, specific tools, expertise and ways of precise measurements of EMC performances.

III. COURSE DESCRIPTION

The course is targeted to engineering students in master level, as well as IC designers in industry to address the needs for specific training in EMC-award IC design. The two-days course consists in 6 main parts:

- Introduction to EMC for ICs
- Basic Concepts in EMC of ICs
- Measurement methods for emission and susceptibility
- Modeling techniques
- Design Guidelines for improved EMC
- Future challenges

Half of the time is spend with lectures, including problem-based learning, exercises, and demonstrations; the other half is dedicated to practical training.

The first part presents the challenges for electromagnetic compatibility of integrated circuits and recalls some key examples of IC redesigns because of EM-related non compliance. A set of basic concepts is proposed in the second part, covering specific units, impedance, interconnects, origin of noise, noise margins, time/frequency conversion and 50 Ω matching. The third part focuses on the standard measurement of the IC emission [5] and susceptibility [6]. The fourth part is related to modeling approaches for predicting EMC, based on standards such as IBIS, ICEM, and ICIM [7]. The fifth part is dedicated to the presentation of guidelines to reduce emission and improve immunity at IC level. Finally, roadmaps and future challenges are briefly reviewed, inspired from [8].

IV. PRACTICAL TRAINING

A. *EMC of ICs in practice*

To support and illustrate the course, we have developed a freeware called IC-EMC [9], a windows-based software demonstrator which aims at simulating parasitic emission and susceptibility of integrated circuits. The full package can be downloaded from www.ic-emc.org, a non-profit site dedicated to EMC of integrated circuits. The tool IC-EMC includes a conventional schematic editor, (See Fig. 3), a set of tools to help user to build EMC models, an interface to Spice for analog simulation and a post-processor for easy comparison between measured and simulated parasitic emission and susceptibility. The tool is used by the teacher as an illustration for most basic concepts covered during the formal course, and by students during practical training sessions.

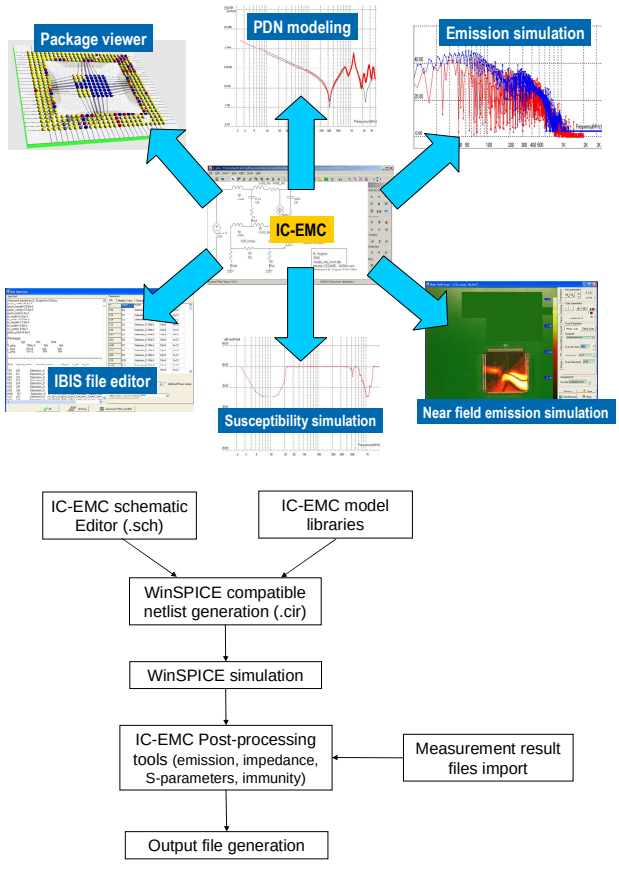

Figure 3. The IC-EMC capabilities in terms of emission and immunity prediction, and the generic flow used to simulate EMC at integrated circuit level

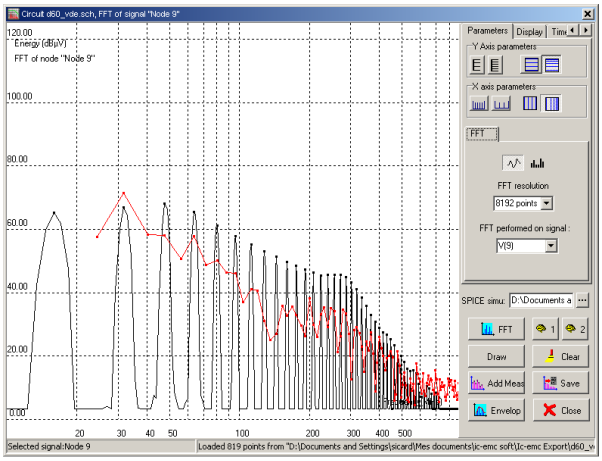

Figure 4. An example of comparison between measured and simulated parasitic emission conducted during the practical session of the course

A set of tools with significant added value for EMC analysis are used during the training:

- An emission model generator which translated an IC specification directly into an approximated noise model. Students are asked to specific a microcontroller and forecast its emission level, without any specific knowledge of the layout details.
- A near- magnetic field estimator based on elementary current dipole radiation. Students may illustrate field cancelation, loop effect reduction at a simple click.
- A library of common standard IEC models, to ease the simulation of 1/150Ω conducted mode and TEM cell radiated mode measurement methods.
- A 3D package viewer based on IBIS, to illustrate the role of R,LC parasitic effects due to package and die connection.

V. EVALUATION

Since the early trainings started in 2002, more than 20 sessions involving 300 students and engineers have been organized, either in a one-day or two-days format. The evaluation of the course impact has made through 1à questions listed in Table I. At the end of this course, the majority of students said they understood the mechanisms of parasitic emission and susceptibility, and felt confident in their ability to handle standard measurements of emission and susceptibility at IC level. Most of IC designers also felt they could take part in a global EM-improvement strategy, and were willing to apply "golden design rules" to address circuits with interference problems.

The evaluation results shown in Fig. 5 include both initial training in engineering departments (ISEN France, ENSME France) and in companies (e.g Nokia, On-semiconductor). It can be observed that not all students find the topic in close relation with their studies, while the vast majority of engineers in companies have found the course highly profitable for their daily work.

TABLE I
COURSE EVALUATION QUESTIONNAIRE

#	Question
1	I appreciated the contents of the training.
2	The level of the training is in accordance with my expectations.
3	The balance between theory and practice was acceptable
4	The contents was adapted to life-long learning.
5	I appreciated the documents given in the training.
6	I appreciated the way the training was taught
7	The contents is clearly related to my work/studies.
8	I may use the contents directly in my activities
9	The lecturer followed the initial planning
10	Overall I was satisfied with the quality of this course.

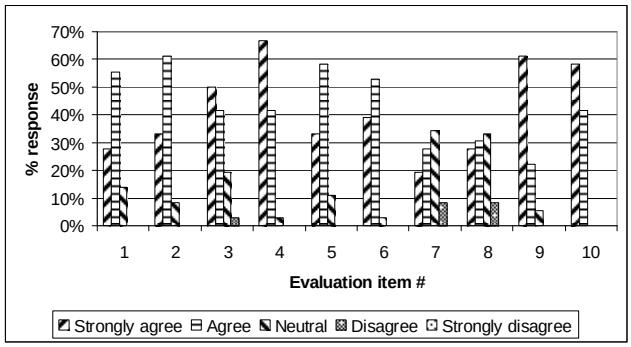

Figure 5. Evaluation of the course "EMC of Ics" compiling 10 course feedback, for a total of more than 100 students

The very high satisfaction rate is also linked with the introducing of a practical training and problem-based approach during lectures, which reinforce discussion, interaction, questions and answers from the audience.

CONCLUSION

This paper has introduced a novel course on EMC of ICs at engineering level, which was successfully taught in engineering schools as well as in industry to enhance the understanding of interference issues at component level and to give practical ways of improving electronic design for improved EMC.

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