Design of Energy-Aware Cyber-Physical Systems

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Many thanks to:
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SoC Platforms for Cyber-Physical Systems

Progress in semiconductor technology:
- microcontroller,
- sensors, power electronics,
- RF interfaces,
for complete systems in single package or chip!

(Picture: SINTEF/Infineon Austria)

Cyber-Physical Systems, WSN, AI, IoT, ...
Dependability, adaptivity, resilience,
networking 100,000s of nodes in focus.

mobility, autonomy = LOW/ULTRA-LOW POWER?
1. Why Energy/Power-Awareness?
2. Challenges ...
3. ... and help by model-based design
4. Lessons learned
   – Methodology
   – Architecture
Power Aware Design vs. Energy Aware Design

**Power Awareness**
- Power peaks below limit
- Caused by switching activities/capacities
- Heating, IR-Drop, crosstalk

**Energy Awareness**
- Energy for task below limit
- Caused by leakage
- Enable long run-times, autonomy

Not independent!
- (Trivial: Power = Energy d/dt)
- Efficiency of power supply, ...
Smart Systems … (as seen e.g. by EPoSS for Europe 2020)

1990
First generation:
- Sensing + actuation
- Signal conditioning, preprocessing
- Communication via bus interface

2005
Second generation:
- Multifunctional sensing, actuation, inference
- Predictive, adaptive
- Networking, partially autonomous

2020
Third generation:
- Self-calibrating, self-healing
- Artificial intelligence
- Self-organized network
- **Energy autonomous**

Internet of things
Smart home
Smart grid
Smart production

(Figure: BOSCH)

(Figure: Infineon)
Energy Harvesting Opportunities
(e.g. in Automobile)

**Generation:**
- Passive RFID
  
  0.1 $\text{uW} / \text{cm}^2$ Antenna
- Photovoltaics
  
  10 $\text{uW-15.000 uW} / \text{cm}^2$
- Active RFID – Active
  
  up to 4W, falls quadratic with distance
- Thermal
  
  some W, increases with temperature

**Energy-aware design:**
- Generation depends on location, scenario
- Consumption depends on use, design, ...

**Consumption:**
- Computing
  
  some $\text{uW}$
- Transmitting
  
  some $\text{mW}$
- Sensing
  
  (depends on kind of Sensor)
Smart Home, Smart Grid, Ambient Intelligence, e-Health
Smart Home - Really Smart?

### Number of Nodes (Home)
- Lighting: 10-50
- Windows open?: 10-20
- Doors?: 10-50
- Scenario recogn.: 20-50
- **... sum:** 10-100s

### Standby
- Today’s avg.: 1 .. 10 W
- Today’s best: 100 mW
- SmartCoDe’s ZigBee: 50-90mW
- Ambitious objective: 1 .. 10 mW

### Standby Power of Smart Building

<table>
<thead>
<tr>
<th>Number of Nodes</th>
<th>Today ...</th>
<th>2015?</th>
<th>Target for 2020?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Node</td>
<td>1 .. 10 W</td>
<td>100 mW</td>
<td>10 mW</td>
</tr>
<tr>
<td>10 Nodes</td>
<td>10 .. 100 W</td>
<td>1 W</td>
<td>100 mW</td>
</tr>
<tr>
<td>1000 Nodes</td>
<td>1 .. 10 KW</td>
<td>100 W</td>
<td>10 W</td>
</tr>
</tbody>
</table>

Energy aware + Power aware design for efficiency of power converters!
Design of Energy-Aware Cyber-Physical Systems

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Design: Hugo De Man (@Talk at 60th Anniversary of Manfred Glesner ...)

Software centric systems
(7th heaven?)

Application: usage, QoS requirements
Network: MAC, rouging
OS: power management strategies
Middleware: scheduling resources

Architecture: power gating, DVFS, ...
Circuit: Adiabatic, Sub-threshold, ...
Technology: leakage power, capacities, ...

Application development
„Platform“, fixed API
Circuit design

Hell of nano-scale physics
Example:
Advanced TPMS

Usage of hardware defined by
- Scenario & Application
- Communication protocols
- Architecture

Energy management:
- Know application and scenarios
- Develop power management strategy
- Match with RT-Level infrastructure
- Match with technology

Power consumed in hardware,
Battery for days.
Challenge 1:  
Power consumption vertically, EDA horizontally

Design today  
mostly horizontal

Needed for  
Power/energy aware design:

Application: usage, QoS requirements  
Network: MAC, rouging  
OS: power management strategies  
Middleware: scheduling resources  
Architecture: power gating, DVFS, ...  
Circuit: Adiabatic, Sub-threshold, ...  
Technology: leakage power, capacities, ...
Challenge 2: 

*What is the cause of power consumption?*

- "Due to command to do X from network"
- "The software running on the processor"
- "The processor/transceiver/..."!
- "Due to the physical scenario Y"
Can EDA help?

**Short answer:**
NO.

Unless you put all this in one formal model to enable overall system optimization!

**But:** modelling/simulation is first step!

- **Application:** usage, QoS requirements
- **Network:** MAC, rouging
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Model-based Approach, Concept

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Design issue modeled accurately

„Behavioural“ model
Model-Based Approach [Haase 2012]

+ **Means/tools to**
  - Estimate power at various levels of abstraction
  - Trace power consumption to its causes

**Cycle-accuracy**

- Microcontroller Emulators
  - ATEMU
  - MSPsim
  - AVRORA

- Operating System Emulators
  - TOSSIM
  - TOSSF
  - COOJA
  - Emsim

- Real-code application
  - Operating System + Drivers + API
  - Hardware Abstraction Layer (HAL)
  - Hardware interfaces

**Functional Simulation**

- Network and System Simulators
  - SNOPS
  - PAWiS
  - SensorSim
  - VisualSense
  - IDEA1
  - SENSE
  - Prowler
  - J-Sim
  - ns-2

**SystemC? with AMS, TLM ext.**

*e.g.*: **SYCYPHOS**
(SNOPS, SmartCoDe, ANDRES)
SystemC + TLM + AMS extensions!
SystemC AMS, Modelling AMS, RF, Physical systems

TDF Process

discrete Process

processing()
{
  out.write(...) 
}

H(s), H(z), DAE

out = f(in)

electr. network

R
C

ReCoSoC: Design of Energy-Aware Cyber-Physical Systems
Modelling Communication with TLM

TLM 2.0
- Models communication via buses
- Abstracts data granularity ("payload"), timing accuracy

Wireless TLM
- Route of packet in a WSN: forks, dead ends, ...
- Modeling "air": reflections, obstacles, etc. for wireless transmissions
WSN extensions for the TLM 2.0 generic payload [Damm 2009, 2010]

Packet sent:
Updated by node before it passes transaction to environment.

Packet from „Air“
Updated by environment before it passes transaction to nodes
• received signal quality
• routing
• power used for task
Power Profiling (1)

Transceiver:

...  
set_psm_state(run)  
...  
...  
set_psm_state(sleep)  
...  

Power state machine, Power states:

- run  
  Pr [W]

- sleep  
  Ps [W]

Power logfile
Power Profiling [Haase 2011]

M2M Commands

Transaction A->B: Get Pressure

Power Logfile

SW Activities

Listening
Receiving
Sensing

(Re-) Transmitting

Components

µP ISS (Power)
Transceiver (Power)
Sensor (Power)

Power models from SNOPS/SYCYPHOS library
Architecture Exploration: Non-ideal Behavior

**Complete model with assumed/measured parameters!**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Type</th>
<th>Default value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>sc_module_name</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>_gain</td>
<td>double</td>
<td>-</td>
<td>gain in dB</td>
</tr>
<tr>
<td>_ip3</td>
<td>double</td>
<td>-</td>
<td>IP3 in dBm</td>
</tr>
<tr>
<td>_ideal</td>
<td>bool</td>
<td>-</td>
<td>true for simulation of ideal LNA, otherwise false</td>
</tr>
</tbody>
</table>
Architecture Exploration: Power Management

Execution of TDF processes controlled by clk/enable signals (events), SW by Interrupts (events)
Architecture Exploration: X-Domain partitioning

Add Instruction Set Simulator(s) of processors to be used

Protocol Processor ASIC, DSP

μP Memory

Software Applikation Phy-App Layer

Control & Power Management

PowerDown

Clk, Enable

Interrupt

Add Instruction Set Simulator(s) of processors to be used

ReCoSoC: Design of Energy-Aware Cyber-Physical Systems
Example: Power profiling of TPMS with In-Car WSN; 18 8-Bit-uC with Firmware + Transceiver + Sensors
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(Video showing Driving scenario and estimated power assigned to processors, analog/RF, Sensors, SW activities, Transactions ...)

ReCoSoC: Design of Energy-Aware Cyber-Physical Systems
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Lessons learned (Methodology)

Key for „low power/energy“:
Sure all levels must be involved, but 2 things very useful

1. **Very early power budgeting** and estimation using functional models
2. Granularity of **infrastructure** for **power gating** (RFTS) or regulating (DVFS, AVFS) is key
   - **Bottom up**: determines standby power
   - **Top-down**: determines duty cycles
   - Important: Times for entering / leaving power states
     - Power converters
     - Clock generation (e.g. PLL)
Lessons learned (Architecture)

uC spend (too) much power/time for waiting, administrating peripherals!

Benchmark developed:

Specifically optimized re-configurable ASIC: 200 -> 0.12 nJ [Glaser 2010]
Lessons learned (Architecture)

Don’t wake processor for frequent, „simple“ tasks:

Use of
a) Simple, specific processor
b) Re-configurable system, optimized for specific task

Specifically optimized re-configurable ASIC: 0.12 nJ [Glaser 2010]