Design of Energy-Aware Cyber-Physical Systems

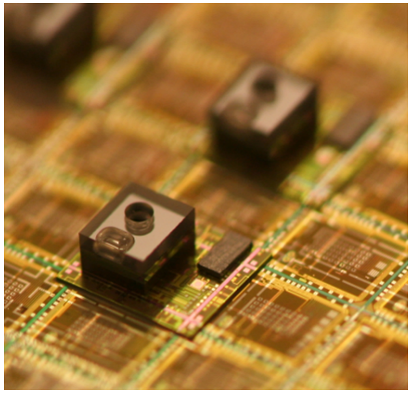
Prof. Dr. Christoph Grimm

Many thanks to:

Markus Damm, Jan Haase, Javier Moreno, Thomas Herndl, Stefan Mahlknecht, Josef Wenninger, Sumit Adhikari, Carna Radojicic, Jiong Ou, Florian Schupfer, Florian Brame

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

SoC Platforms for Cyber-Physical Systems



(Picture: SINTEF/Infineon Austria)

Progress in semiconductor technology:

- microcontroller,
- sensors, power electronics,
- RF interfaces,

for complete systems in single package or chip!

Cyber-Physical Systems, WSN, AI, IoT, ...
Dependability, adaptivity, resilience,
networking 100.000s of nodes in focus.

mobility, autonomy = **LOW/ULTRA-LOW POWER?**

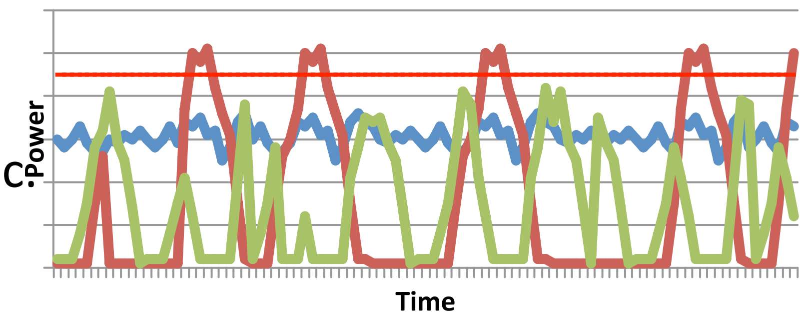
Design of Energy-Aware Cyber-Physical Systems

1. Why Energy/Power-Awareness?
2. Challenges ...
3. ... and help by model-based design
4. Lessons learned
   - Methodology
   - Architecture

Power Aware Design vs. Energy Aware Design

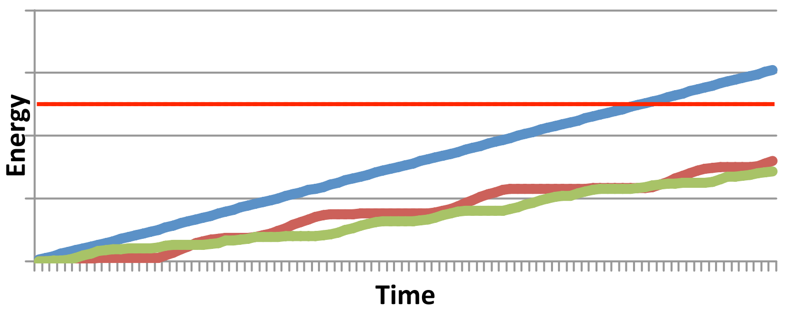
Power Awareness

- Power peaks below limit
- Caused by switching activities/capac...
- Heating, IR-Drop, crosstalk



Energy Awareness

- Energy for task below limit
- Caused by leakage
- Enable long run-times, autonomy

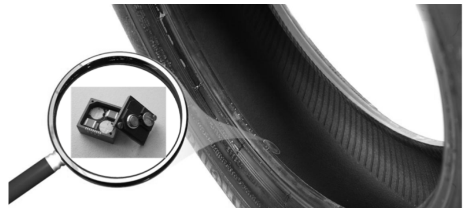


Not independent!

- (Trivial: Power = Energy d/dt)
- Efficiency of power supply, ...

Smart Systems ... (as seen e.g. by EPoSS for Europe 2020)

(Figure: BOSCH)



(Figure: Infineon)

Internet of things
Smart home
Smart grid
Smart production

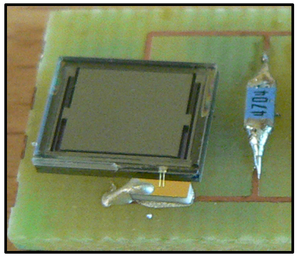
1990 — **2005** — **2020**

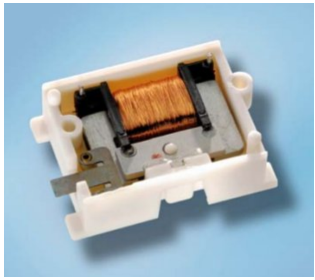
First generation:
- Sensing +actuation
- Signal conditioning, preprocessing
- Communication via bus interface

Second generation:
- Multifunctional sensing, actuation, inference
- Predictive, adpative
- Networking, partially autonomous

Third generation:
- Self-calibrating, self-healing
- Artificial intelligence
- Self-organized network
- **Energy autonomous**

Energy Harvesting Opportunities
(e.g. in Automobile)





Generation:

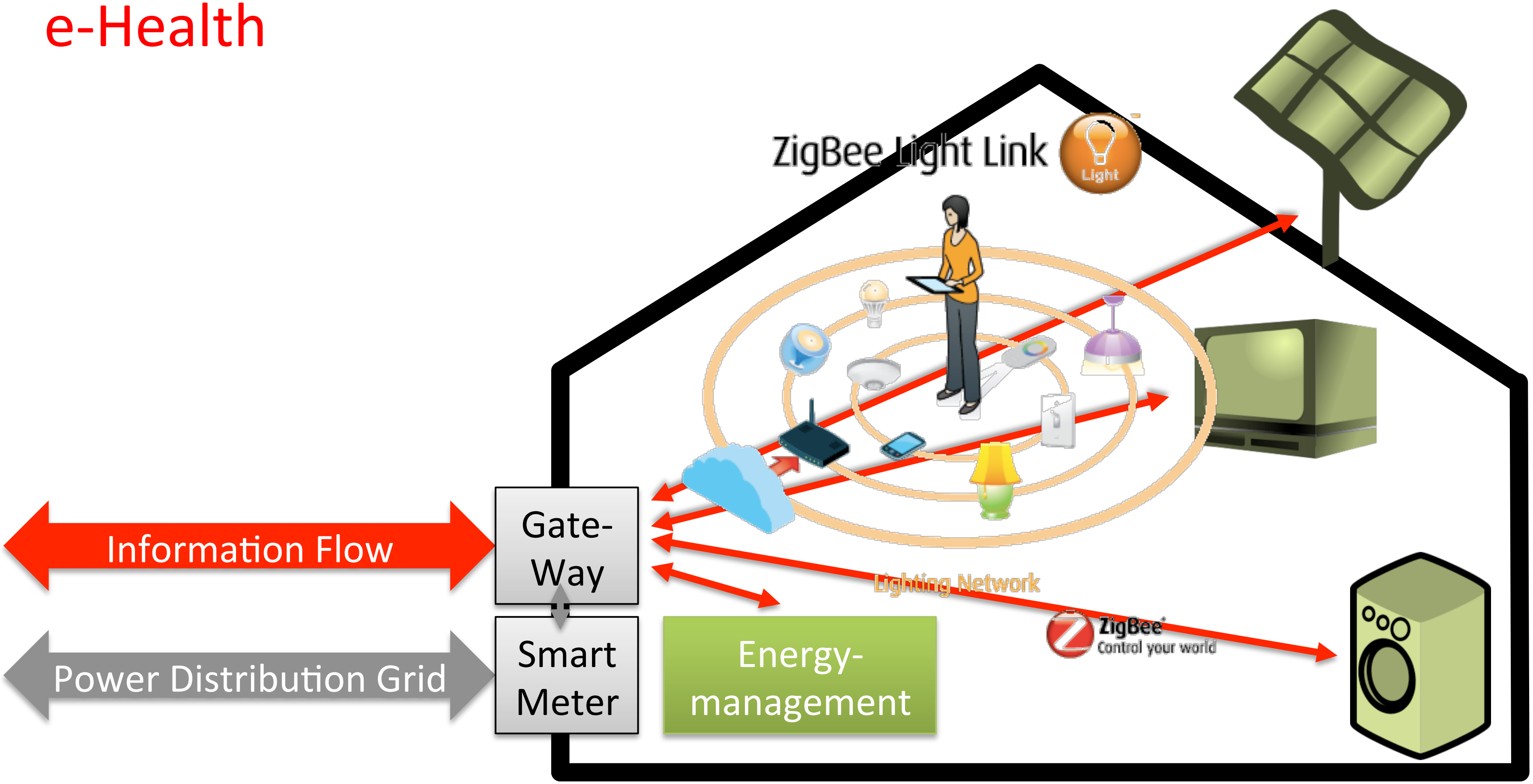
Passive RFID	0.1 uW / cm^2 Antenna
Photovoltaics	10 uW-15.000 uW / cm^2
Active RFID – Active	up to 4W, falls quadratic with distance
Thermal	some W, increases with temperature

Energy-aware design:
Generation depends on location, scenario
Consumption depends on use, design, ...

Consumption:

Computing	some uW
Transmitting	some mW
Sensing	(depends on kind of Sensor)

Smart Home, Smart Grid, Ambient Intelligence, e-Health



Smart Home - Really Smart?

Energy aware +
Power aware design
for efficiency of power converters!

Number of Nodes (Home)	
Lighting	10-50
Windows open?	10-20
Doors?	10-50
Scenario recogn.	20-50
... sum:	**10-100s**

Standby	
Today's avg.:	1 .. 10 W
Today's best :	100 mW
SmartCoDe's ZigBee:	50-90mW
Ambitious objective:	1 .. 10 mW

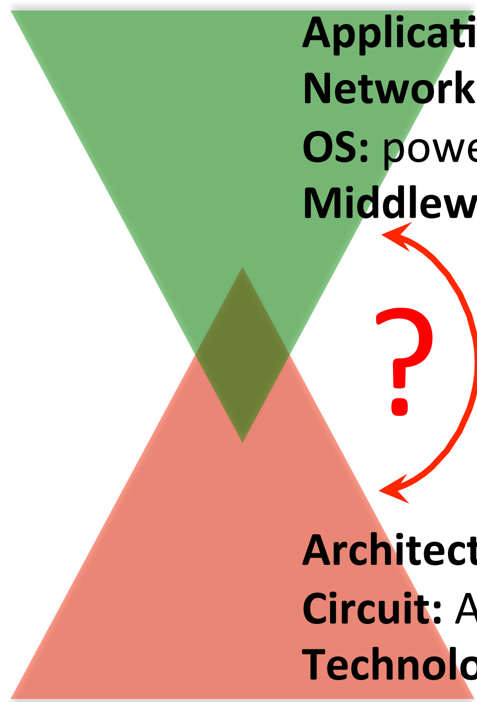
Standby Power of Smart Building	Today ...	2015?	Target for 2020?
1 Node	1 .. 10 W	100 mW	10 mW
10 Nodes	**10 .. 100 W**	1 W	100 mW
1000 Nodes	**1 .. 10 KW**	**100 W**	10 W

Design of Energy-Aware Cyber-Physical Systems

1. Why Energy/Power-Awareness?
2. Challenges ...
3. ... and help by model-based design
4. Lessons learned
   - Methodology
   - Architecture

Design: Hugo De Man (@Talk at 60th Anniversary of Manfred Glesner ...)

Software centric systems
(7th heaven?)



Application development

Application: usage, QoS requirements
Network: MAC, rouging
OS: power managent strategies
Middleware: scheduling ressources

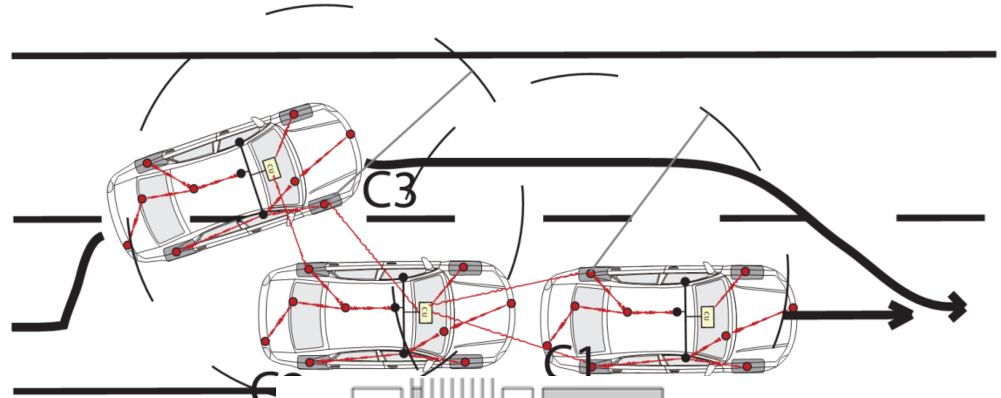
„Platform", fixed API

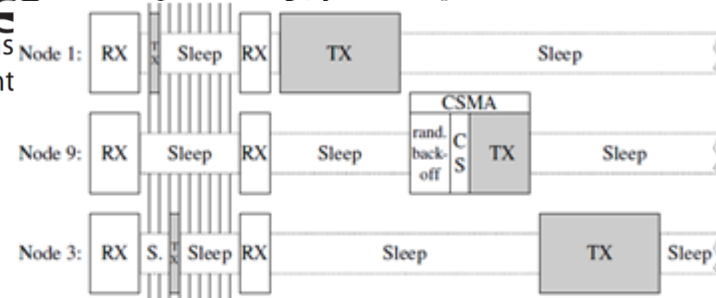
Architecture: power gating, DVFS, ...
Circuit: Adiabatic, Sub-threshold, ...
Technology: leakage power, capacities, ...

Circuit design

Hell of nano-scale physics

Example:
Advanced TPMS

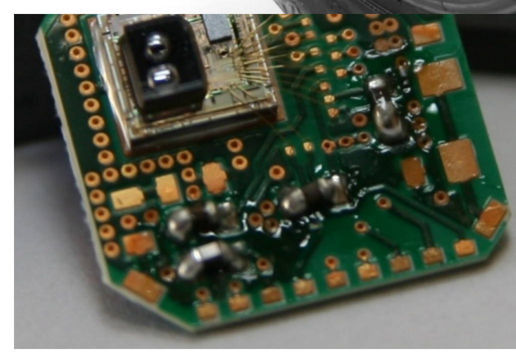




Usage of hardware defined by
- Scenario & Application
- Communication protocols
- Architecture

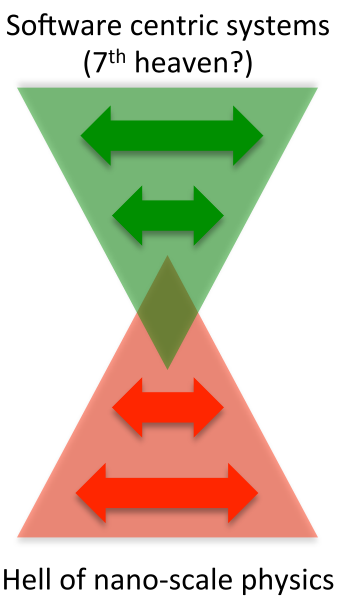
Energy management:
- Know application and scenarios
- Develop power management strategy
- Match with RT-Level infrastructure
- Match with technology

Power consumed in hardware,
Battery for days.



Challenge 1:
Power consumption *vertically, EDA horizontally*

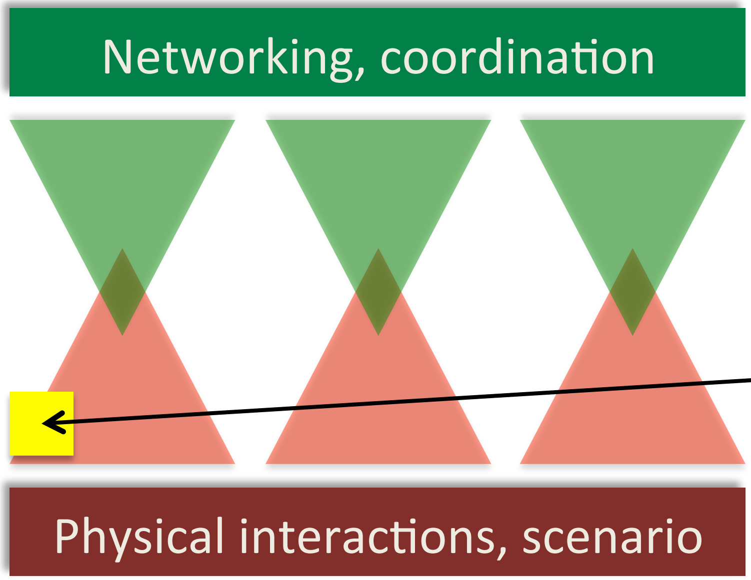
Design today
mostly horizontal



Needed for
Power/energy aware design:

Application: usage, QoS requirements
Network: MAC, rouging
OS: power managent strategies
Middleware: scheduling ressources
Architecture: power gating, DVFS, ...
Circuit: Adiabatic, Sub-threshold, ...
Technology: leakage power, capacities, ...

Challenge 2:
What is the cause of power consumption?



„Due to command to do X from network“

„The software running on the processor“

„The processor/transceiver/...“!

„Due to the physical scenario Y“

Can EDA help?

Short answer:

NO.

Unless you put all this in one formal model to enable overall system optimization!

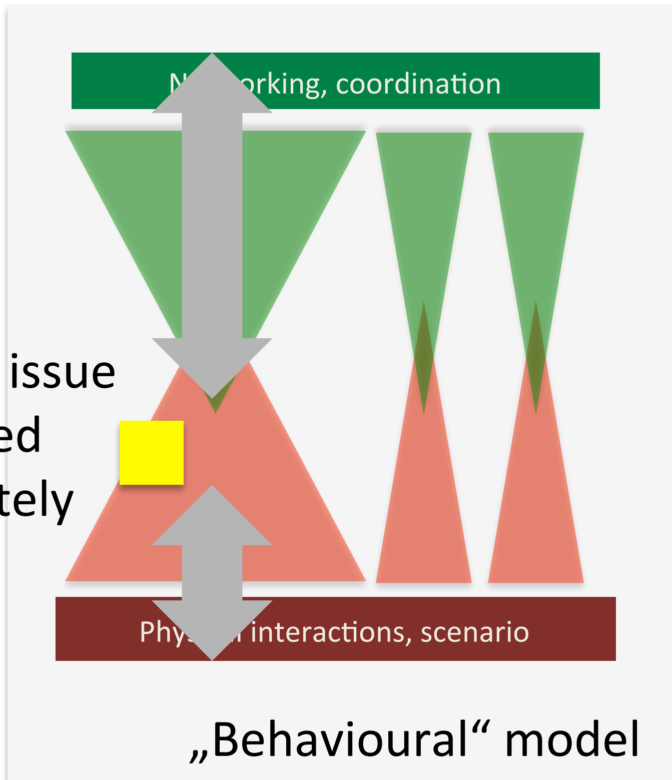
Application: usage, QoS requirements
Network: MAC, rouging
OS: power managent strategies
Middleware: scheduling ressources
Architecture: power gating, DVFS, ...
Circuit: Adiabatic, Sub-threshold, ...
Technology: leakage power, capacities, ...

But: modelling/simulation is first step!

Design of Energy-Aware Cyber-Physical Systems

1. Why Energy/Power-Awareness?
2. Challenges ...
3. ... and help by model-based design
4. Lessons learned
   - Methodology
   - Architecture

Model-based Approach, Concept

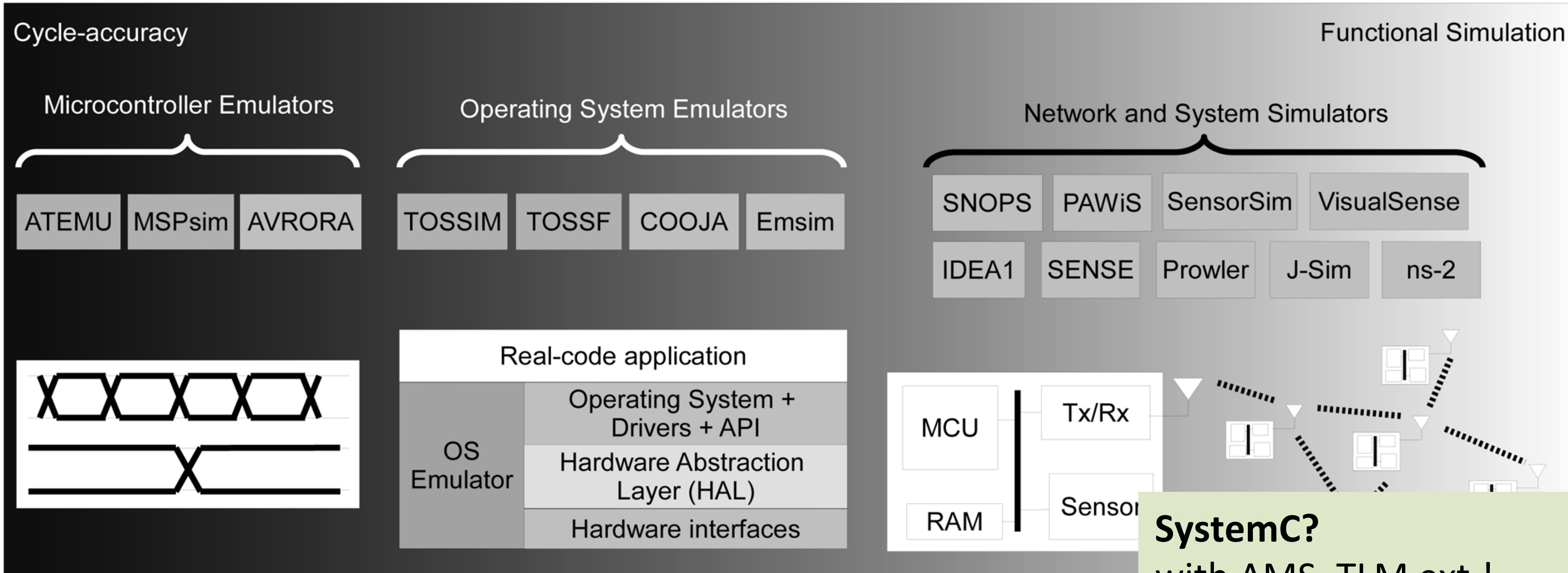


Design issue modeled accurately

Application: usage, QoS requirements
Network: MAC, rouging
OS: power managent strategies
Middleware: scheduling ressources

Architecture: power gating, DVFS, ...
Circuit: Adiabatic, Sub-threshold, ...
Technology: leakage power, capacities, ...

Model-Based Approach [Haase 2012]

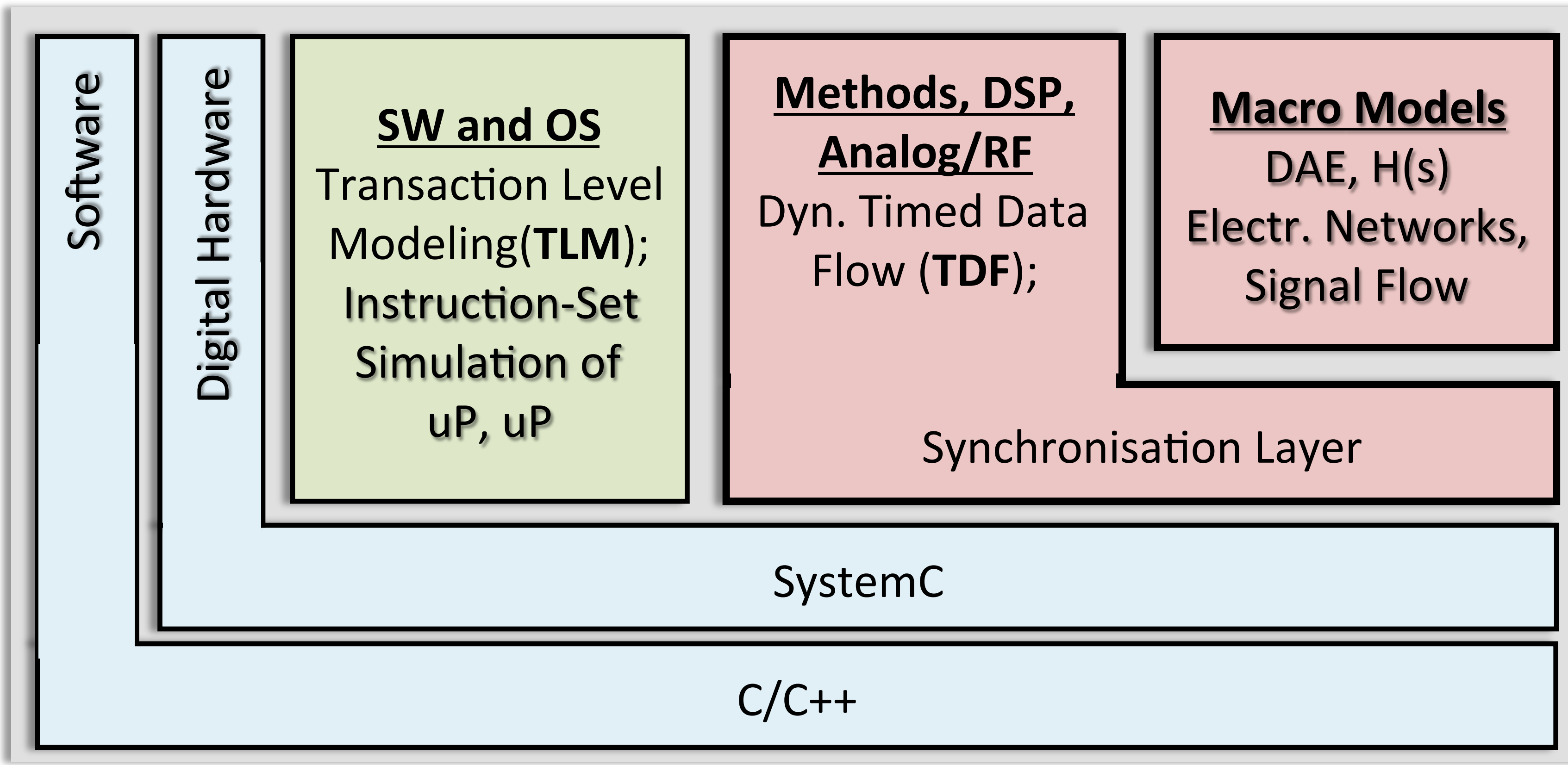


SystemC?
with AMS, TLM ext.!

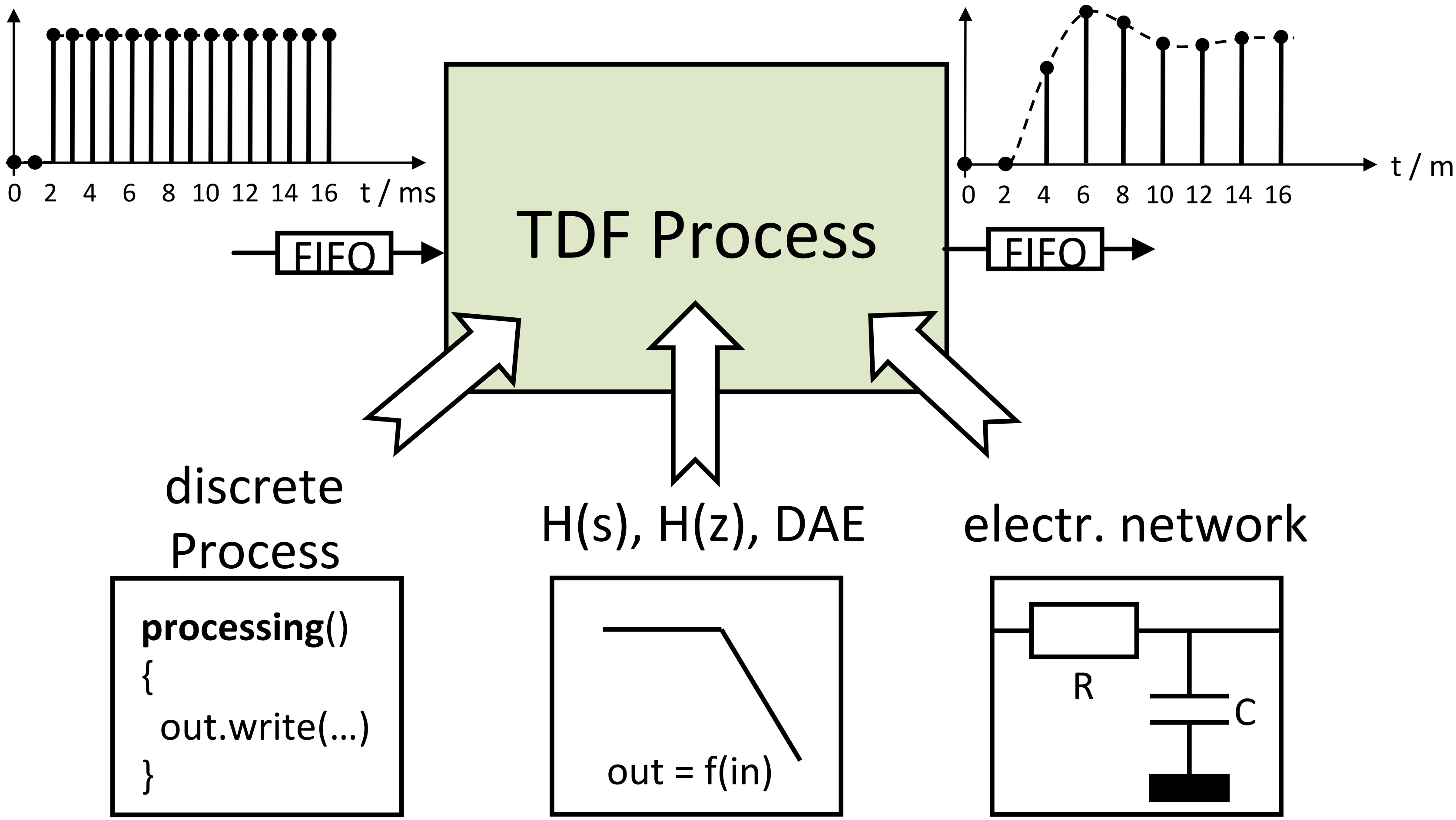
+ **Means/tools** to
  – Estimate power at verious levels of abstraction
  – Trace power consumption to its causes

e.g.:
SYCYPHOS
(SNOPS, SmartCoDe, ANDRES)

SystemC + TLM + AMS extensions!



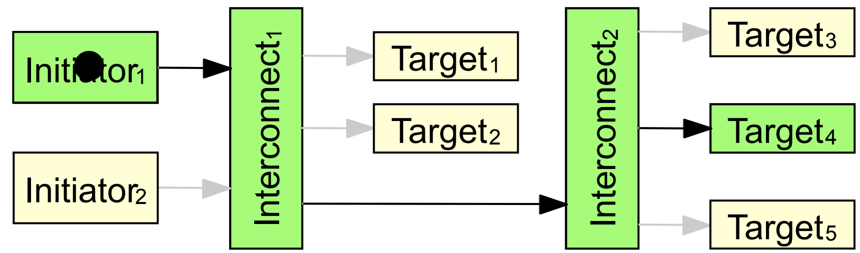
SystemC AMS, Modelling AMS, RF, Physical systems



Modelling Communication with TLM

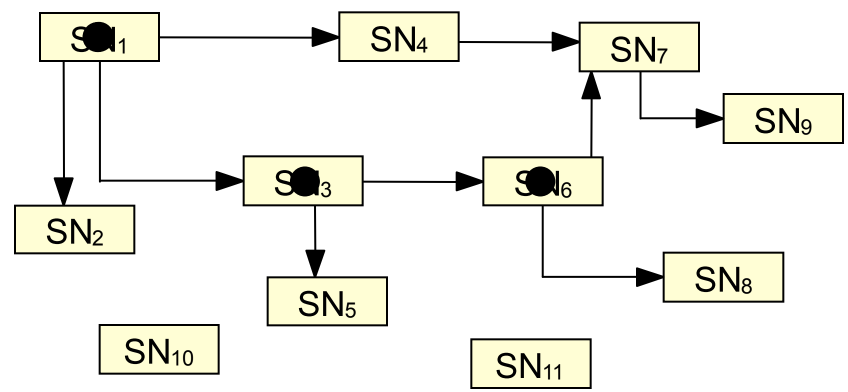
TLM 2.0

- Models communication via buses
- Abstracts data granularity ("payload"), timing accuracy



Wireless TLM

- Route of packet in a WSN: forks, dead ends, …
- Modeling "air": reflections, obstacles, etc. for wireless transmissions

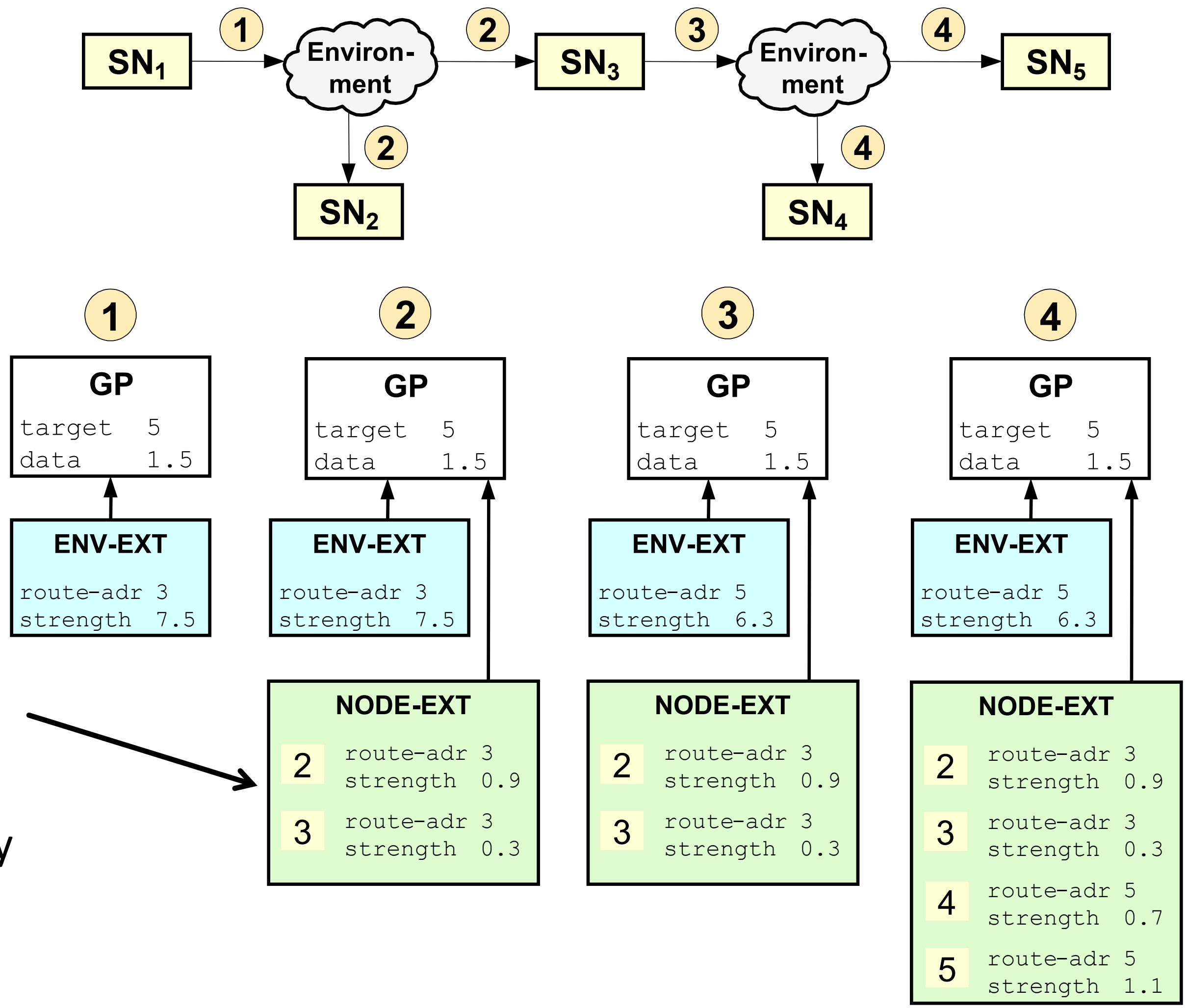


WSN extensions for the TLM 2.0 generic payload [Damm 2009, 2010]

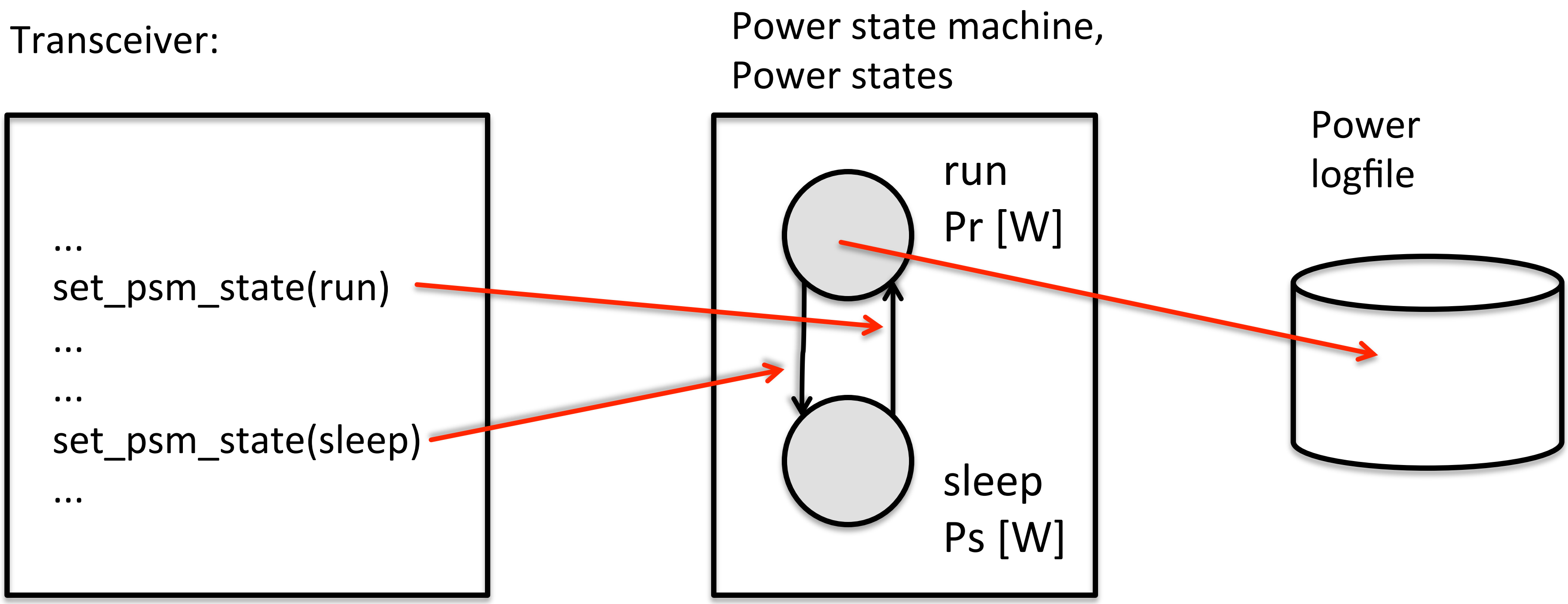
Packet sent:
Updated by node before it passes transaction to environment.

Packet from „Air“
Updated by environment before it passes transaction to nodes

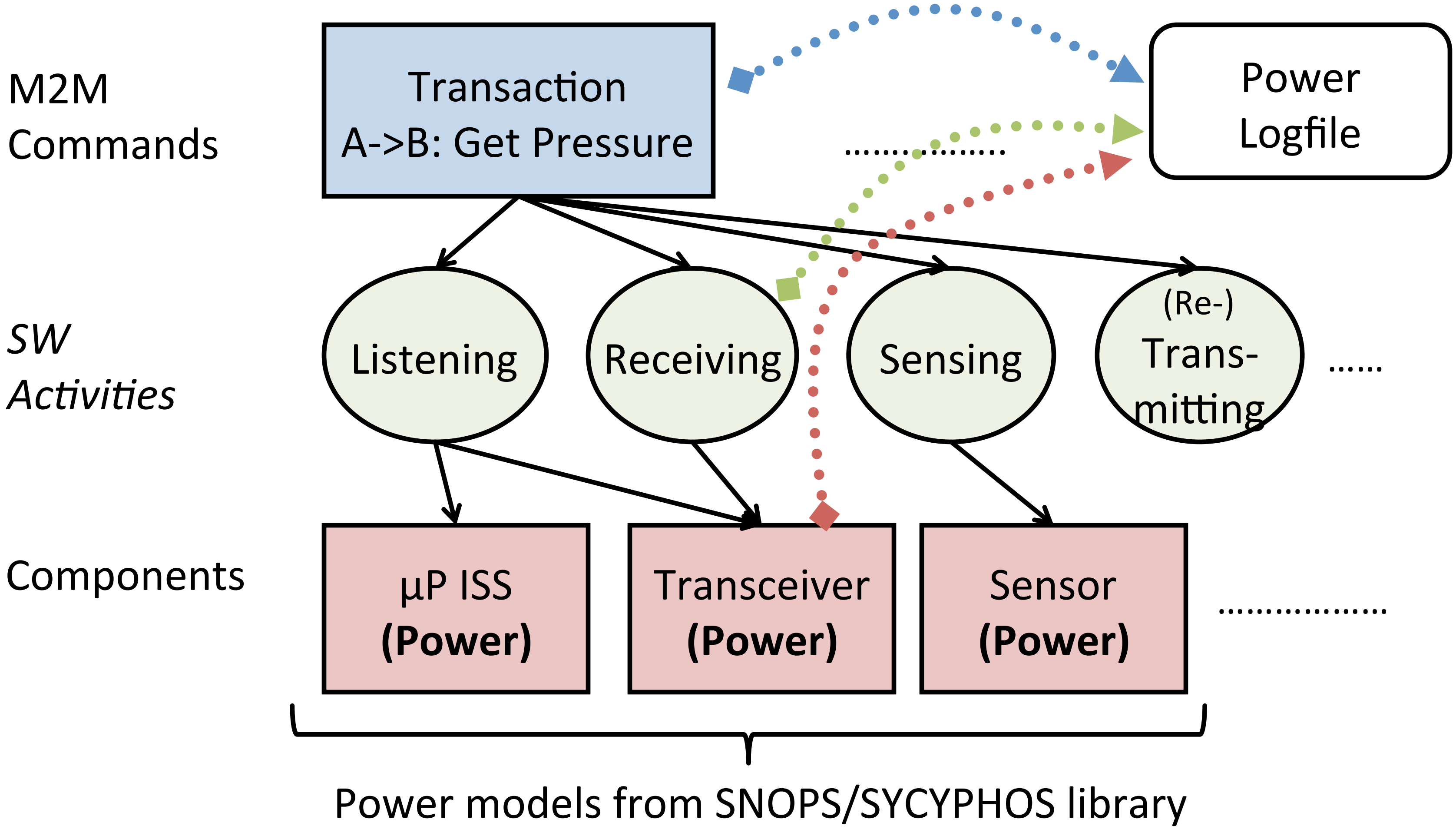
- received signal quality
- routing
- power used for task



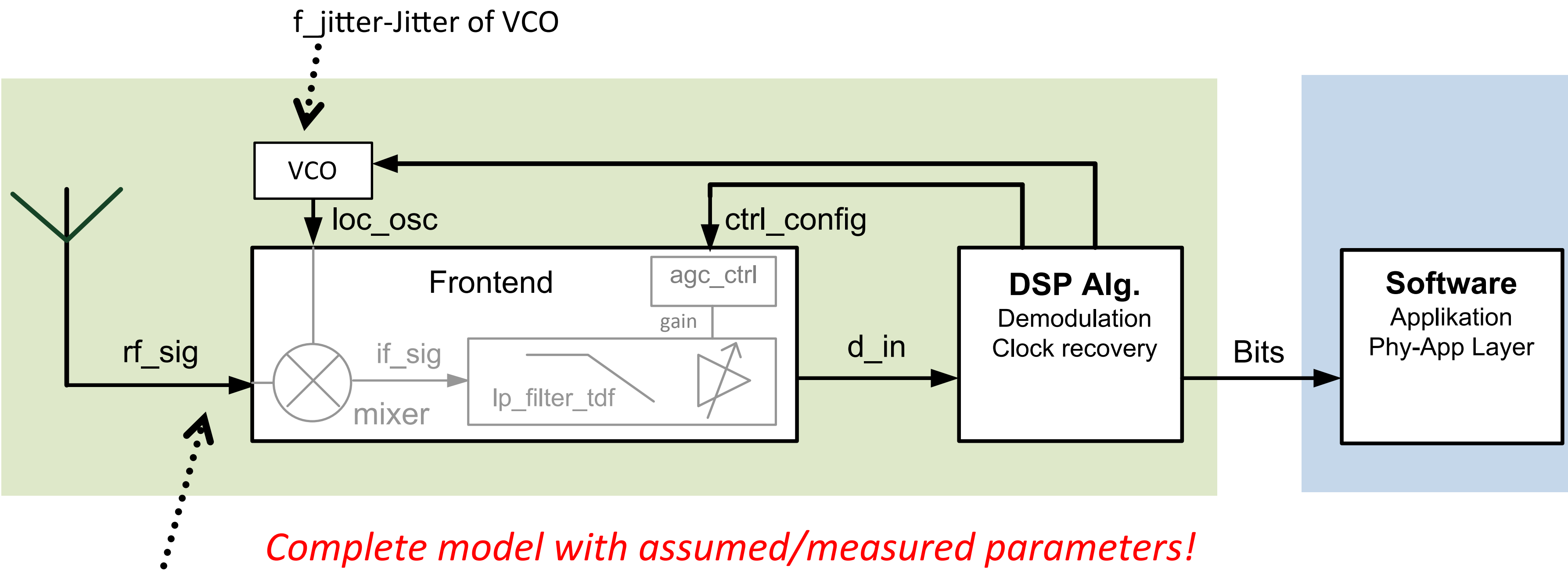
Power Profiling (1)



Power Profiling [Haase 2011]



Architecture Exploration: Non-ideal Behavior

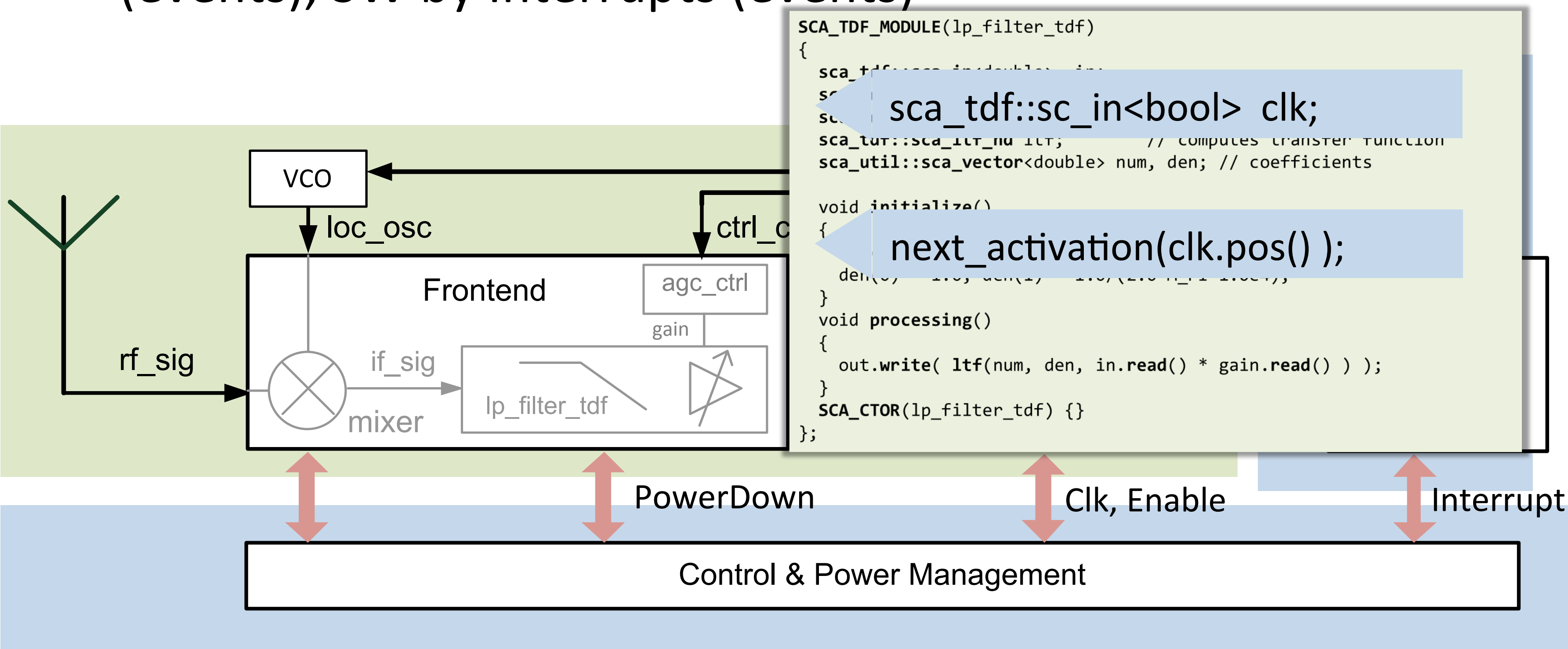


Complete model with assumed/measured parameters!

Parameter	Type	Default value	Description
n	sc_module_name	-	
_gain	double	-	gain in dB
_ip3	double	-	IP3 in dBm
_ideal	bool	-	true for simulation of ideal LNA, otherwise false

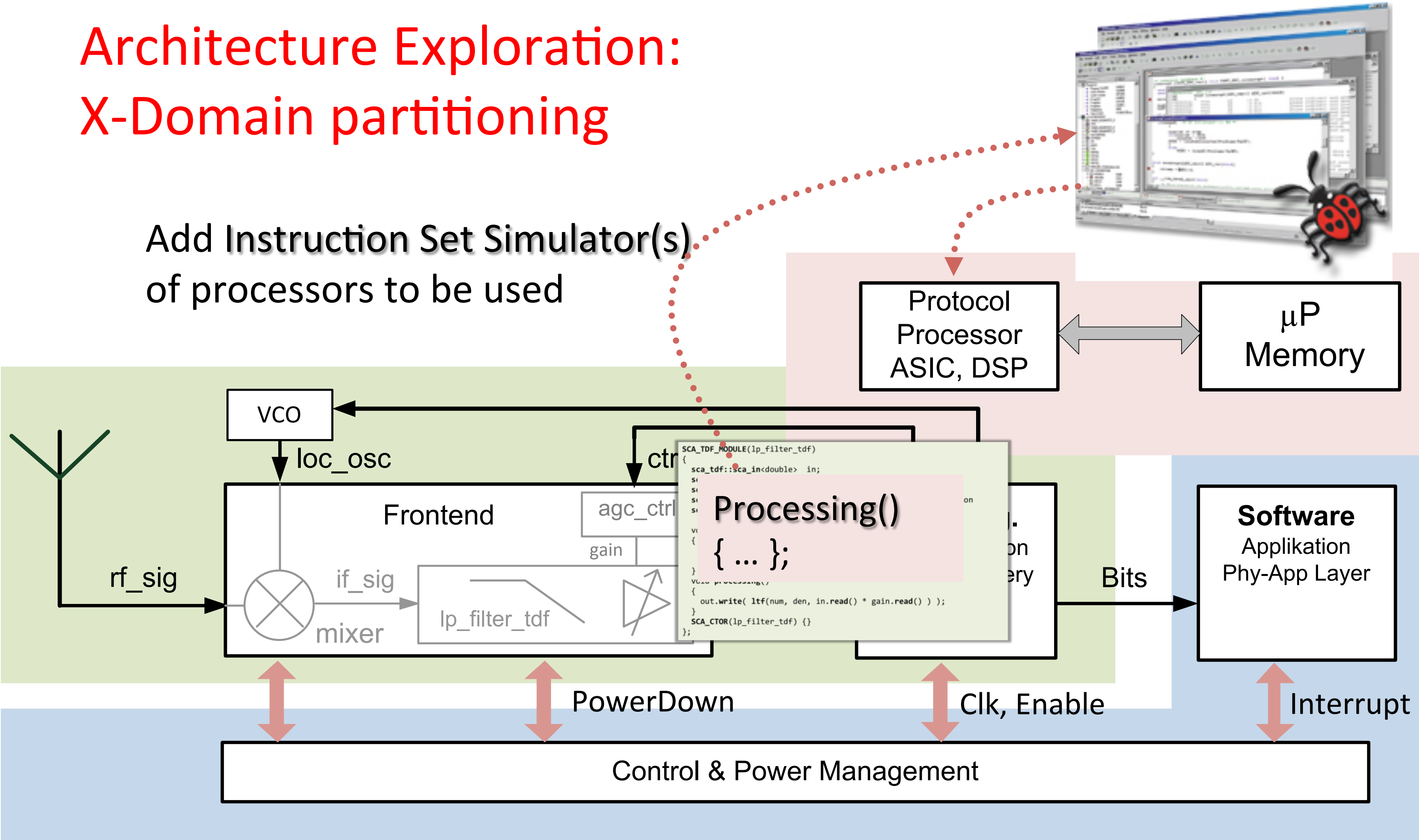
Architecture Exploration: Power Management

Execution of TDF processes controlled by clk/enable signals (events), SW by Interrupts (events)

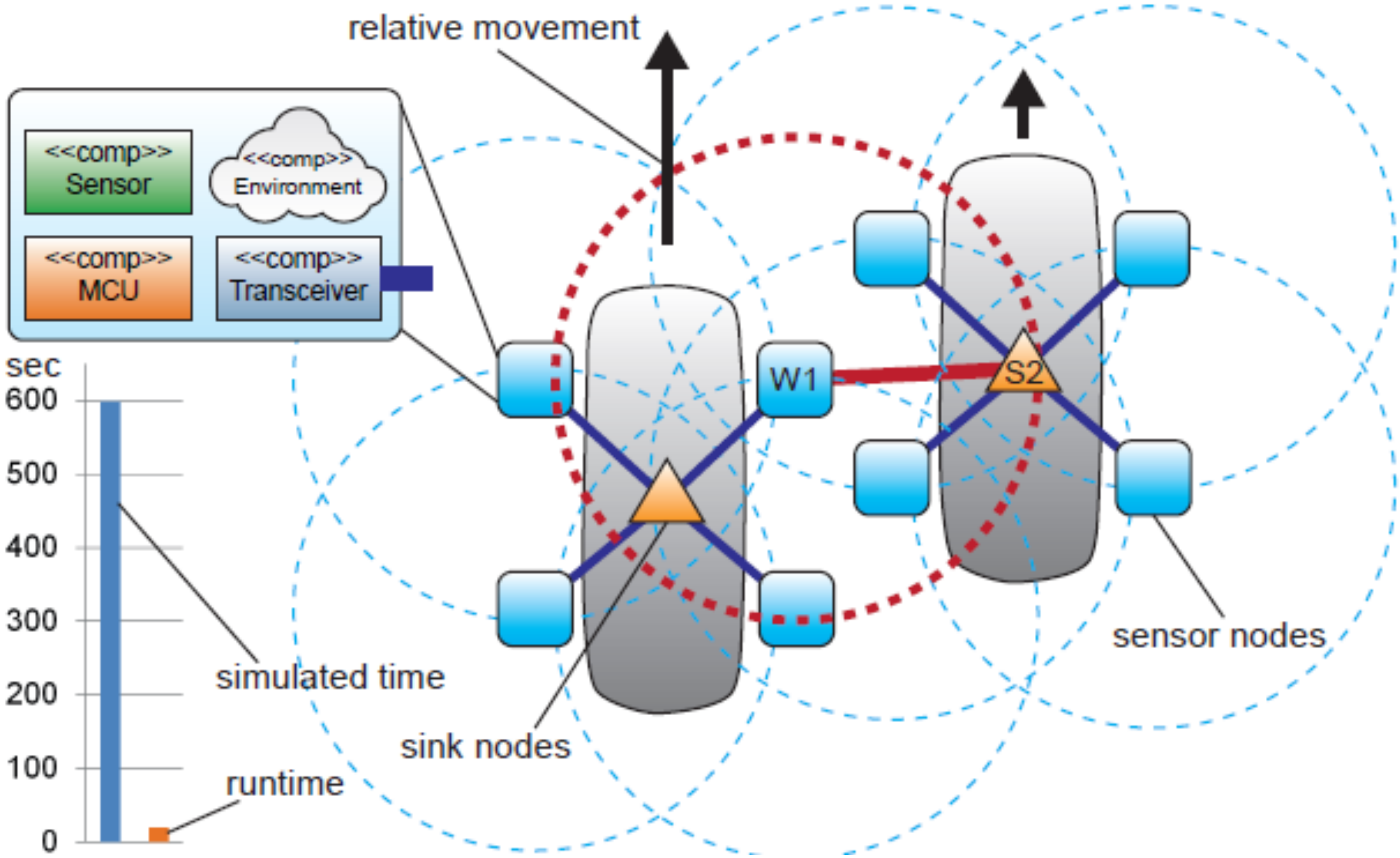


Architecture Exploration:
X-Domain partitioning

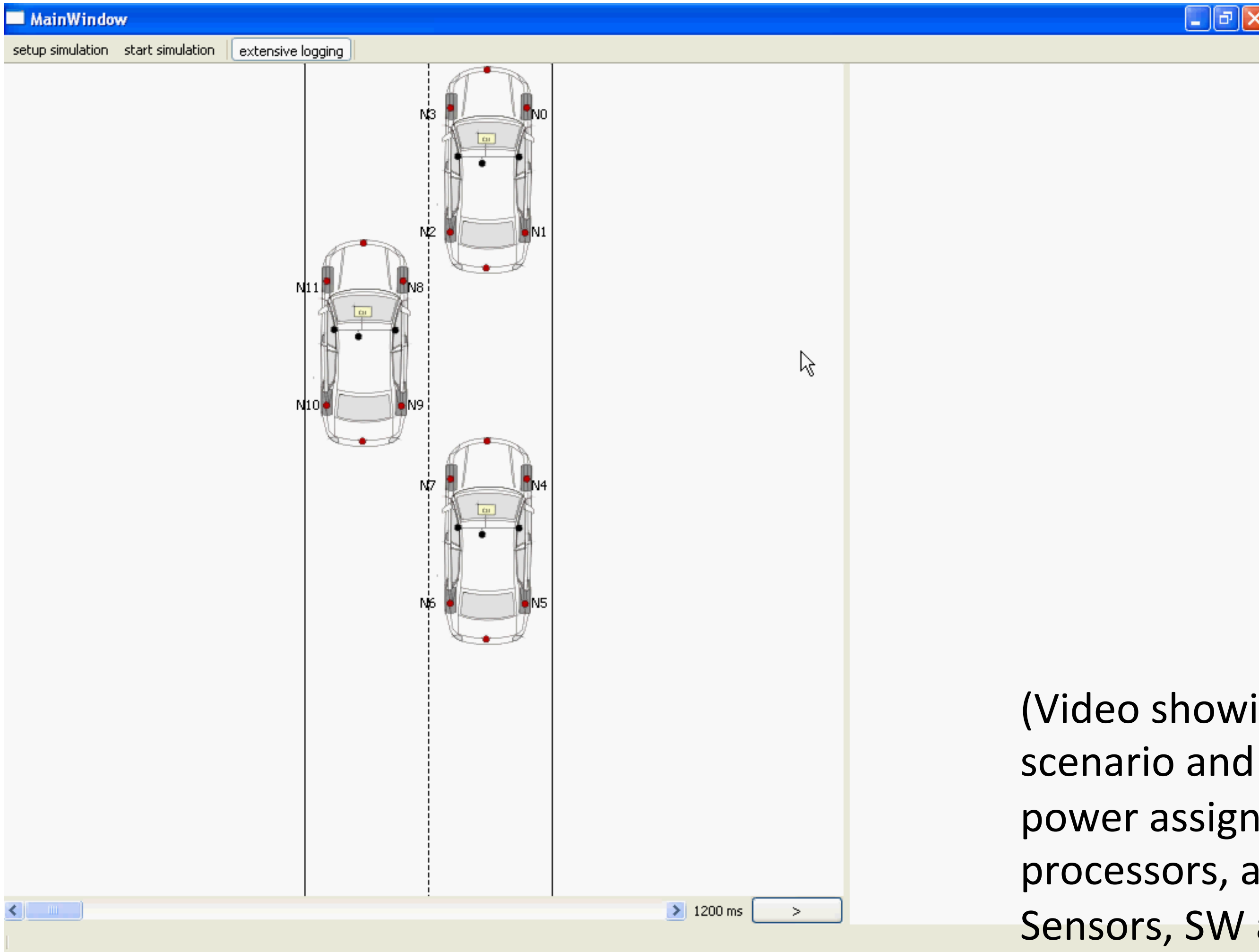
Add Instruction Set Simulator(s) of processors to be used



Example: Power profiling of TPMS with In-Car WSN; 18 8-Bit-uC with Firmware + Transceiver + Sensors



Example: Power profiling of TPMS with In-Car WSN; 18 8-Bit-uC with Firmware + Transceiver + Sensors



(Video showing Driving scenario and estimated power assigned to processors, analog/RF, Sensors, SW activities, Transactions ...)

Design of Energy-Aware Cyber-Physical Systems

1. Why Energy/Power-Awareness?
2. Challenges ...
3. ... and help by model-based design
4. Lessons learned
   - Methodology
   - Architecture

Lessons learned (Methodology)

Key for „low power/energy“:

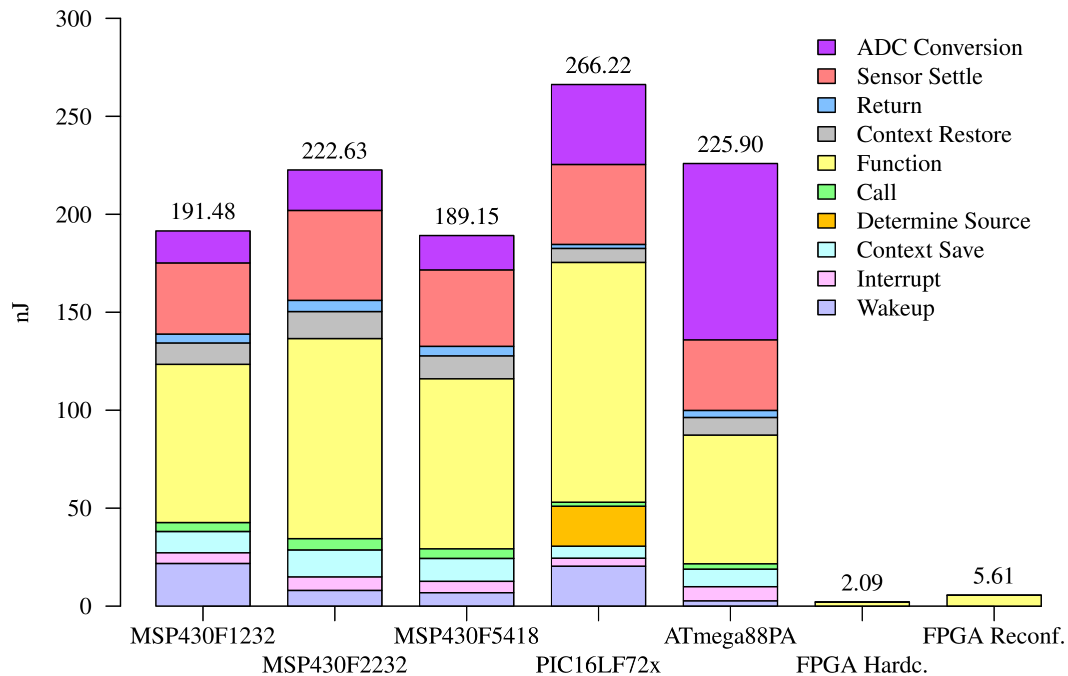
Sure all levels must be involved, but 2 things very useful

1. **Very early power budgeting** and estimation using functional models
2. Granularity of **infrastructure** for **power gating** (RFTS) or regulating (DVFS, AVFS) is key
   - Bottom up: determines standby power
   - Top-down: determines duty cycles
   - Important: Times for entering / leaving power states
     - Power converters
     - Clock generation (e.g. PLL)

Lessons learned (Architecture)

uC spend (too) much power/time for waiting, administrating peripherals!

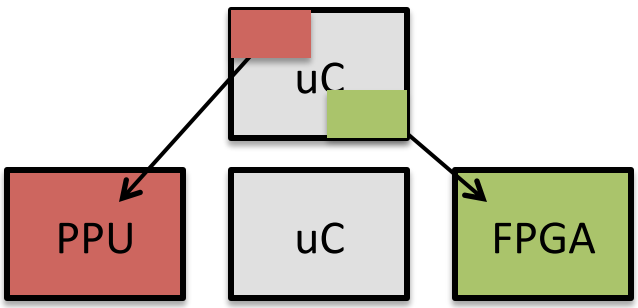
Benchmark developed:



Specifically optimized re-configurable ASIC: 200 -> **0.12 nJ [Glaser 2010]**

Lessons learned (Architecture)

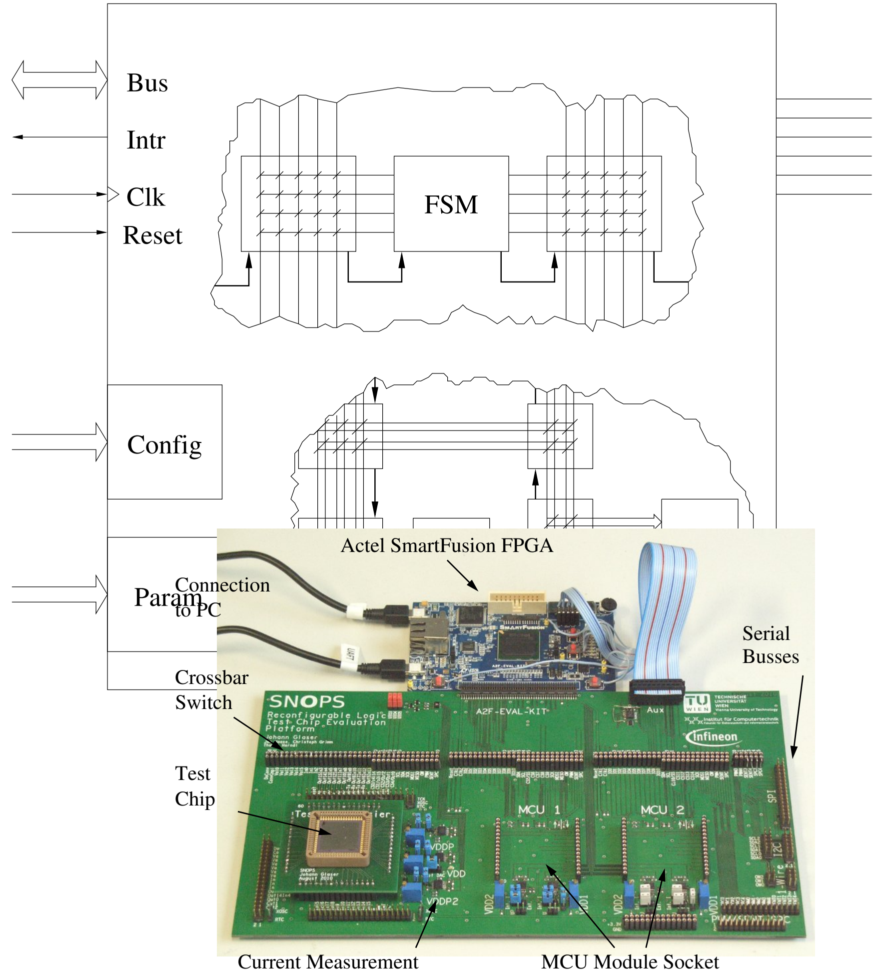
Don‘t wake processor for frequent, „simple“ tasks:



Use of

a) Simple, specific processor

b) Re-configurable system, optimized for specific task



Specifically optimized re-configurable ASIC: **0.12 nJ [Glaser 2010]**