The Connected IT world

7 trillion wireless devices in 2017, mobile traffic increase 60%/year until 2017

Source: J. Rabaey
Content

Shift from computation centric to data transfer and memory centric architectures
- Not only on large scale (IT World)
- But also on small scale (System-on-Chip)

Metrics for architecture efficiency
- Wireless baseband processing
- Impact of memories and data transfers on metrics
- Impact of application (communications) performance on metrics

3D Integration
- 3D memories and memory controllers

3.5G Digital Workload (100GOPS@1Watt)

Future: 1 TOPS in 1+ Watt

Source: Kees van Berkel, MPSoC2010
Baseband Receiver Structure

Mobile Phone Trends – Outer receiver

Source: Kees van Berkel, MPSoC2010
Recent Decoder Designs @ TU KL

- 160.8 Gbit/s LDPC Decoder
  65nm technology, 12mm²

- 2.15 Gbit/s LTE TC Decoder
  65nm technology, 7.7mm²

Music Baseband SDR Chip @ 65nm

12 Vektorprozessoren
~20 GOPs
~25 mio. gate equ.
~3.8 MB SRAM

Source: Infineon
LETI / TU KL Magali Chip

- 477mW NoC Based Digital Baseband for MIMO 4G SDR
- 96M transistors, 27mm², 65nm technology

22 processing units:
- 5 VLIW processors
- ARM11 processor
- ASIP processor
- HW accelerators
- Distributed memory
- 15 asynchronous NoC router
- Sophisticated power management

Metric – Energy Efficiency

Example - SODA, DSP and GP Architectures
Metric Assessment - Channel Decoders

All architectures based on standard synthesis flows, 65nm technology@worst case, all data in-house available

<table>
<thead>
<tr>
<th>Decoder</th>
<th>Flexibility</th>
<th>Max Block-size</th>
<th>Payload Throughput [Mbit/s]</th>
<th>Freq. [MHz]</th>
<th>Area [mm²]</th>
<th>Dynamic Power [mWatt]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIP (Magali)</td>
<td>Conv. Codes</td>
<td>N=16k</td>
<td>40 14/6 iter 38/6 iter</td>
<td>385 (P&amp;R)</td>
<td>0.7 (P&amp;R)</td>
<td>~100</td>
</tr>
<tr>
<td></td>
<td>Binary TC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Duo-binary TC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTE Turbo (Music)</td>
<td>LTE turbo code</td>
<td>N=18k</td>
<td>150 (6 iter)</td>
<td>300 (P&amp;R)</td>
<td>2.1 (P&amp;R)</td>
<td>~300</td>
</tr>
<tr>
<td>LDPC flex (Magali)</td>
<td>R=1/4 to</td>
<td>N=16k</td>
<td>150-300</td>
<td>385 (P&amp;R)</td>
<td>1.172 (P&amp;R)</td>
<td>~389</td>
</tr>
<tr>
<td></td>
<td>R=9/10</td>
<td></td>
<td>(20-10 iter)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDPC fixed (Magali)</td>
<td>R=3/4</td>
<td>N=1.2k</td>
<td>480 (6 iter)</td>
<td>435 (P&amp;R)</td>
<td>0.583 (P&amp;R)</td>
<td>~202</td>
</tr>
<tr>
<td>LDPC WiMedia 1.5</td>
<td>R=1/2-4/5</td>
<td>N=1.3k</td>
<td>640 (R=1/2,5 iter) 960</td>
<td>265</td>
<td>0.51</td>
<td>~193</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(R=3/4,5 iter)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CC Decoder</td>
<td>64-state NSC</td>
<td></td>
<td>500</td>
<td>500</td>
<td>0.1</td>
<td>~37</td>
</tr>
</tbody>
</table>

Algorithmic Throughput Calculations [Gops]

<table>
<thead>
<tr>
<th>Code</th>
<th>Operations per decoded information bit normalized to ~8bit addition</th>
<th>100Mbit/s</th>
<th>300Mbit/s</th>
<th>1 Gbit/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC: states=64</td>
<td>~200</td>
<td>~20</td>
<td>~60</td>
<td>~200</td>
</tr>
<tr>
<td>LDPC Min-Sum</td>
<td>5 iter 75/R</td>
<td>~7.5/R</td>
<td>~22.5/R</td>
<td>~75/R</td>
</tr>
<tr>
<td></td>
<td>10 iter 150/R</td>
<td>~15/R</td>
<td>~45/R</td>
<td>~150/R</td>
</tr>
<tr>
<td></td>
<td>20 iter 300/R</td>
<td>~30/R</td>
<td>~90/R</td>
<td>~300/R</td>
</tr>
<tr>
<td></td>
<td>40 iter 600/R</td>
<td>~60/R</td>
<td>~180/R</td>
<td>~600/R</td>
</tr>
<tr>
<td>LDPC Min-Sum</td>
<td>(x3.4 for λ-3-Min alg.)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 iter 280</td>
<td>~28</td>
<td>~84</td>
<td>~280</td>
</tr>
<tr>
<td></td>
<td>4 iter 560</td>
<td>~56</td>
<td>~168</td>
<td>~560</td>
</tr>
<tr>
<td></td>
<td>6 iter 840</td>
<td>~84</td>
<td>~252</td>
<td>~840</td>
</tr>
</tbody>
</table>
Area- and Energy Efficiency

What about Memory/Data Transfers

Current metric: energy efficiency = only operations/energy
Data transfers/accesses substantially contribute to the power consumption

Example (R=0.5)
150 Mbit/s Turbo: ~126 Gops ~40 Gaccesses
150 Mbit/s LDPC: ~90 Gops ~80 Gaccesses

Efficient data transfer is key for efficient implementation
- LTE TC: special interleaver structure to avoid access conflicts
- DVB-S2/WiMAX LDPC: special code structure to minimize access conflicts

Efficiency metrics based on operations only are not appropriate
- Power includes operations and accesses!
- Architectures are favored where operations dominate compared to accesses
Communications Performance

Overall efficiency of a baseband receiver depends on
- Implementation performance
- Communications performance
- Flexibility

Comparison of two iterative decoders with same communications performance but different parameters (codes, code rate, iterations)
⇒ impact on implementation efficiency
**Fixed Communication Performance**

Blocksize 6145 information bits, TC: 150Mbit/s @6.5 iterations

**Implementation Efficiency**

TC efficiency constant for all code rates, 6.5 iter
- R=4/5, 10 iter
- R=1/2, 20 iter
- R=1/3, 40 iter

TC LTE
- flexible LDPC
Lessons learned

- Understanding trade-offs between implementation efficiency, application performance and flexibility requirements is mandatory for efficient baseband receivers.

- Operation based metrics for energy and area efficiency can be misleading.

- Memory and data transfers have to be considered in metrics for design space exploration.

- Implementation efficiency metrics have to be linked to application performance.

Next-Generation Mobile Platform Traffic

- Traditional JEDEC DRAM channels are saturating.
Next Generation Teraflop Computing Platform

Year 2018
8nm Core, 10Gflop

400mm² Die size
1150 Cores

1 TF, ~ 100 W

Aggressive voltage scaling
Efficient signaling
Hierarchical heterogeneous topologies

Source: Intel

Energy-Efficient Seismic Modeling

Reverse Time Migration (RTM) Method

- Exploration area: 30km x 20km area, 10km depth
- Exploration ship: 10 streamer lines with 1000 receivers each, time sampling interval of 1ms and listening a total of 12 seconds each
- Reaching a computation time of on week
  - >1M cores necessary with 38MW power!
- Green Wave Computer (45nm): 2D torus NoC based, 76,000 optimized Tensilica LX2 cores
  - 5 MW power
3D Integration with TSVs

Through Silicon Vias (TSV)
- Polysilicon filled (FEOL)
  - 10,000 TSV/mm²
- Copper filled (BEOL)
  - 500 TSV/mm²

Wide IO Technology (JEDEC Standard 2012)

Channel
- 4 banks with 64Mb each
- 128 bit @ 200MHz SDR
- 3.2GBps

Memory
- 4 channels
- 1Gb
- 512 bit IO
- 12.8GBps
### 3D Magali Chip

- 65nm tech, 72mm$^2$, 1980 TSVs for 3D NoC, 1250 TSV for wide I/O memory
- Heater, temperature sensors

![Diagram of 3D Magali Chip](source: LETI)

### Power Savings in DRAM Memory Interfaces

- Much wider I/Os possible >> 32 bits

<table>
<thead>
<tr>
<th>Memory link, peak bandwidth and power consumption efficiency</th>
<th>Cost for 1TBps memory bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>![Diagram of Memory Link](source: LETI)</td>
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<table>
<thead>
<tr>
<th>Component</th>
<th>Memory Capability</th>
<th>Bandwidth</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-core</td>
<td>Memory capability</td>
<td>8.5 GBps 30 mW/Gbps</td>
<td>3800 240 W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.3 GBps 20 mW/Gbps</td>
<td>7700 160 W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.8 GBps 4 mW/Gbps</td>
<td>41000 32 W</td>
</tr>
</tbody>
</table>

Source: LETI
3D-stacked DRAMs

DRAM macro cut out of a 8 bank 1Gb DDR2 SDRAM chip:

Common logic can either be placed on a separate die or on each DRAM layer.

Organization and Naming

A single 3D-layer consists of 3D-DRAM banks
A bank is composed of DRAM core tiles

Tile: basic memory macro cut out of a commodity DRAM
Single 3D-layer Design Space

1x 128Mb with 64 I/Os

2x 64Mb with 128 I/Os

4x 32Mb with 256 I/Os

8x 16Mb with 512 I/Os

Control / Voltage generators / Signaling

TSV area: I/Os and Power

Comparison 2Gb (8 layers/8 banks)

Comparison to Micron’s Hybrid Memory Cube (HMC)
- Our 3D-DRAM is more than competitive

64Mb 64Mb

64Mb 64Mb

128 I/Os 256 I/Os

8 layers ⇒ 2Gb/channel

HMC
Multi-Channel 3D-DRAM Controller

Different request granularities
- But normally fixed to 128 bit (Wide IO JEDEC Standard)

Three types of I/O accesses possible from 32-bit to 128-bit

Fine-grained 3D-DRAM Access

On the fly switching of the data width: 32, 64, 128

- 128bit: Native – 16 CSLs – 2 Wordlines
- 64bit: 8 CSLs + 1 Wordline
- 32bit: 4 CSLs + 1 Wordline
Flexible 3D-DRAM Access

Burst Length (BL) on the fly switching
- BL can be switched on the fly (no Mode Register Set)

Combining BL and data width on the fly switching
- Additional signals needed between 3D Channel Controller and 3D-DRAM

Single 3D-DRAM access size range: 8..128 Bytes

8 Bytes (BL=2 * 32 I/Os) ➔ 128 Bytes (BL=8 * 128 I/Os)

Results

Investigated different configurations
- #Layers
- Organisation of layers
- Technologies
Investigated 3D-DRAM Configurations

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<thead>
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<tbody>
<tr>
<td><strong>256</strong></td>
<td>1 x [4x64Mb]</td>
<td>4</td>
<td>58</td>
<td>6f^2</td>
<td>16</td>
<td>200</td>
</tr>
<tr>
<td>512</td>
<td>2 x [4x64Mb]</td>
<td>4</td>
<td>58</td>
<td>6f^2</td>
<td>26</td>
<td>200</td>
</tr>
<tr>
<td>1024</td>
<td>8 x [2x64Mb]</td>
<td>8</td>
<td>46</td>
<td>6f^2</td>
<td>35</td>
<td>300</td>
</tr>
<tr>
<td>*2048</td>
<td>8 x [2x128Mb]</td>
<td>8</td>
<td>46</td>
<td>6f^2</td>
<td>60</td>
<td>167</td>
</tr>
<tr>
<td>4096</td>
<td>8 x [4x128Mb]</td>
<td>8</td>
<td>45</td>
<td>4f^2</td>
<td>97</td>
<td>200</td>
</tr>
</tbody>
</table>

**SDR x128**

<table>
<thead>
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<td>300</td>
</tr>
<tr>
<td>4096</td>
<td>8 x [4x128Mb]</td>
<td>8</td>
<td>45</td>
<td>4f^2</td>
<td>98</td>
<td>200</td>
</tr>
</tbody>
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**DDR x128**

**Density emulates the published Samsung 1Gb WIDE IO chip [17].**

Simulation Set-Up

Emulation of workload via 3 traffic generators

- Traffic A – Cache misses of a 2 core ARM ~ 100 MB/s per core
- Traffic B – DMA accesses in a SoC (Imaging) ~ 0.8 GB/s
- Traffic C – HD Video DMA accesses ~ 1.5 GB/s
Results with BL and Data Width Switching

Factor 3x energy improvement of 2Gbit 3D compared to 2Gbit LPDDR2 (PageHitRate=50%)

Outlook: Multichannel DRAM Controller

Different access granularities ➔ highly fragmented data accesses

- Port 0: 16 Bytes
- Port 1: 32 Bytes
- Port 2: 64 Bytes
- Port 3: 128 Bytes

Intelligent X-bar switch

Decides where to schedule incoming request

MPSoc address space ➔ physical DRAM address space

Trade-off: Bandwidth/Latency vs. Energy
Thank you for attention!
For more information please visit

http://ems.eit.uni-kl.de

On Complexity, Energy- and Implementation Efficiency of Channel Decoders
F. Kienle, N. Wehn, H. Meyr. IEEE Transactions on Communications,
Vol. 59, Nr. 12, pages 3301 – 3310, December 2011, New York

Exploration and Optimization of 3-D Integrated DRAM Subsystems