An efficient on-chip configuration infrastructure for a flexible multi-ASIP turbo decoder architecture

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8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip

Agenda

- Context
- UDec Architecture & Configuration
- Configuration infrastructure
- Implementation results
- Conclusions

A connected world

DVB Digital Video Broadcasting

Wi Fi

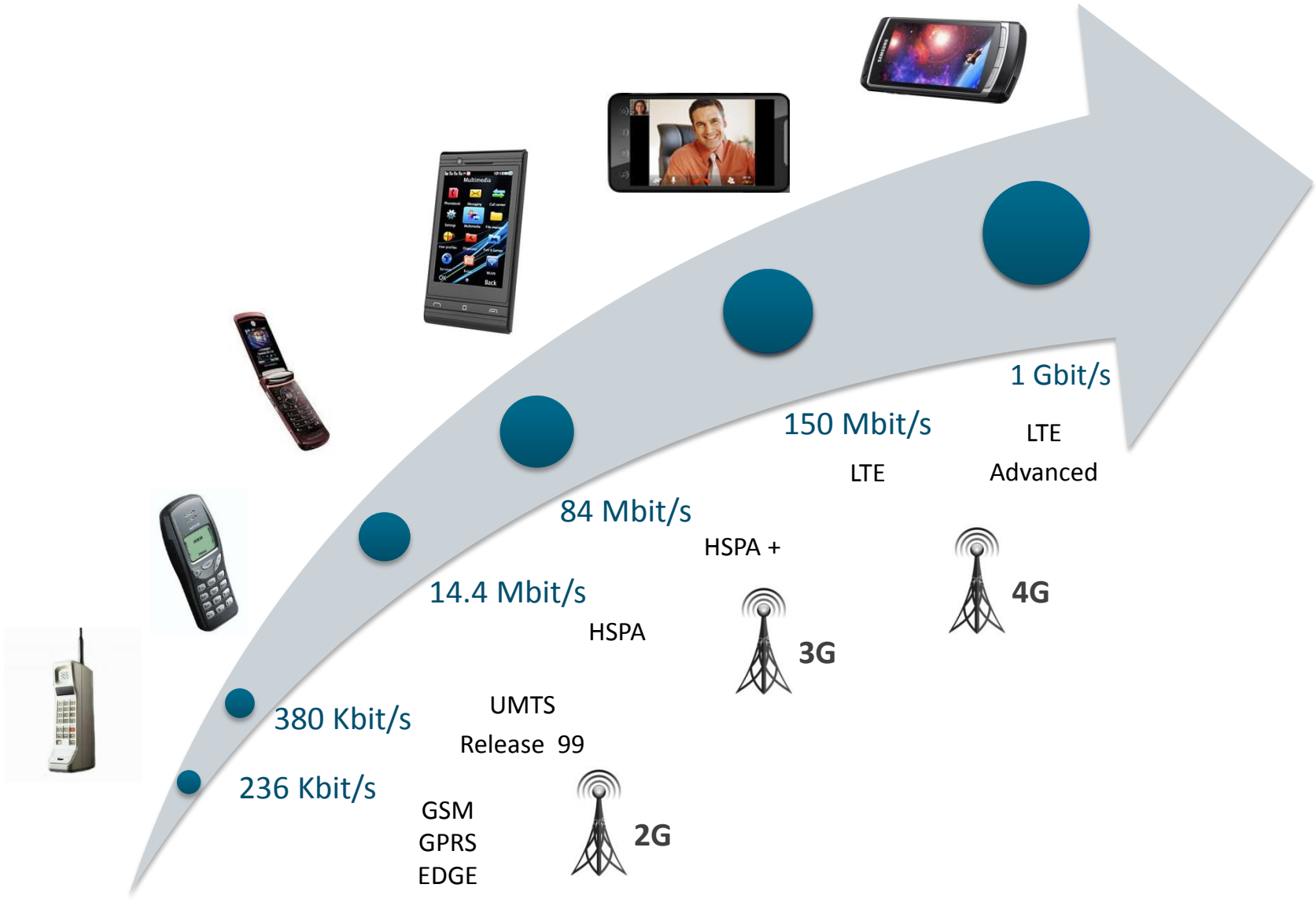
HSPA. MOBILE BROADBAND TODAY

wimax

Bluetooth®

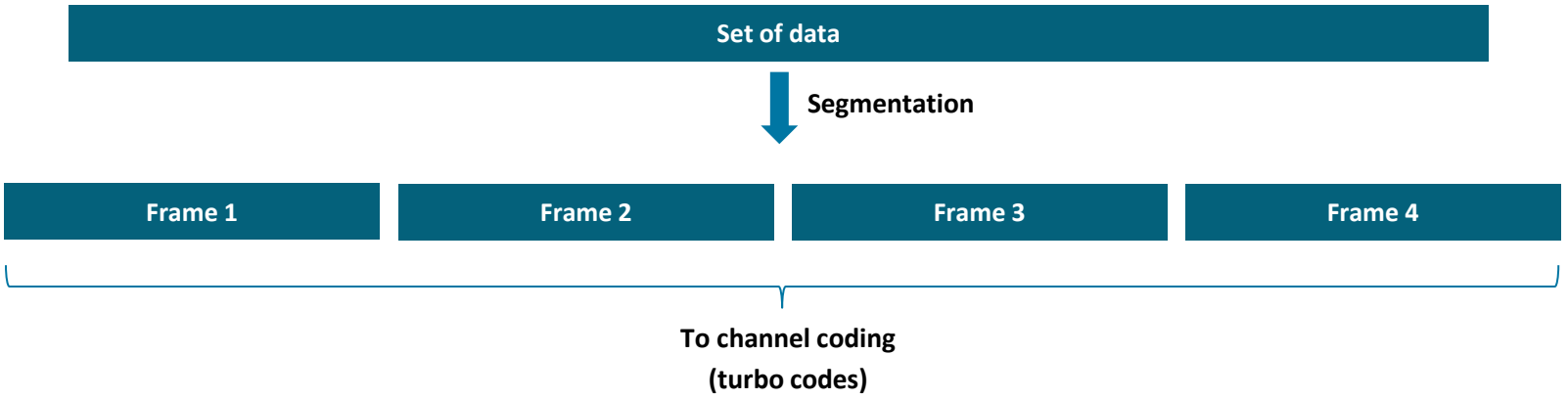
Lte™

Throughput evolution



Configuration & frame duration

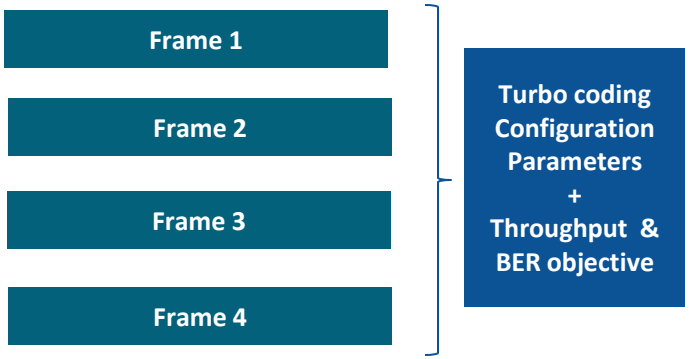
@transmitter side:

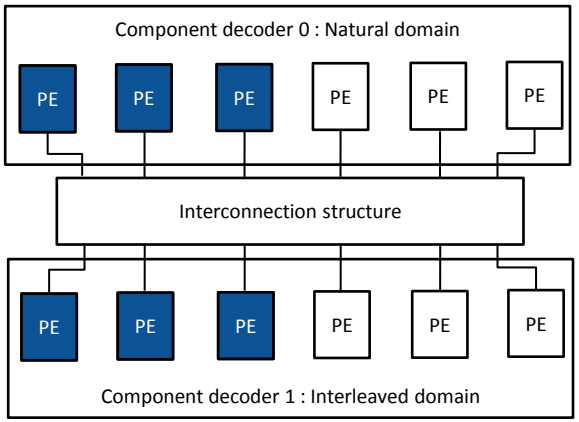


- Turbo coding configuration parameters
  - SBTC or DBTC
  - Code rate
  - Frame size
  - Interleaving law
  - …

Configuration & frame duration

@receiver side:

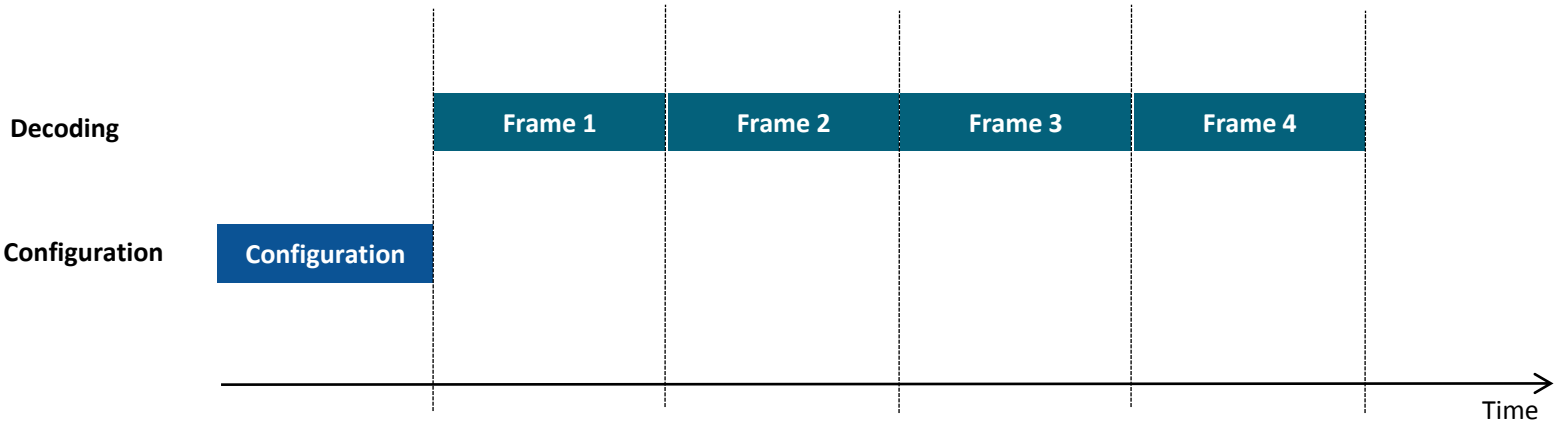


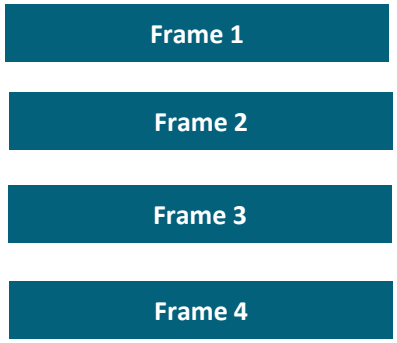


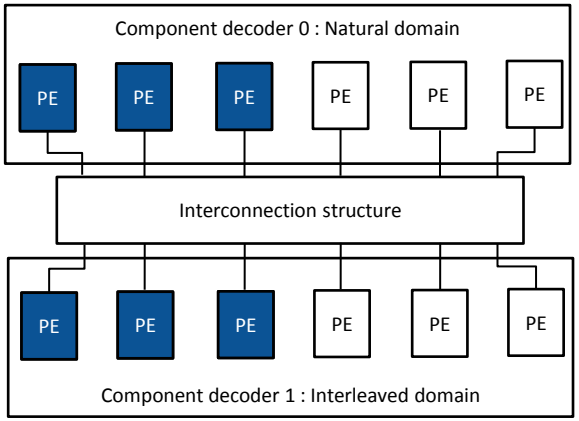
Multiprocessor Turbo decoder architecture

Configuration & frame duration

@receiver side:



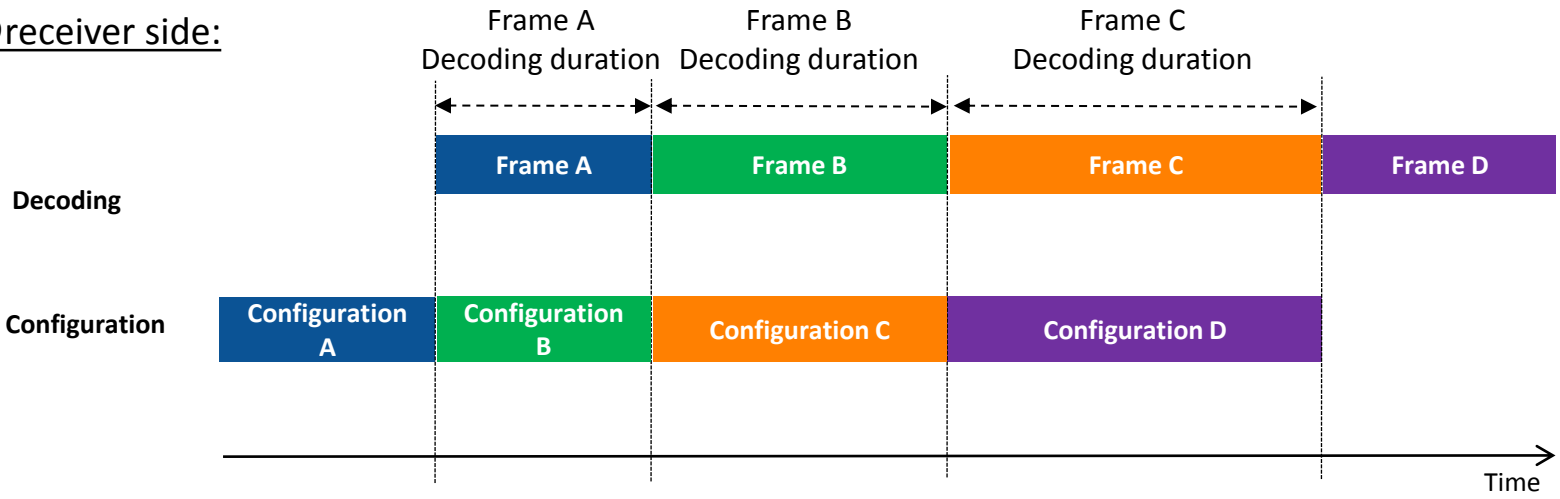


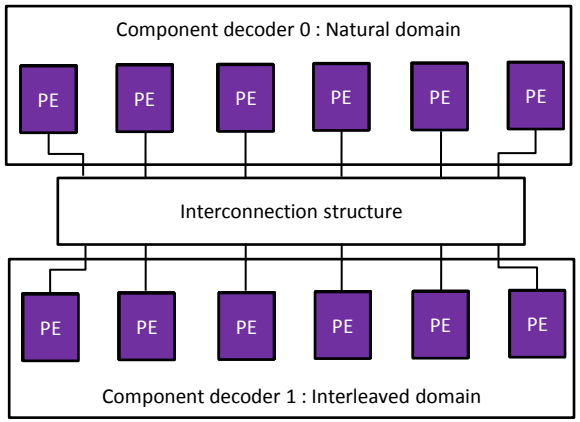


Multiprocessor Turbo decoder architecture

Configuration & frame duration

@receiver side:

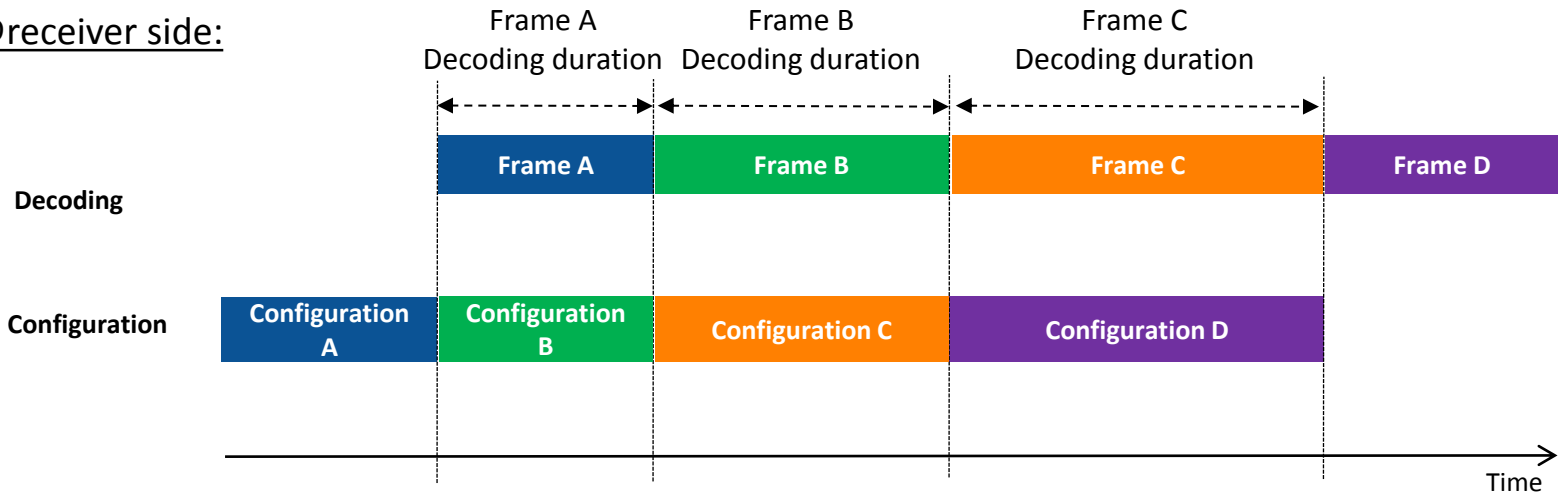




Multiprocessor Turbo decoder architecture

Configuration & frame duration

@receiver side:



$$\text{Configuration Duration} = \text{Current frame decoding duration} = \frac{\text{Frame size (bits)}}{\text{Throughput (Bits/s)}}$$

Configuration Duration ≈ µs

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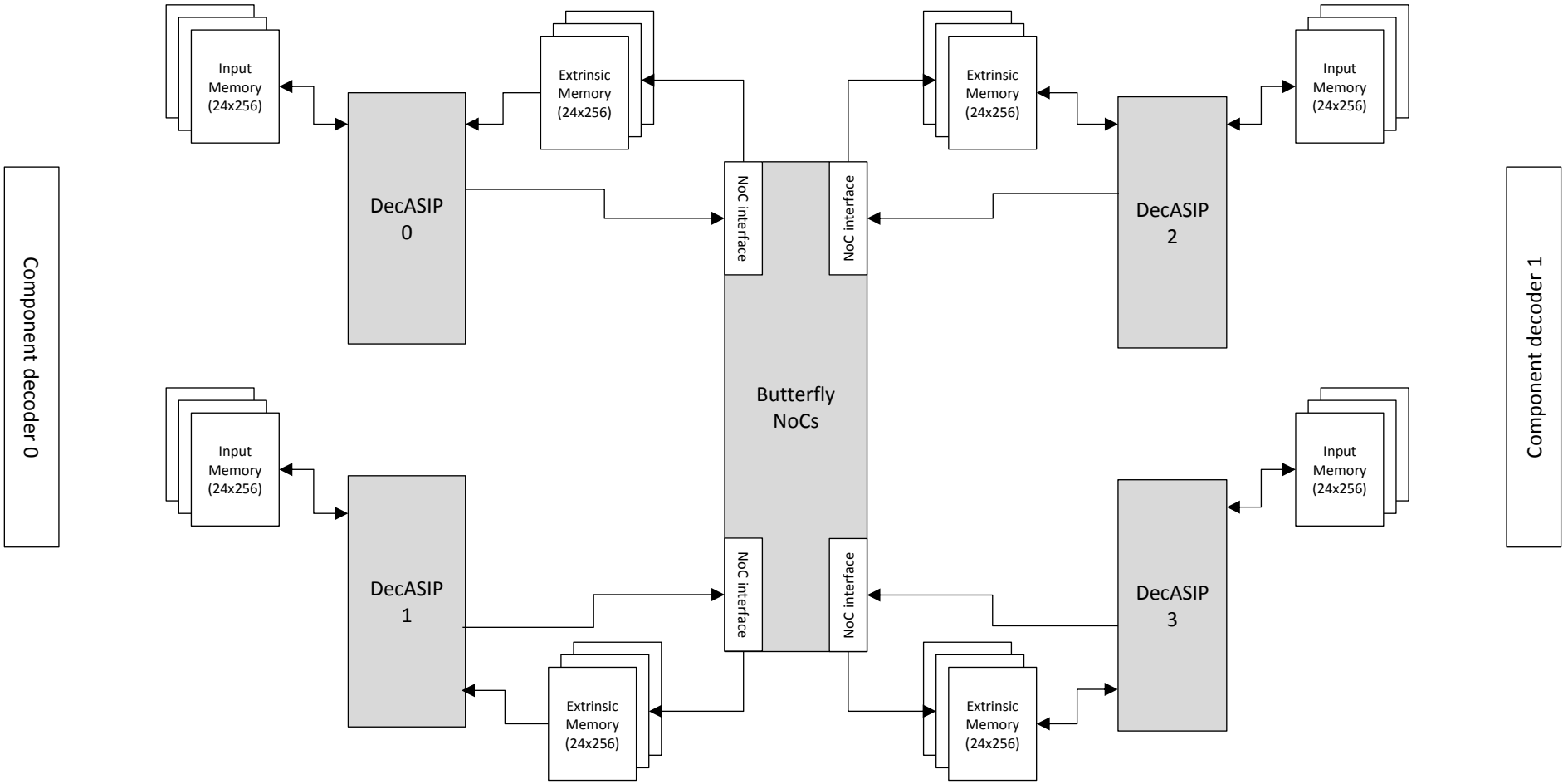
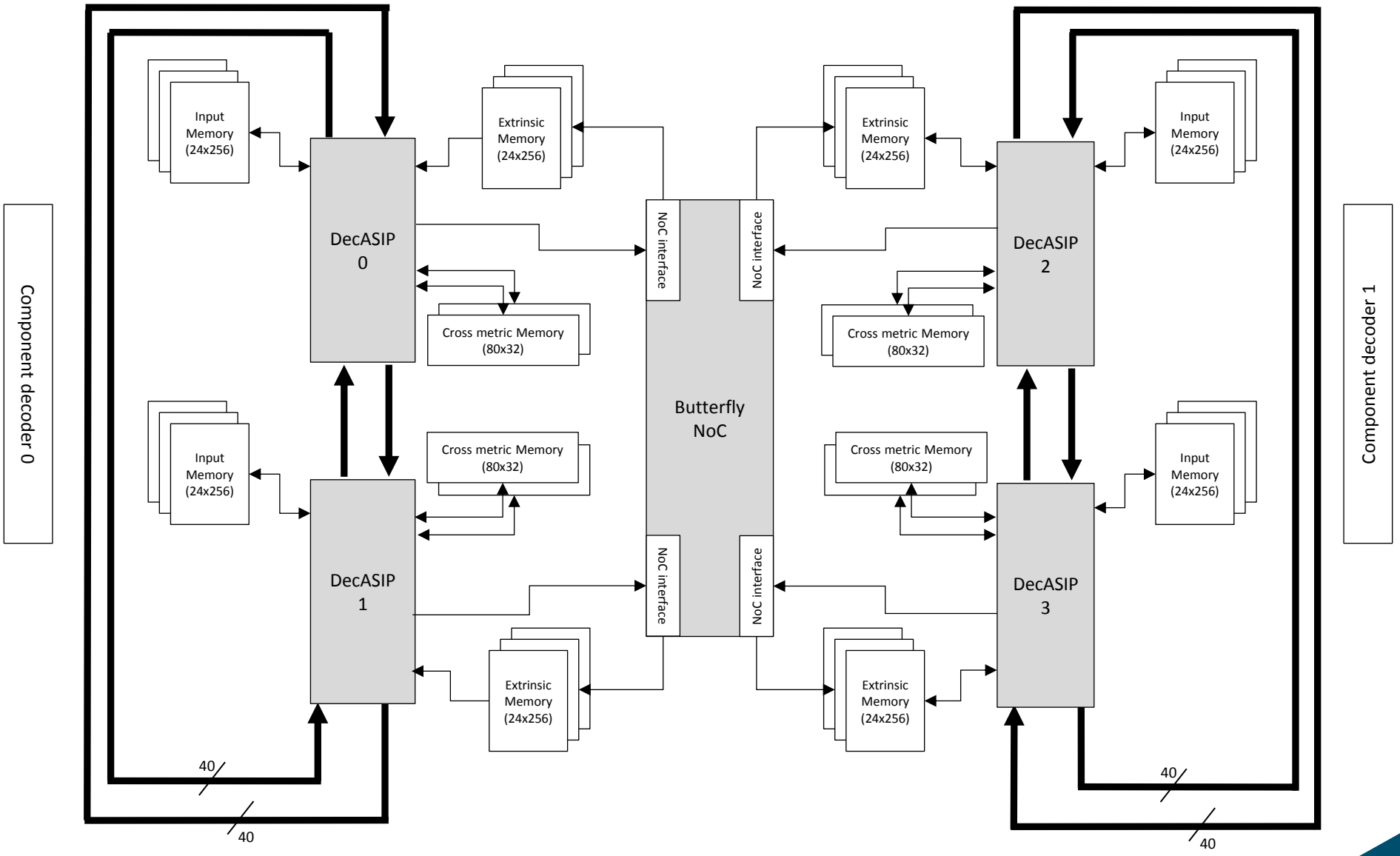
UDec architecture - DecASIP

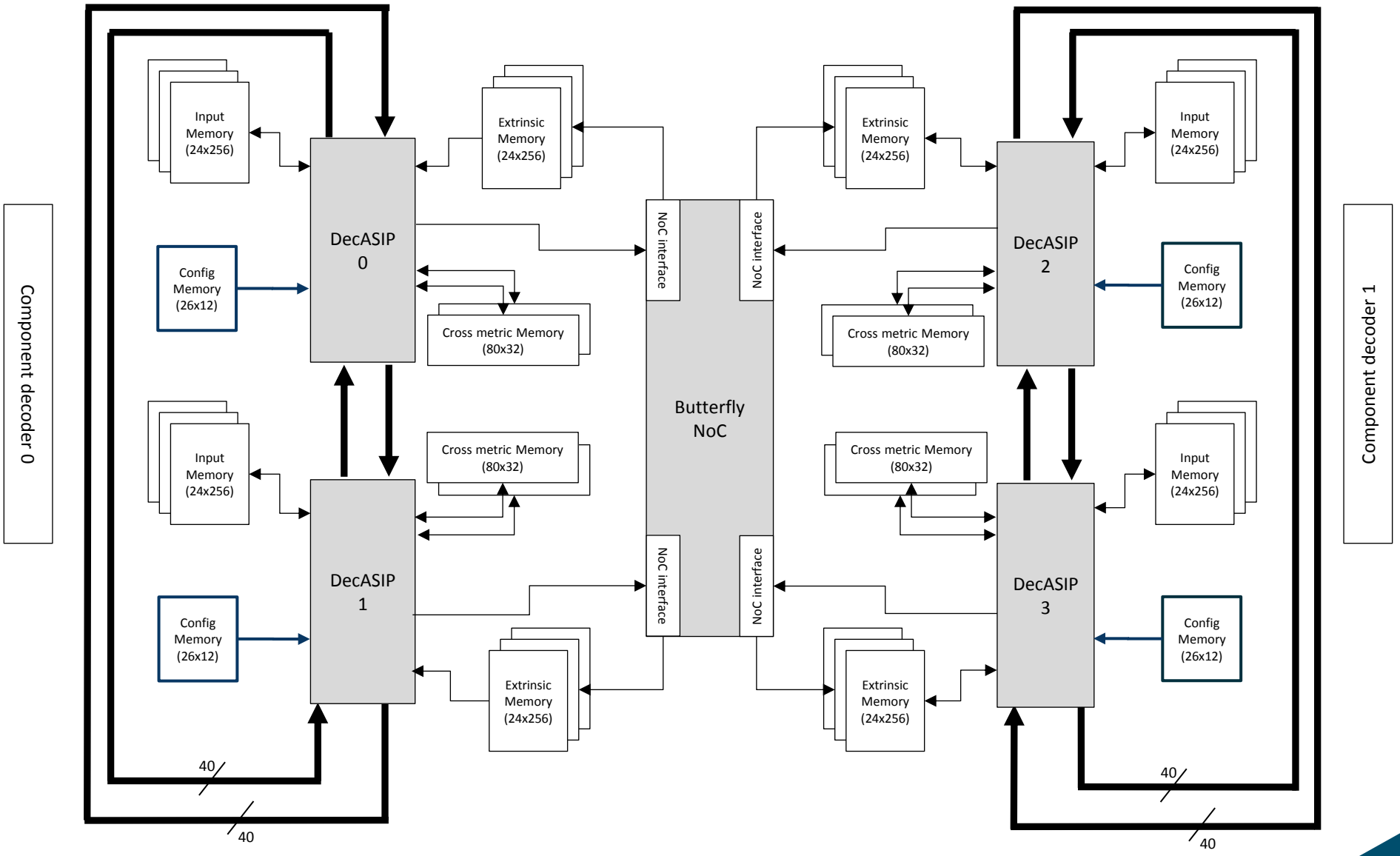
UDec architecture - Extrinsic information



UDec architecture – Boundary state metric



UDec architecture – Configuration memories



UDec Configuration

- The UDec platform is configured through DecASIPs configuration memories
  - can be loaded during the treatments
  - can store several configurations

@	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	-																					Tail	ASIPId			
1	Turbo Seed 0																		Turbo Seed 1							
2	-						TurboInitIteration						Maxiteration						State				NumSteps			
3	Turbo Step 0																		Turbo Step 1							
4	Turbo Step 2																		Turbo Step 3							
5	Turbo Step 4																		Turbo Step 5							
6	Turbo Step 6																		Turbo Step 7							
7	-		@ Tail bits													Scaling Factor								Mode		
8	Turbo PrevStep																		Blocklength in bits							
9	-			NumASIPs				StepIndex				WindowSize								LastWindowSize						
10	-			CurrentWindowN_norm								CurrentWindowID_tail								WindowN_tail						

- Smart memory organization in 3 groups
  - Optimized transfer mechanisms
    - ✓ From @ 0 to 1 : Unicast
    - ✓ From @ 2 to 6 : Multicast
    - ✓ From @ 7 to 10 : Broadcast

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Main challenges

- Low complexity
  - Unidirectional
  - 1 Master
  - Bus-based approach
- Multicasting and Broadcasting
  - Memory organization
- Dynamic Selection
  - Configuration transfer for activated ASIPS only
- Incremental data burst transfer
  - Loading in adjacent parts in the configuration memory

DecASIP configuration memory

@	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	-																					Tail	ASIPId			
1	Turbo Seed 0																		Turbo Seed 1							
2	-						TurboInitIteration						Maxiteration						State					NumSteps		
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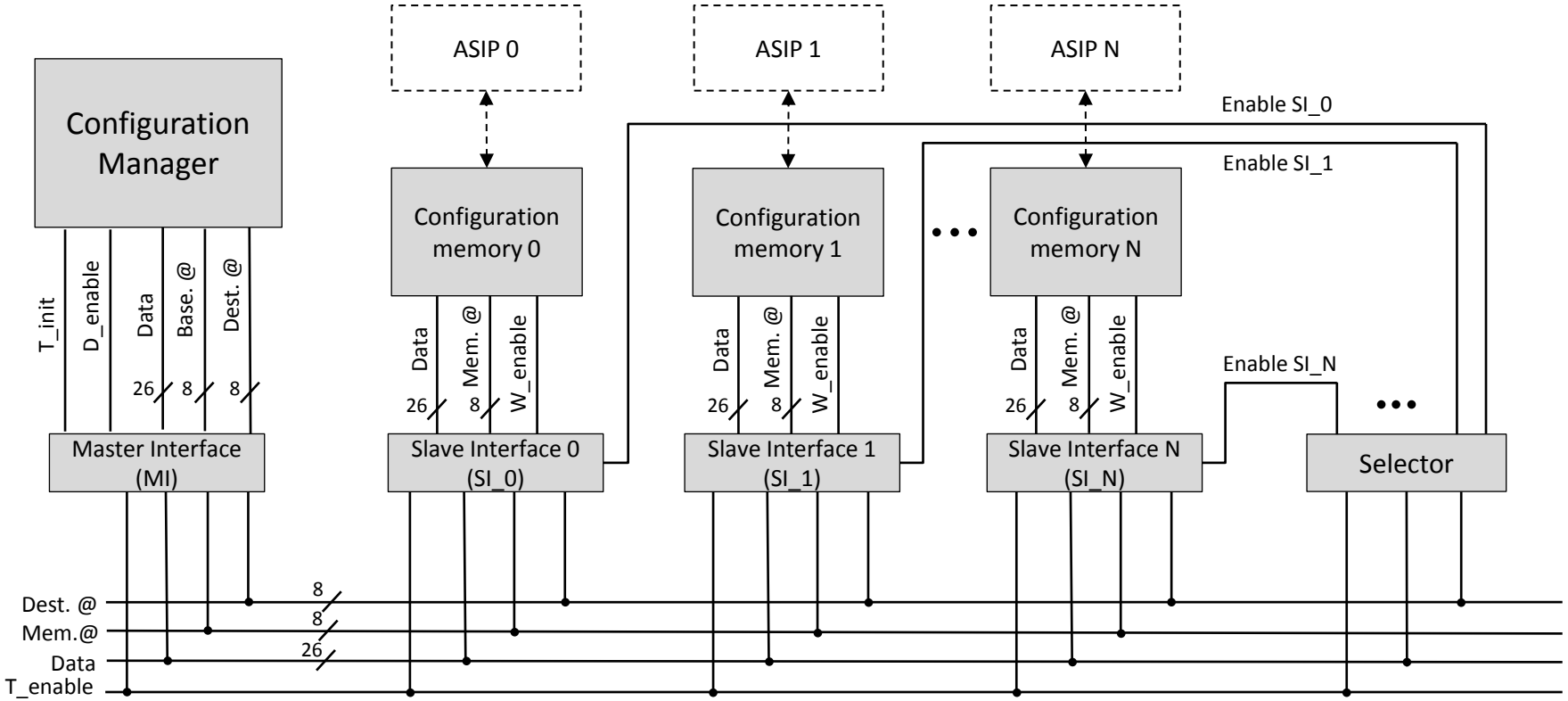
9	-	NumASIPs				StepIndex					WindowSize								LastWindowSize							
10	-	CurrentWindowN_norm									CurrentWindowID_tail								WindowN_tail							

Main challenges: SoA

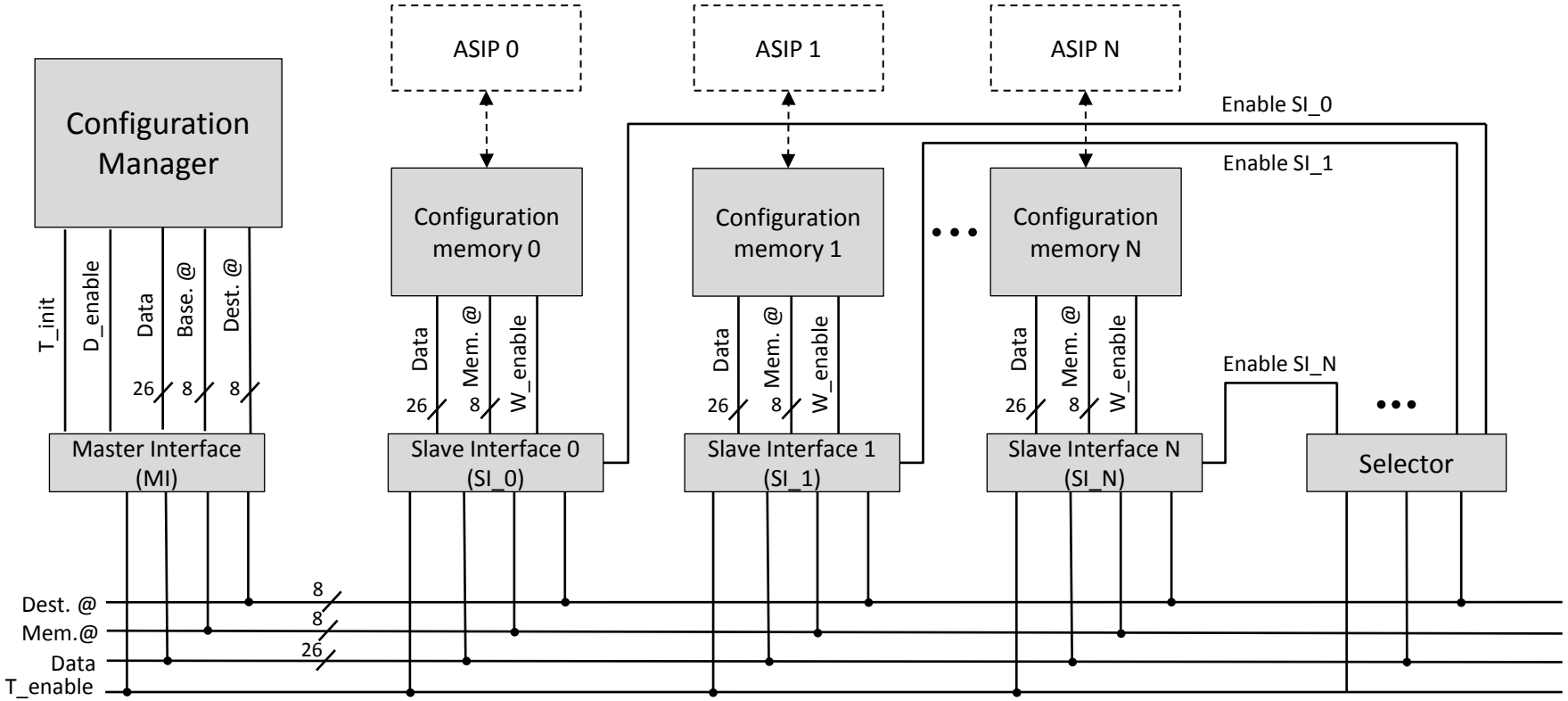
Challenges	AMBA	CoreConnect	Avalon	SiliconBackplane	FSL	This work
Unidirectional (or 1 master)	✓	✓	✓	✓	✓	✓
Multicasting	X	X	X	✓	X	✓
Broacasting	X	X	X	✓	X	✓
Incremental burst	✓	✓	✓	✓	X	✓
Low complexity	X	X	X	X	✓	✓

Architecture overview

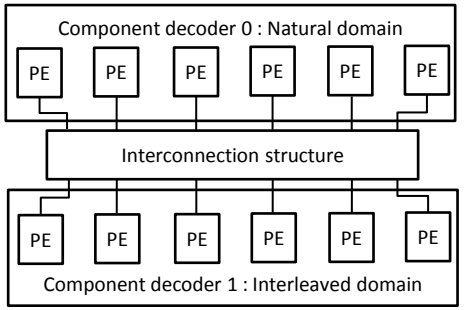


- The Configuration Manager generates and sends the configurations
- The MI provides an interface allowing the connection of the configuration manager to the bus.
- The SI provides an interface between the bus and the configuration memory.
- The Selector provides a simple solution to select, at run-time, DecASIPs that are targeted by the next configuration data.

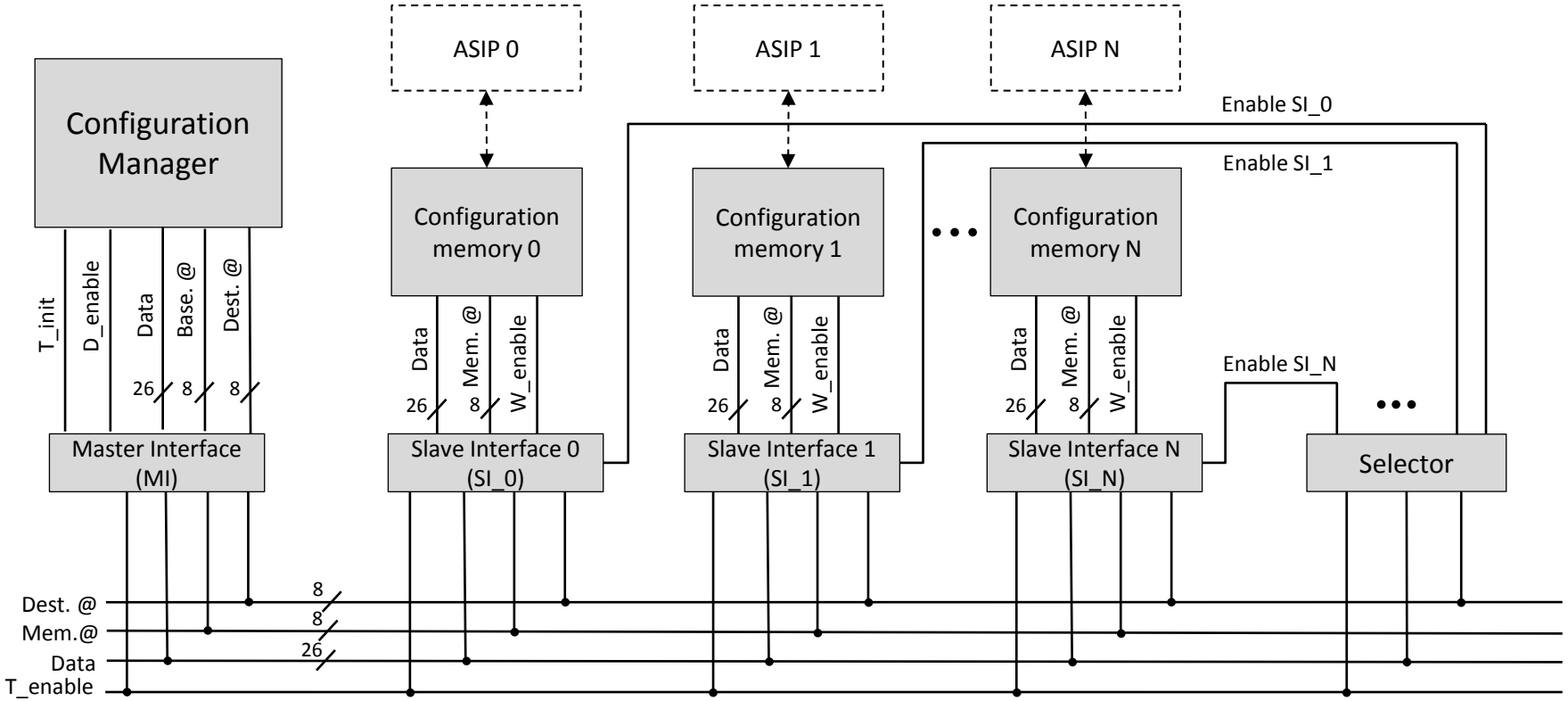
Addressing



- Each SI owns 3 static addresses: Broadcast @, Multicast @ and unicast @
- Each Selector owns a unicast address only

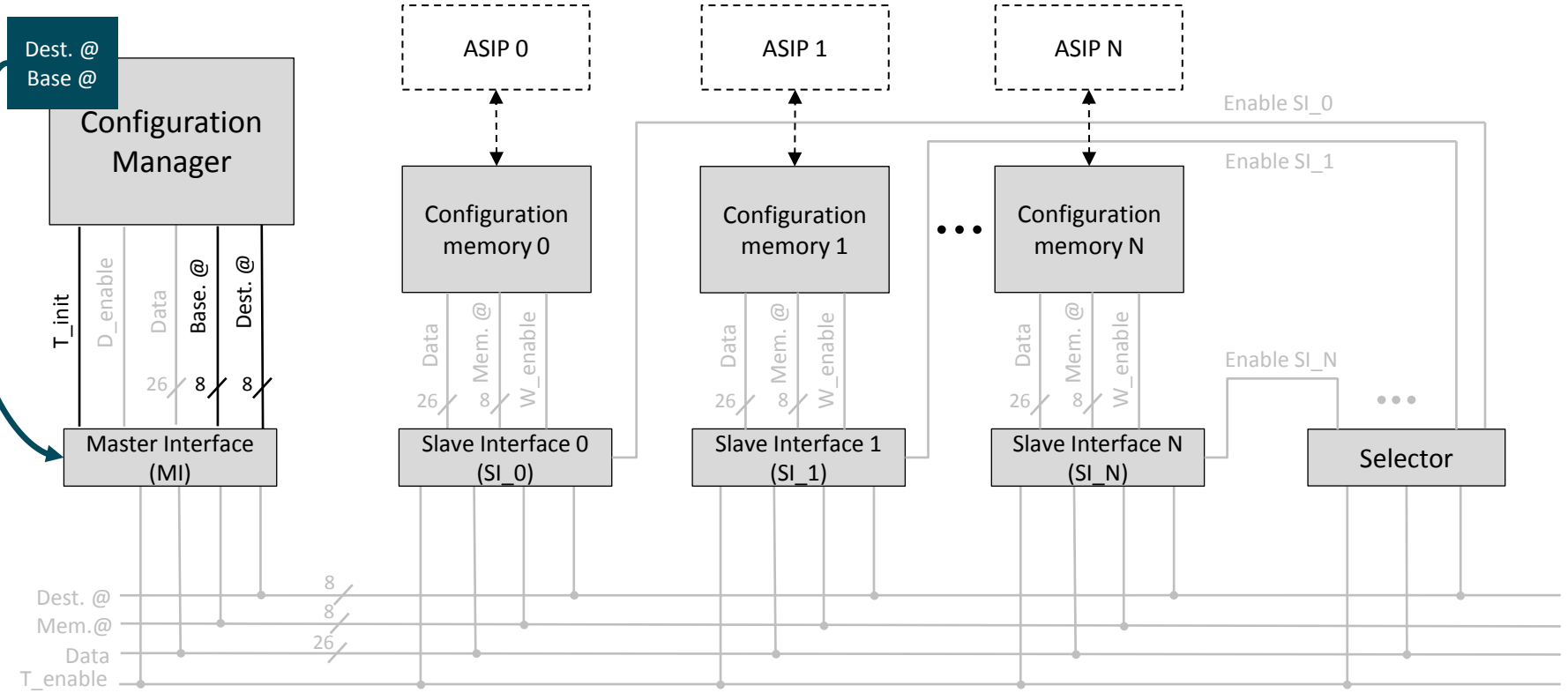


Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

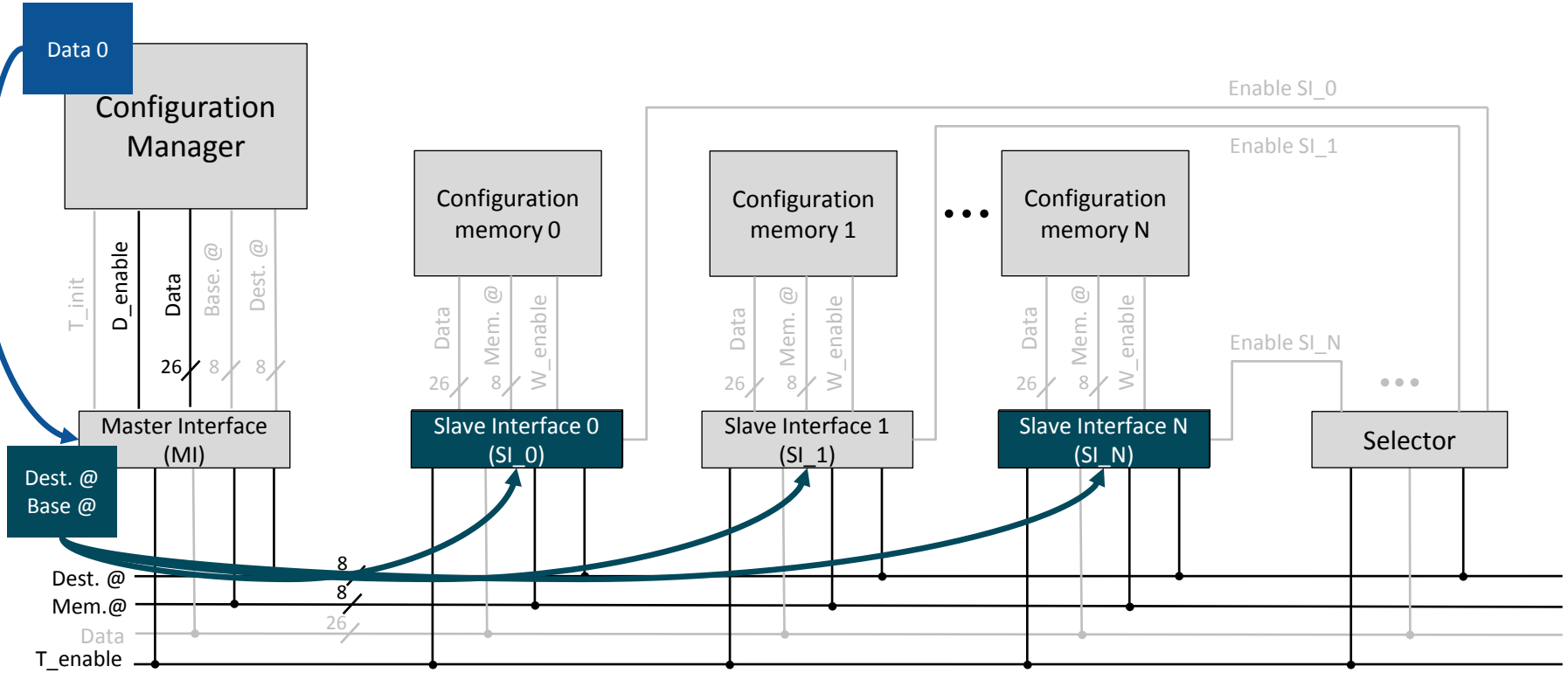
Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

- The destination and the base memory addresses are sent to the MI

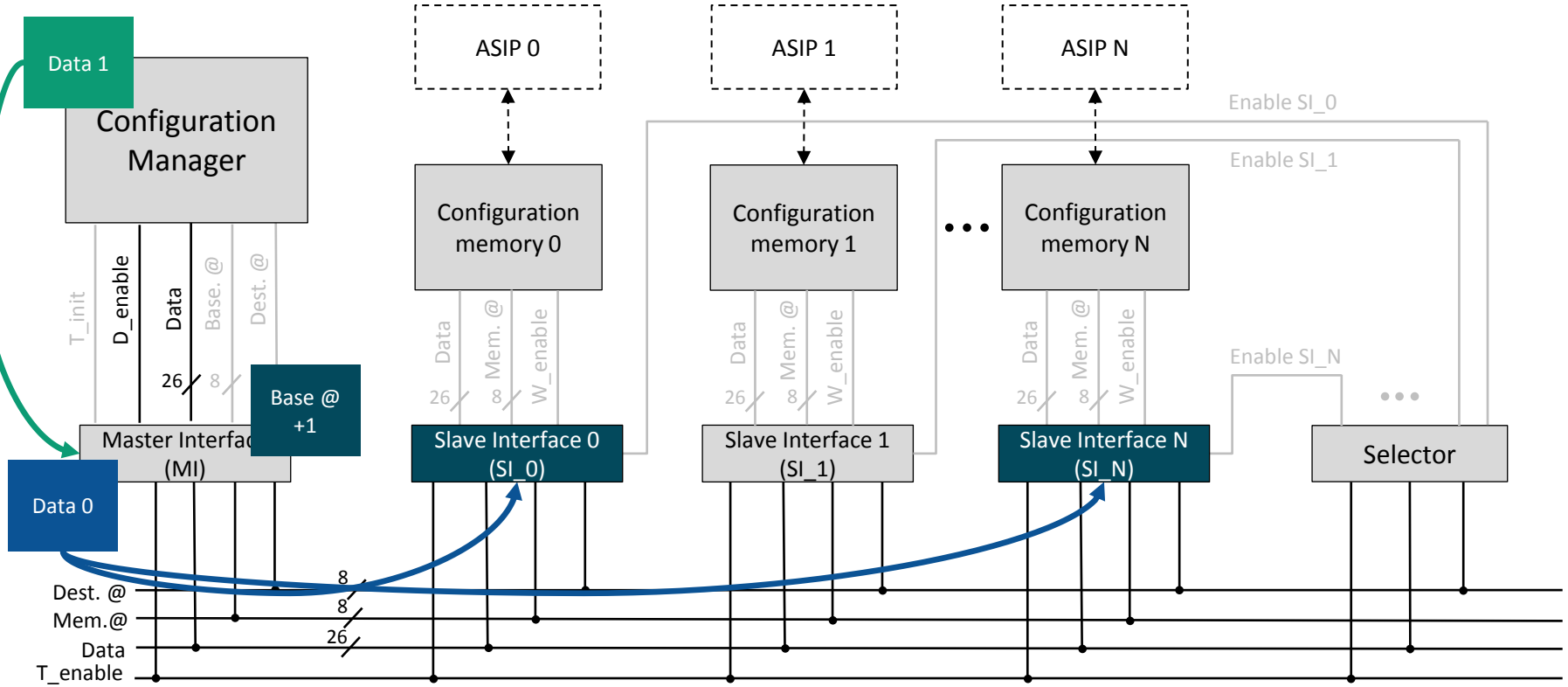
Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

- The destination and the base memory addresses are broadcasted on the bus.
- The first data is sent to the MI

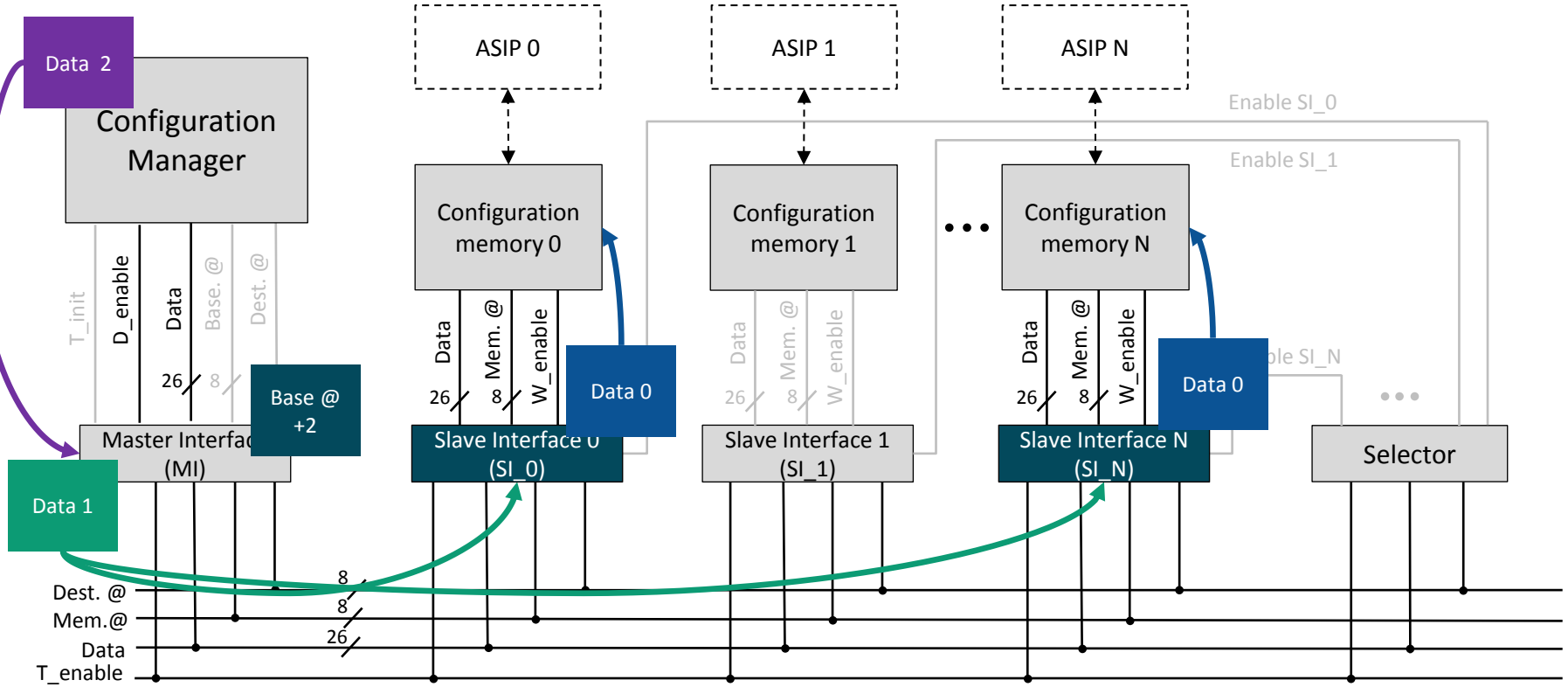
Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

- The First data is putted on the bus
- The second data is sent to the MI which increments the memory address

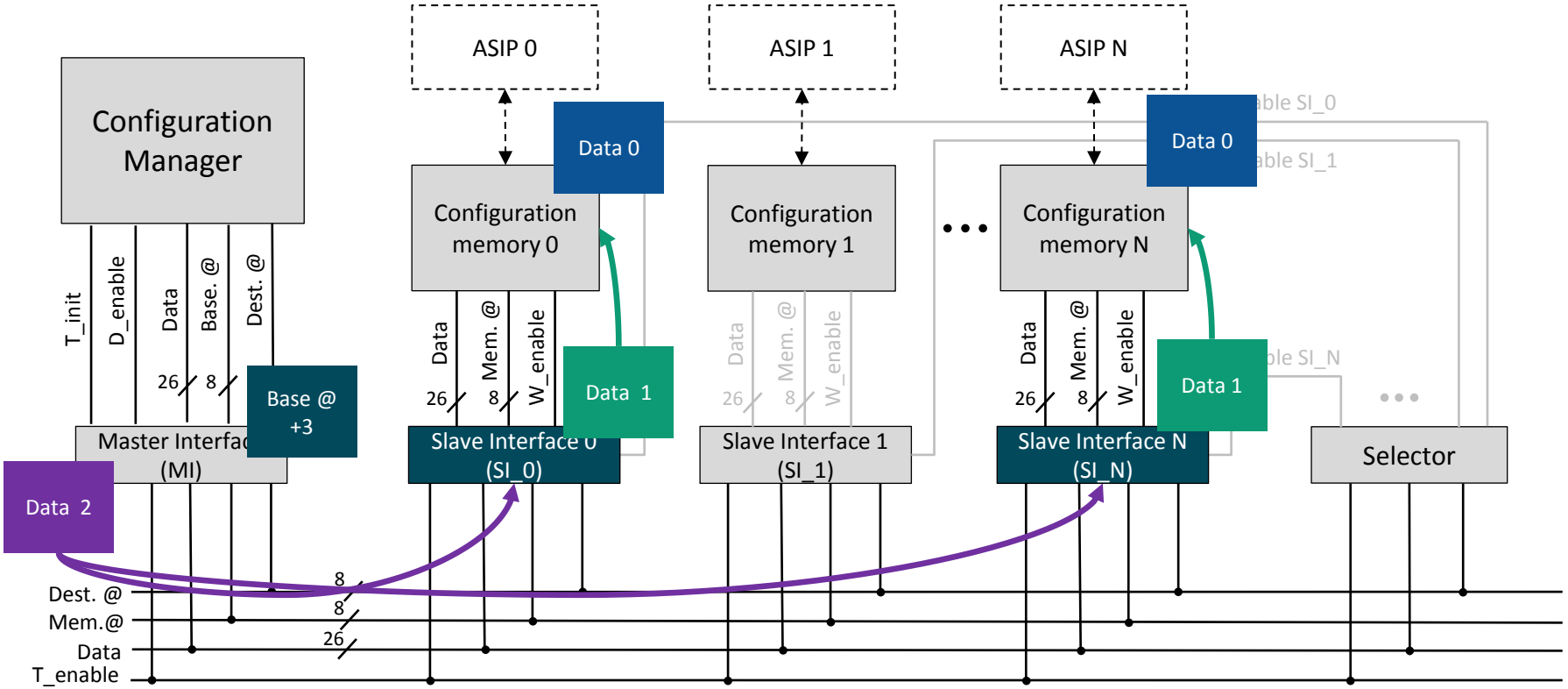
Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

- The SIs drive the memory signals for the first data
- The second data is putted on the bus
- The third data is sent to the MI

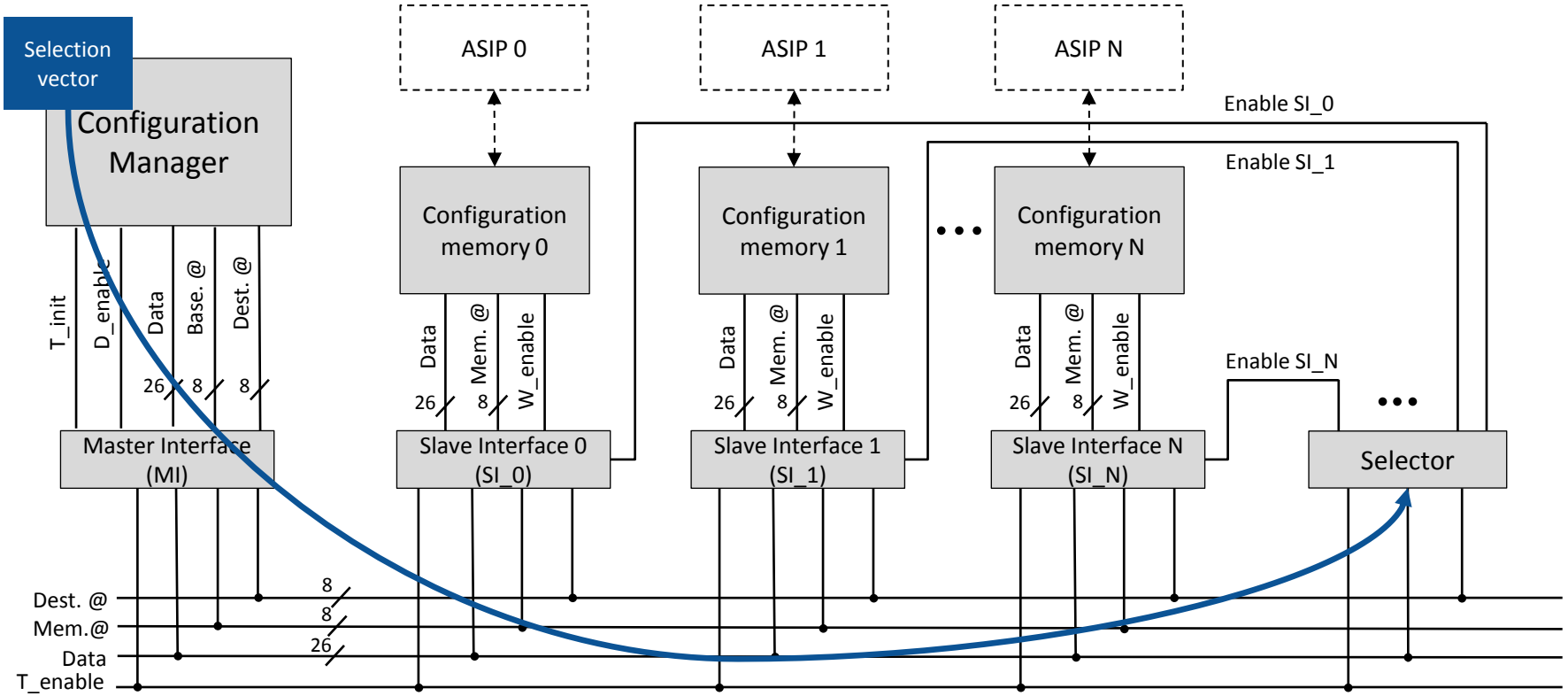
Transfer protocol: 5 steps



1. Transfer initialization
2. Address phase
3. Data phase
4. Memory input driving
5. Memory loading

- The first data is stored in the memory
- The SIs drive the memory signals for the second data
- The third data is putted on the bus

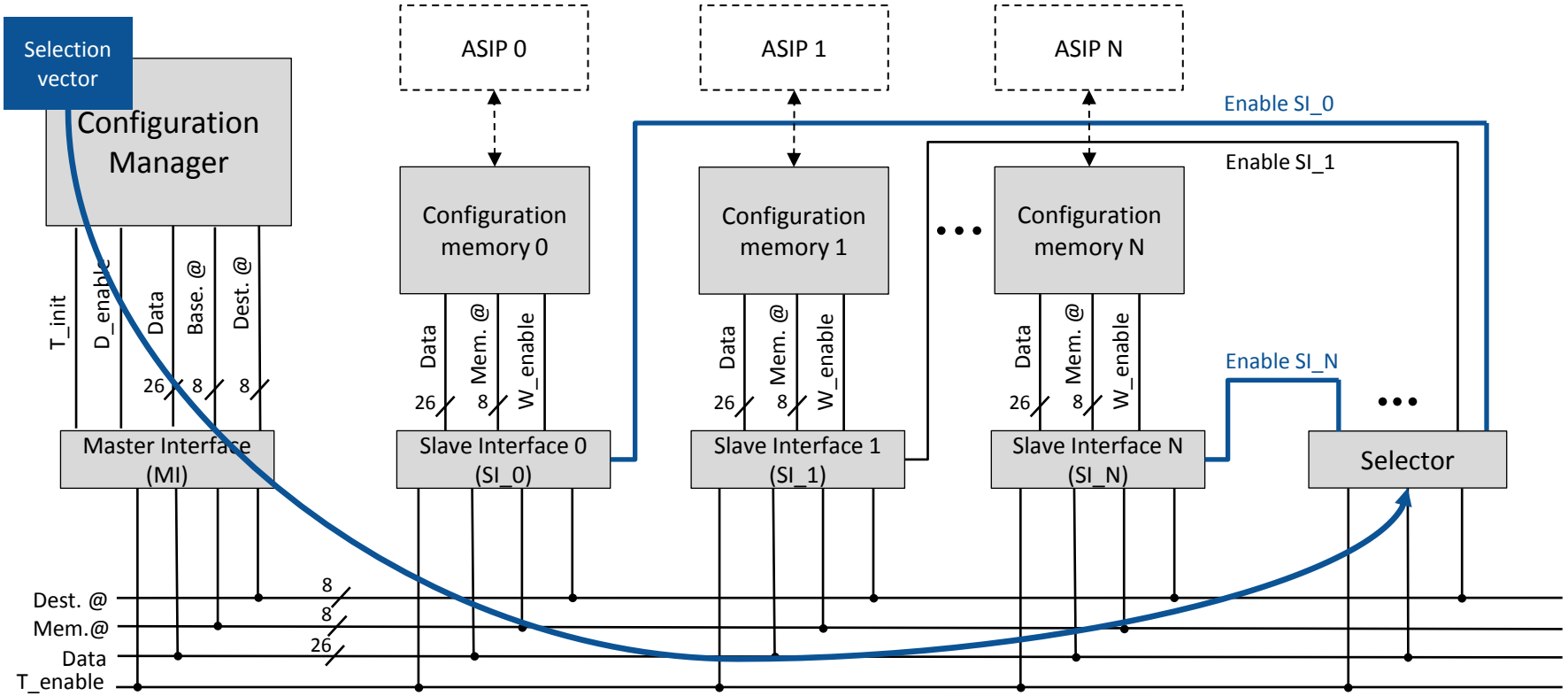
Selection



1. Transfer initialization
2. Address phase
3. Data phase
4. SIs configuration

- The Selector is configured through the bus infrastructure by the configuration manager which sends a configuration vector on the bus

Selection



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- The Selector is configured through the bus infrastructure by the configuration manager which sends a configuration vector on the bus

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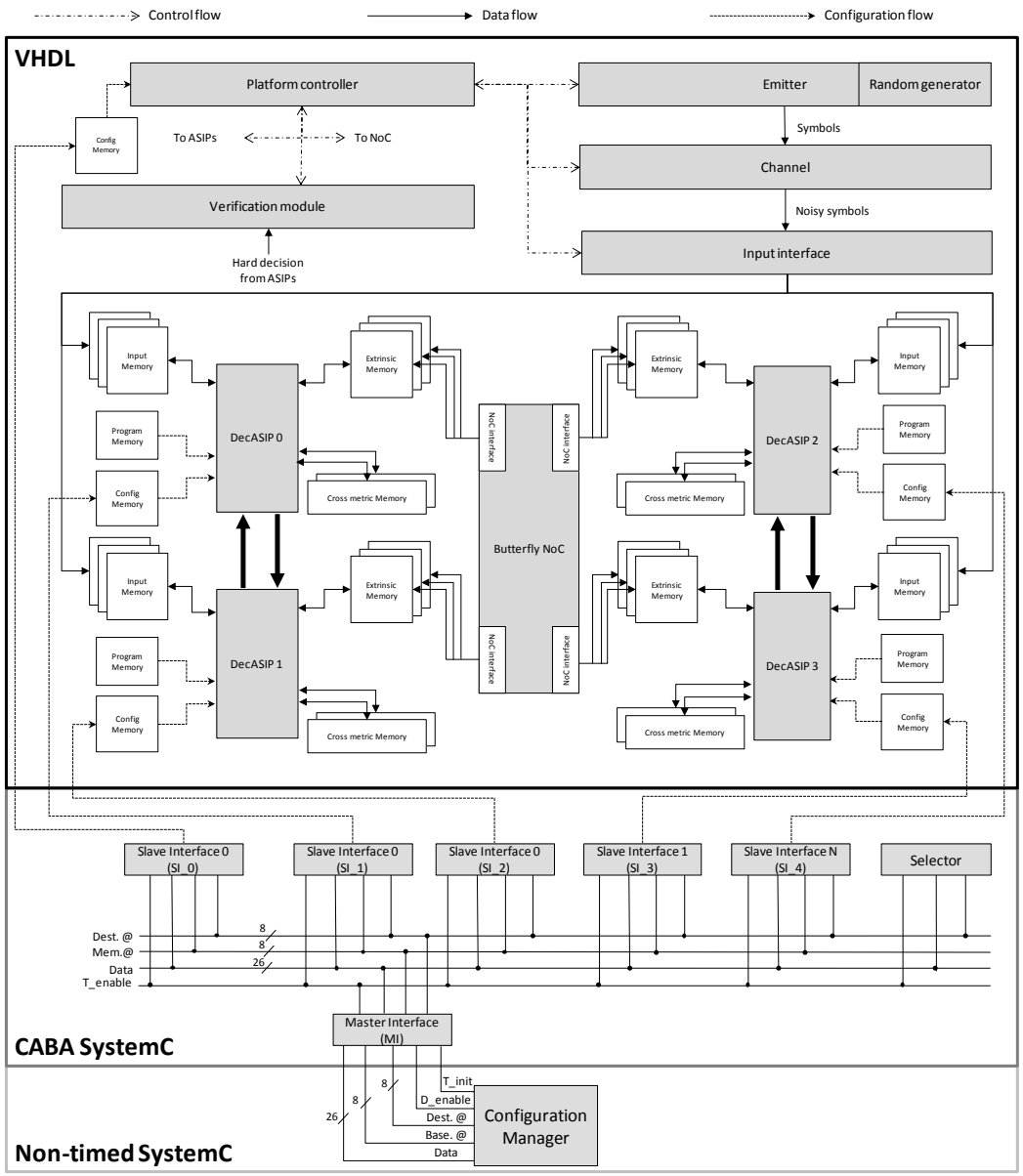
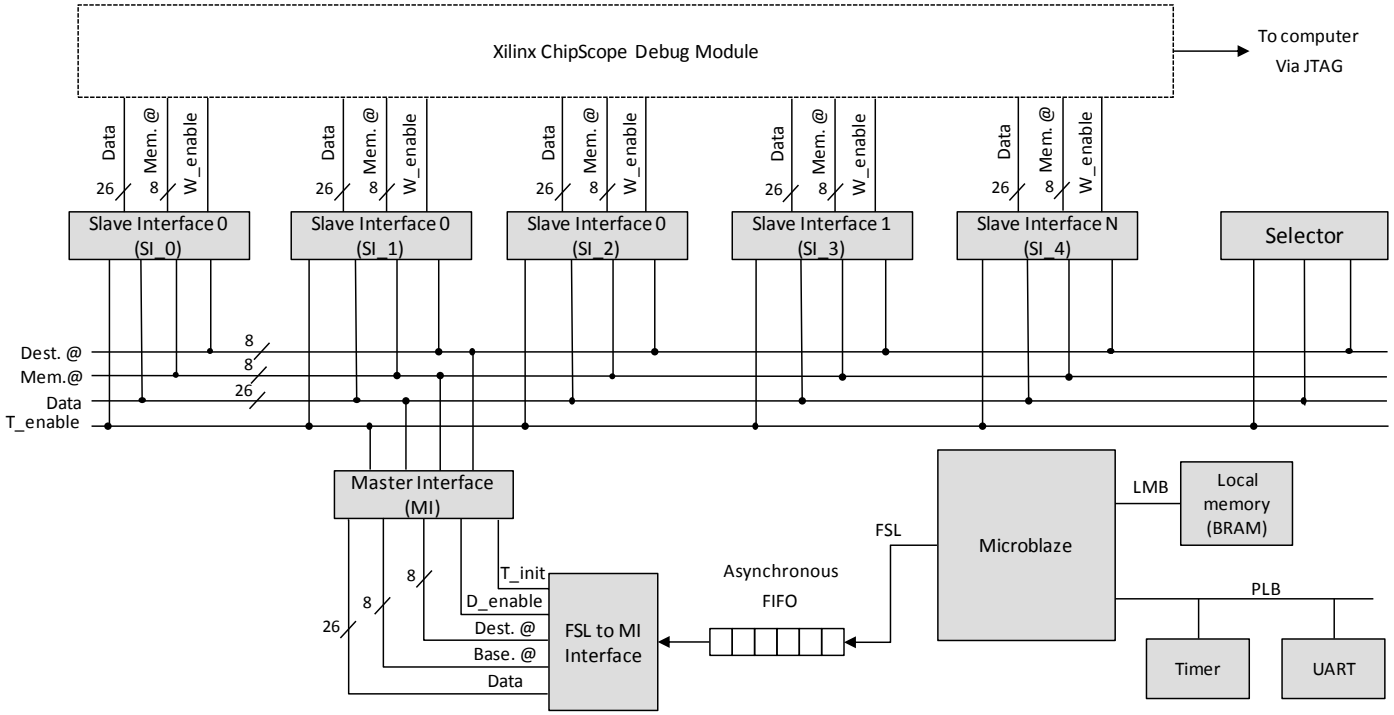
SystemC / VHDL mixed simulation



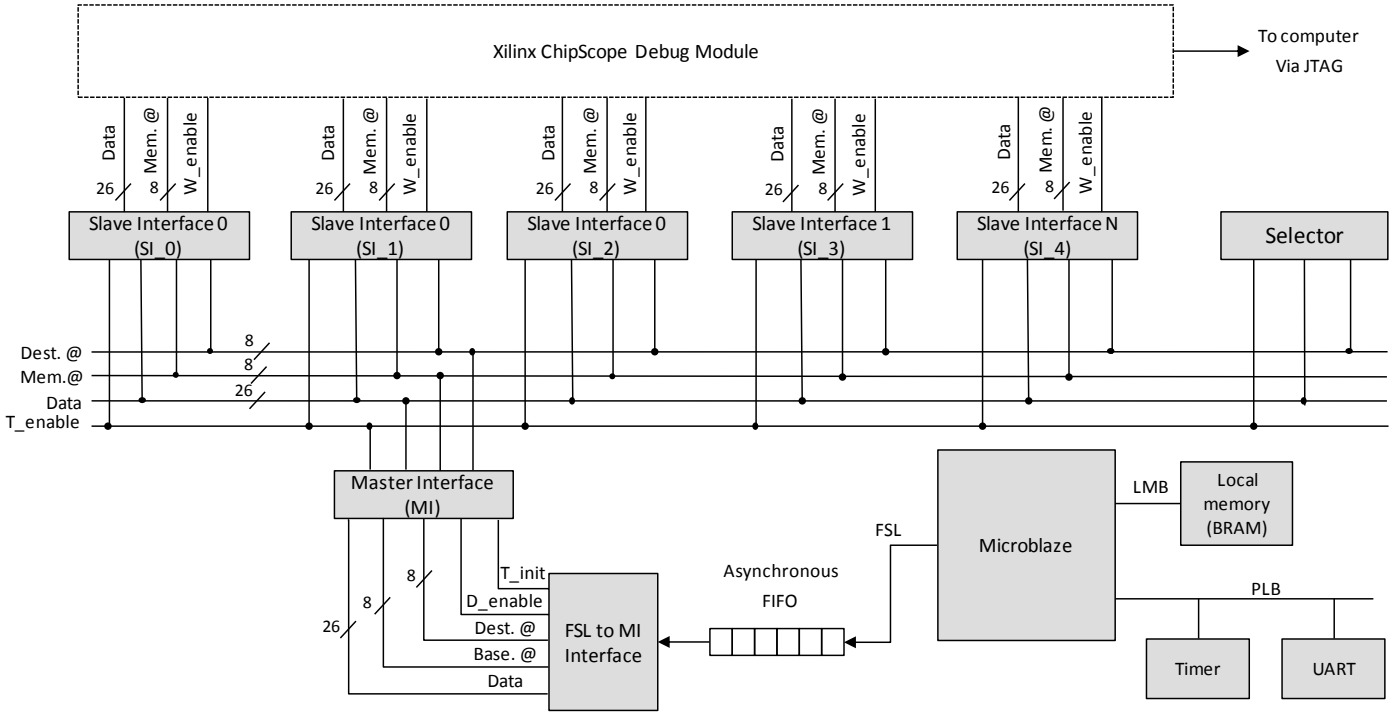
- Fast protocol validation:
  - Functional testing
  - Realistic scenarios
  - Model performance evaluation:

$$\text{Configuration latency} = \frac{31 + (3.N_{ASIP})}{\text{Bus frequency}}$$

FPGA prototype



FPGA prototype



Nb. ASIPs	Transfer latency (in ns)			Speedup	
	This work	PLB4	AXI4	vs. PLB4	vs. AXI4
4	1 032	3 872	2 212	3.75	2.14
6	1 176	5 808	3 168	4.94	2.69
8	1 320	7 744	4 224	5.87	3.2
16	1 896	15 488	8 448	8.17	4.45
32	3 048	30 976	16 896	10.16	5.54
64	5 352	61 952	33 792	11.57	6.31

- FPGA Hardware performance evaluation:

$$\text{Configuration latency} = \frac{93 + (9.N_{ASIP})}{125\text{MHz}}$$

ASIC evaluation

Infrastructure component	Area (in µm²)
MI	1 790
SI	1 150
Selector	784
Infrastructure for 4 DecASIPs	15 199
4 DecASIPs	738 552

- Logical synthesis
  - 65 nm CMOS
  - 500 MHz
  - Configuration infrastructure area overhead for 4 DecASIPs:2%

ASIC evaluation

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- Logical synthesis
  - 65 nm CMOS
  - 500 MHz
  - Configuration infrastructure area overhead for 4 DecASIPs:2%

Nb. ASIPs	Transfer latency (in ns)		Speedup
	FPGA	ASIC (estimated)	
4	1 032	86	12
6	1 176	98	12
8	1 320	110	12
16	1 896	158	12
32	3 048	254	12
64	5 352	446	12

- ASIC performance estimation
  - Speedup : 12 vs. FPGA (125Mhz)

$$\text{Configuration latency} = \frac{31 + (3.N_{ASIP})}{500\,\text{MHz}}$$

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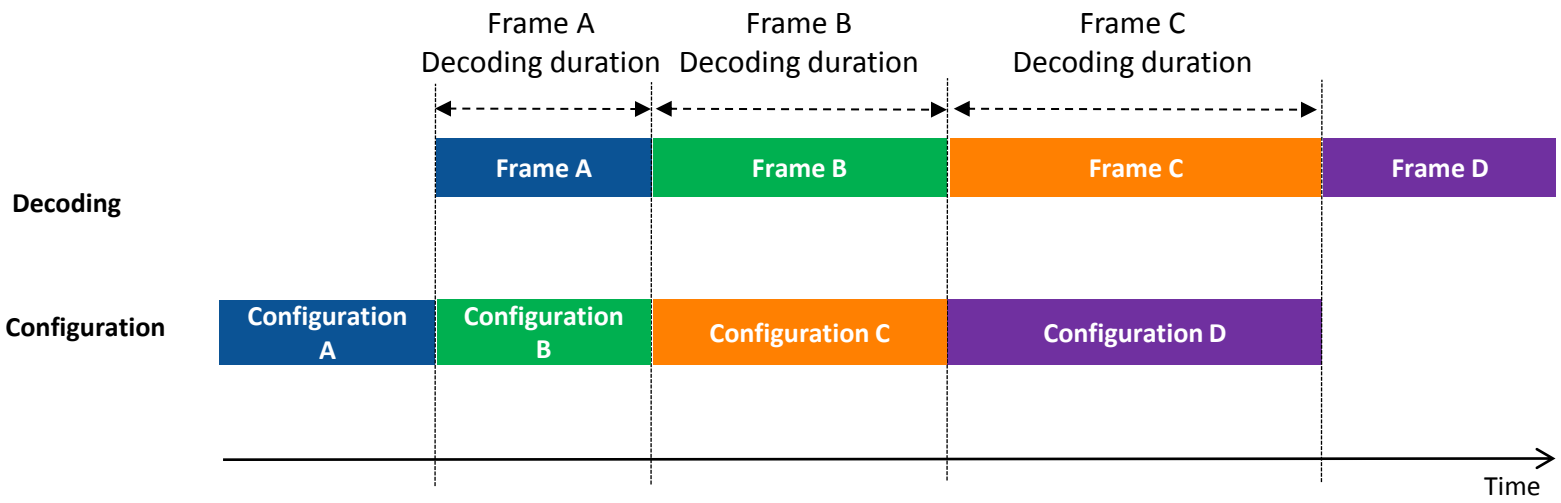
Conclusion

- Configuration data transfer in application specific multiprocessor platforms is still an important challenge

- Configuration infrastructure
  - Pipelined bus
  - Low complexity
  - Multicasting & Broadcasting
  - Incremental burst

Conclusion

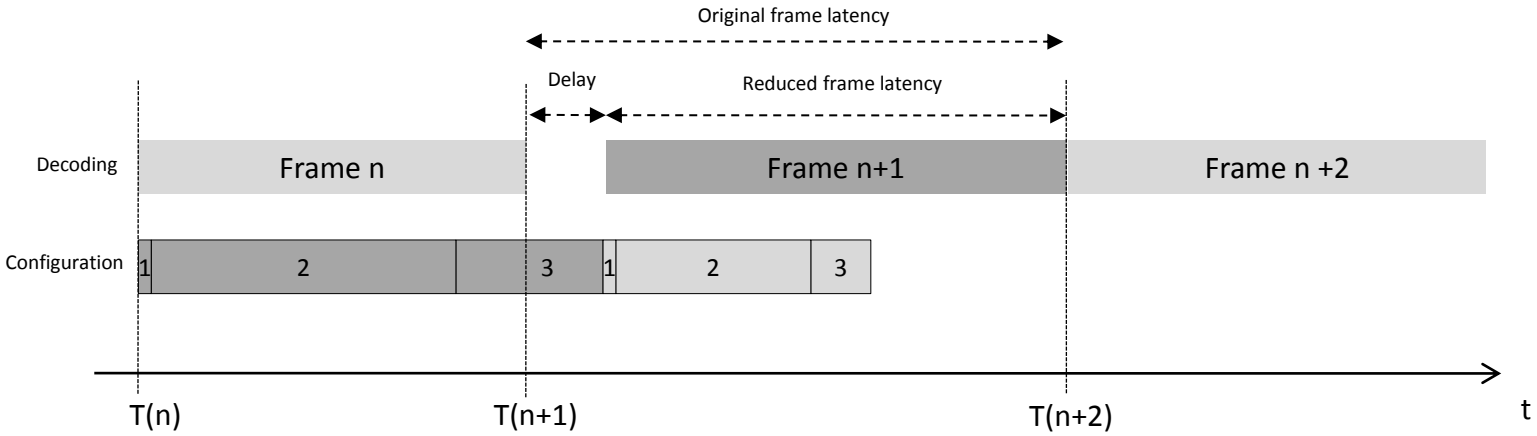


- Hardware implementation
  - FPGA: Configuration of 64 DecASIPs in 5.352 µs
  - ASIC (estimated): 0.446 µs (speedup = 12)

Thank you

Perspectives

- Smart configuration management for very high flexibility



1 Configuration manager read new frame parameters ; 2 configuration generation ; 3 Configuration transfer