



# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

Simen Gimle Hansen, Dirk Koch and Jim Tørresen

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UNIVERSITY  
OF OSLO

# Context Switching Reconfigurable Hardware for Communication Systems (COSRECOS)

## Methodologies

- Temporal module placement
- Analysis
- Partial reconfiguration

## Documentation

- Tutorials
- Labs
- Design examples



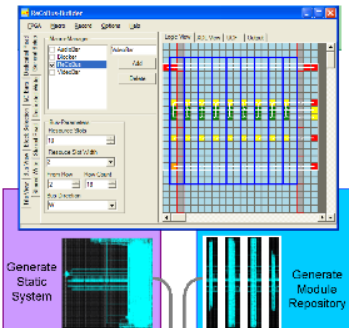
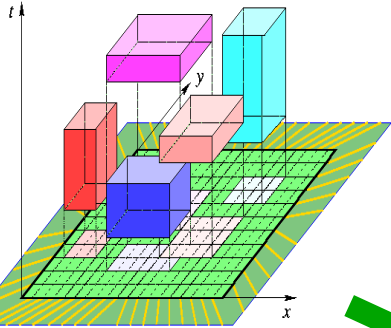
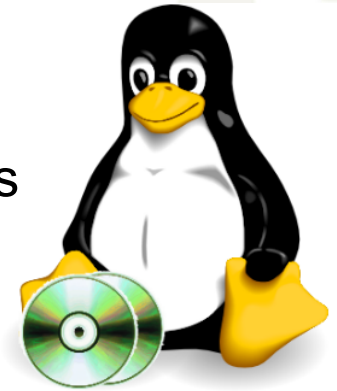
## Applications & reconfigurable systems

## Tools

- Floorplanning & constraining
- Bitstream assembly
- System generation

## OS4RC

- HW/SW interfaces & drivers
- Management
- Diagnosis



# Context Switching Reconfigurable Hardware for Communication Systems (COSRECOS)

**People** PhD students Alexander Wold, Simen G. Hansen and Christian Beckoff  
Postdoc Dirk Koch  
Project manager Jim Torresen

**Website (Google for ``COSRECOS``)**

<http://www.mn.uio.no/ifi/english/research/projects/cosrecos/>

The screenshot shows the website for the COSRECOS project. The header includes the UiO logo and the Department of Informatics, Faculty of Mathematics and Natural Sciences. A search bar is located in the top right. The main navigation menu includes Home, Research, Studies, Student life, Services and tools, About the department, and People. The left sidebar contains a 'Research' section with a 'Research projects' dropdown, and a 'CoSReCoS' section with links for News, Project Details, Publications, Contact, Master-projects at CoSReCos, Conferences, and Tools and downloads. The main content area features the project title 'Context Switching Reconfigurable Hardware for Communication Systems (CoSReCoS)' in a blue box. Below the title, there are two columns: 'FPGA / ASIC: run in space' with an image of a Xilinx Virtex-6 chip, and 'Software: run in time' with an image of a clock. Two green arrows point from the chip and clock images to the 'COSRECOS' text below them. A paragraph at the bottom explains the focus on computer hardware speed and performance, and the use of reconfigurable logic devices (FPGAs).

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**Research**

Research projects

CoSReCoS

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- Project Details
- Publications
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- Master-projects at CoSReCos
- Conferences
- Tools and downloads

**Context Switching Reconfigurable Hardware for Communication Systems (CoSReCoS)**

FPGA / ASIC: run in space      Software: run in time

**COSRECOS**

Much of the focus on computer hardware is on the speed and performance of the latest processors. In parallel to this development, reconfigurable logic devices (Field Programmable Gate Arrays (FPGAs)) are becoming increasingly popular. The main reason for this is that FPGAs can be configured to perform a wide range of functions, and they can be reconfigured in real-time. This makes them ideal for applications that require high performance and flexibility. The COSRECOS project is focused on developing a context switching reconfigurable hardware architecture for communication systems. The architecture is based on a combination of FPGAs and ASICs. The FPGAs are used for the context switching logic, and the ASICs are used for the communication processing. The project is currently in the design phase, and we are looking for students and researchers interested in this area.

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Departments

# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

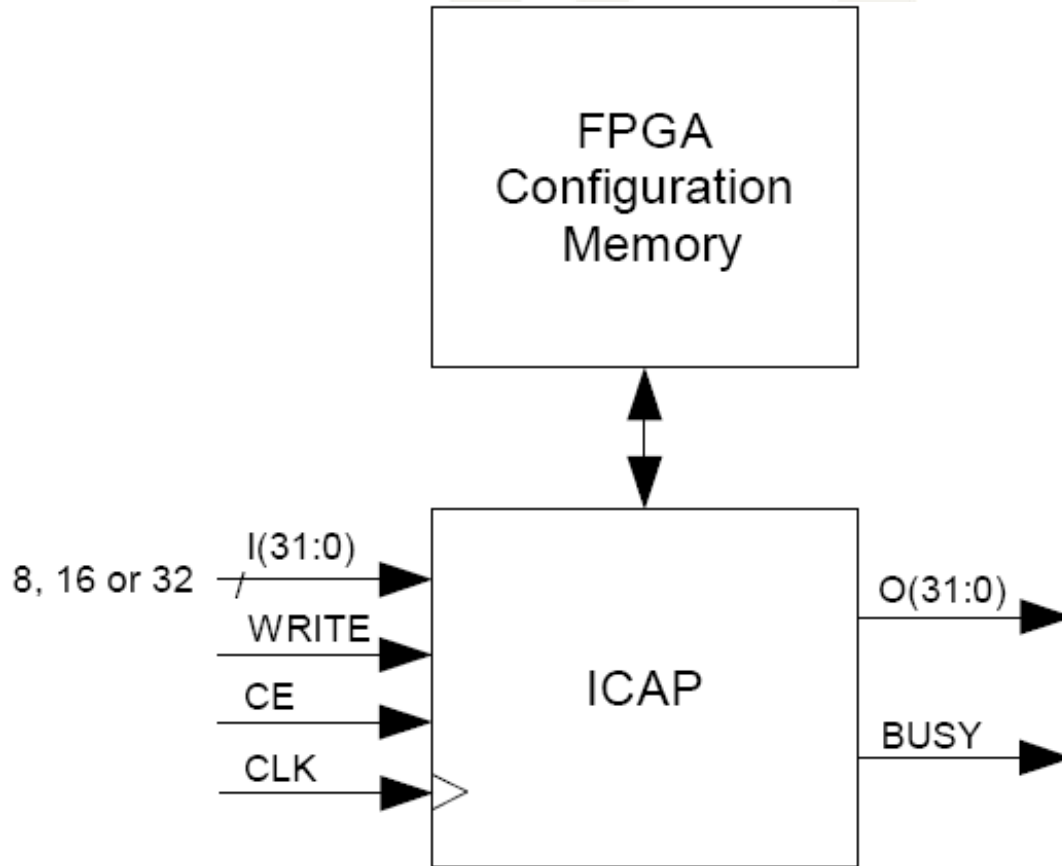
- Partial Run-Time Reconfiguration
  - Slow adaptation in industry
    - Lack of good design tools and design flows
    - No easy way to simulate
    - Simulation is important for product development
- This paper proposes:
  - A simulation framework for cycle-accurate functional modeling and verification of partial run-time reconfiguration at the Register Transfer Level (RTL) in VHDL

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# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Xilinx ICAP (Internal Configuration Access Port) port :

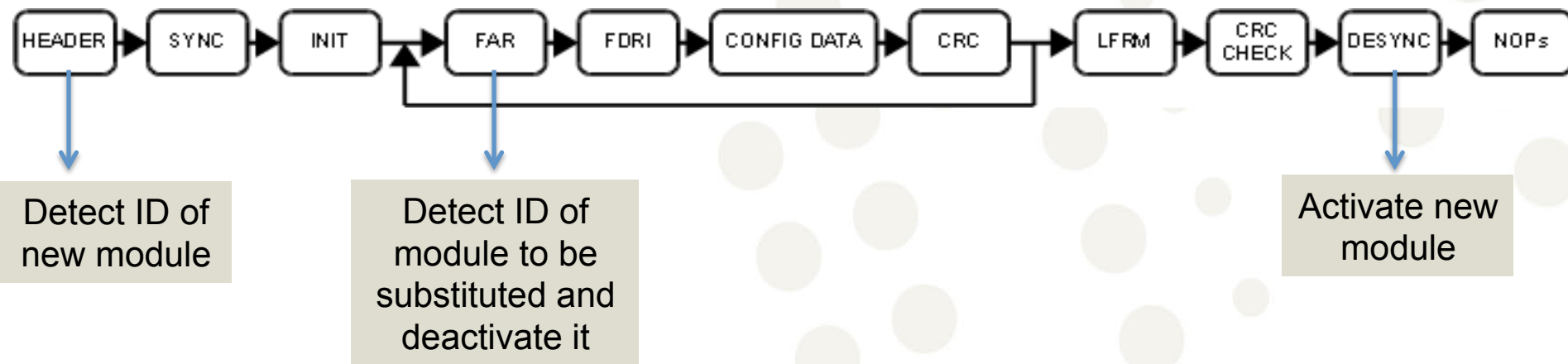


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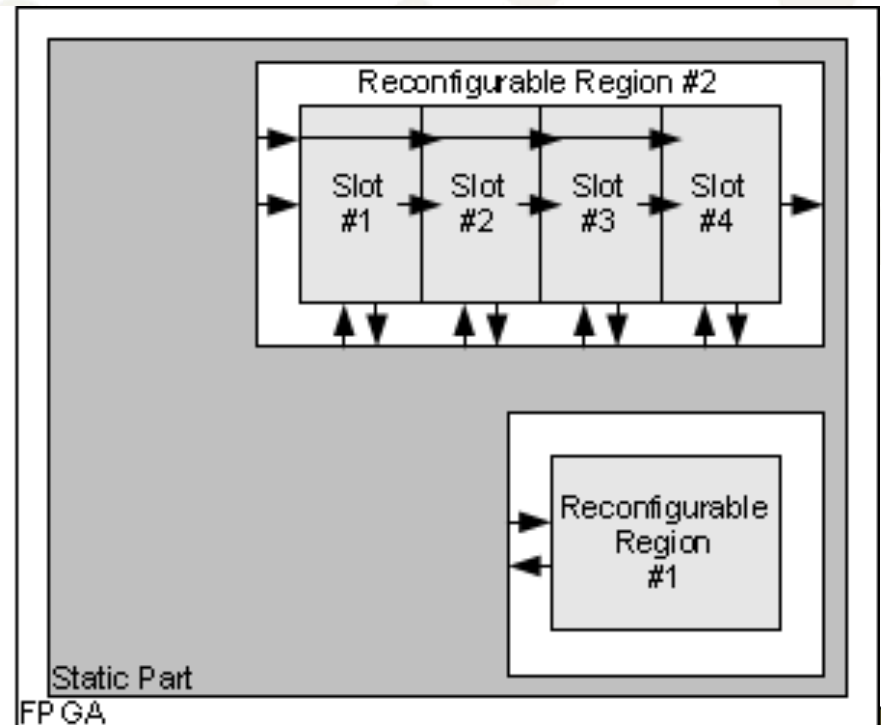
# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Xilinx bitstream format :



# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

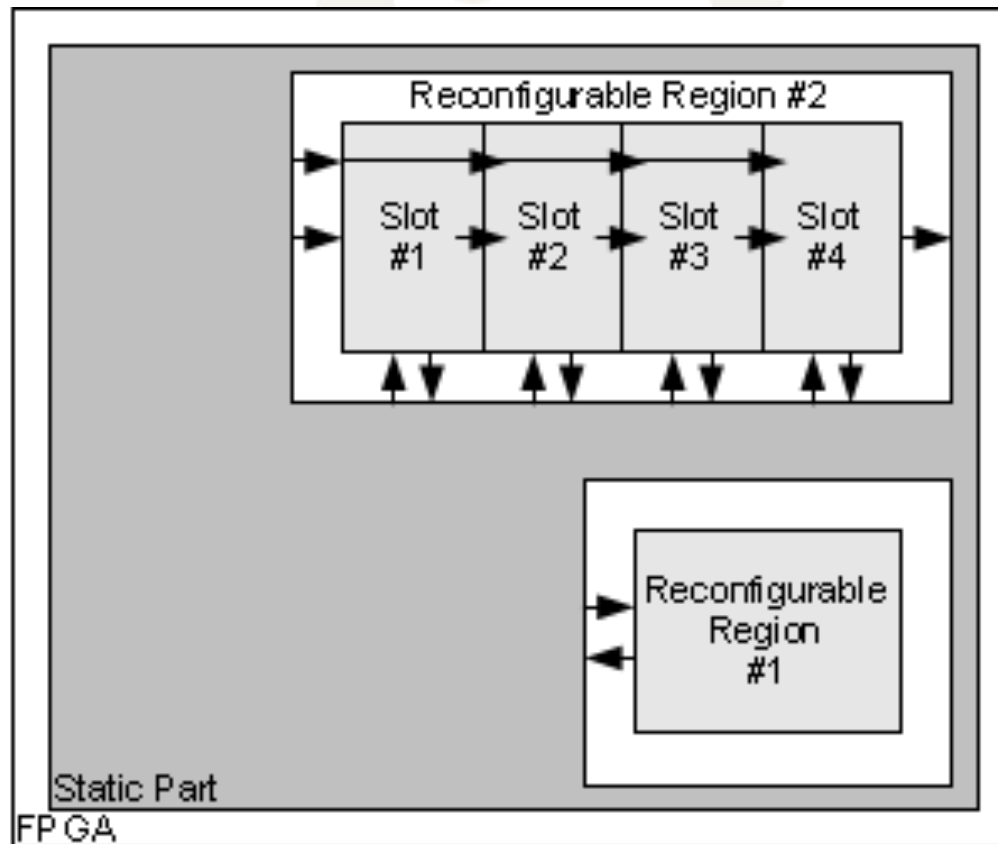
- Simulation Framework Features:
  - Using real bitstreams
  - Support for Island-based and Slot-based partial reconfiguration styles:
  - Support for module relocation



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# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Partial reconfiguration styles :



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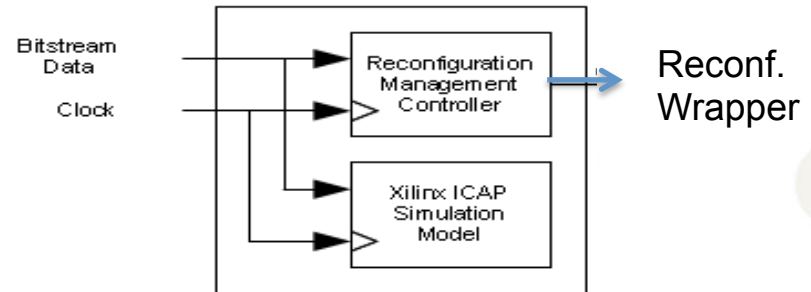
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# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfiguration Controller

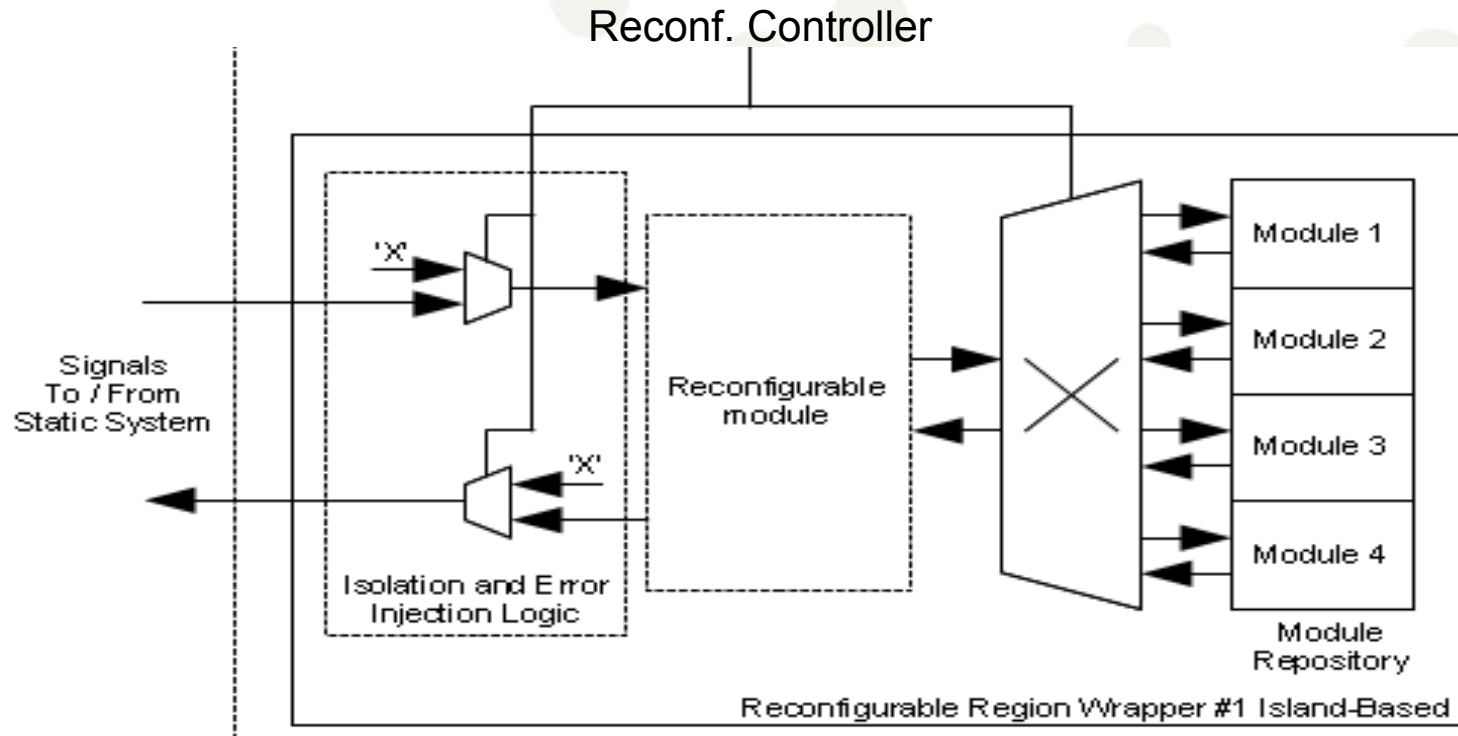
- Parses and tracks the bitstream



- Cycle-accurate based on extracted timing information (Xilinx ChipScope)
  - Keeps track of active and deactivated modules

# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfigurable Region Wrapper
  - Module Repository
  - Crossbar Multiplexer
  - Isolation and Error Injection Logic



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# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

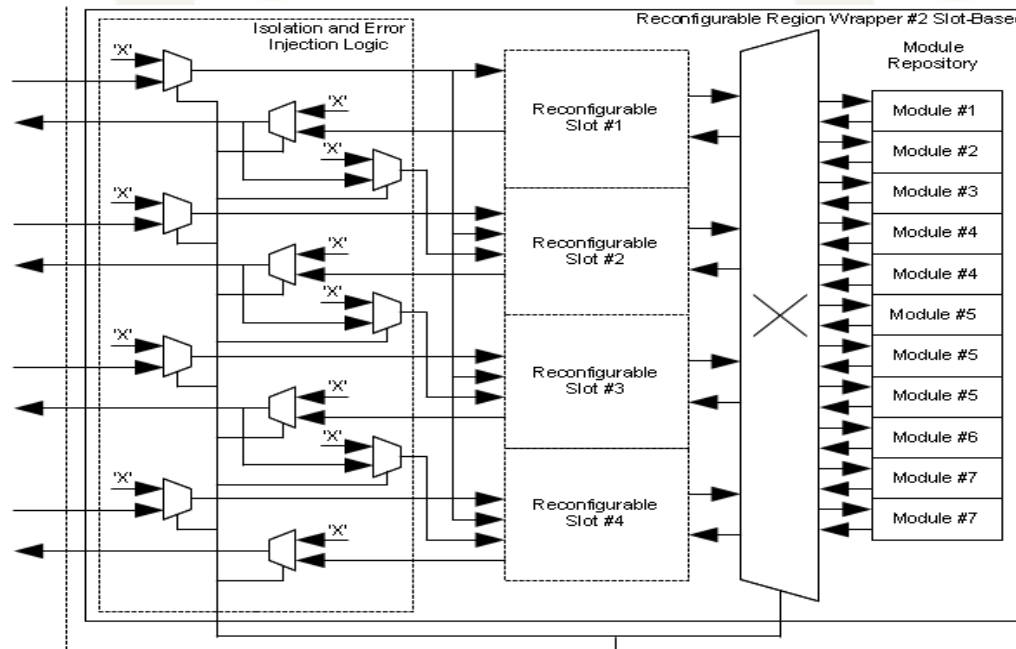
## Collecting Reconfiguration Timing Data:

- Cycle-accurate RTL Modeling achieved by extracting actual timing data from physical device using **Chipscope** (Digilent Atlys Spartan-6 XC6SLX45)
- Different logic resource types investigated (CLBs, DSP48, BRAM)
- **BRAMs** found to have "worst case timing" for deactivation and reactivation

# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

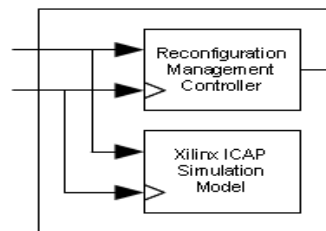
- Reconfiguration Controller
  - Controls the activation and deactivation of incoming and outgoing reconfigurable modules
  - Controls the Crossbar Multiplexer and Isolation and Error Injection Logic in the Reconfigurable Region wrapper
  - Supports :
    - Island-based and Slot-based reconfiguration styles
    - Multiple reconfiguration region
    - Module relocation

Signals to/from static system



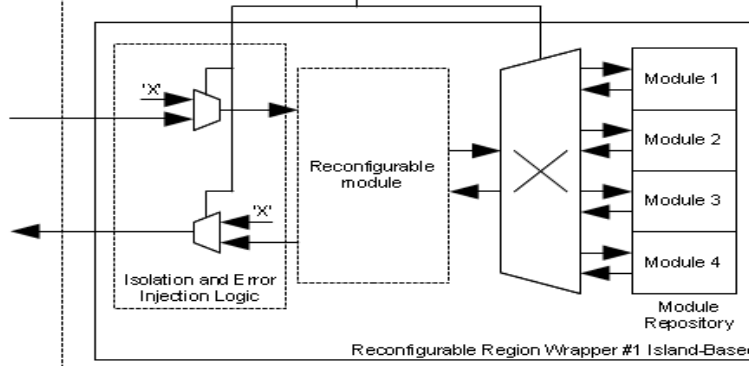
Configuration bitstream

Clock



Control Signals

Signals to/from static system



Static System


Reconfigurable Region Wrapper #1 Island-Based

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# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfiguration sequence :



Bitstream Data	Description
0xNNFF	Module identifier NN
0xFFFF	Dummy word
:	:
0xFFFF	Dummy word
0xAA99	SYNC MSB Word
0x5566	SYNC LSB Word
0XXXXX	Initialization commands
:	
0XXXXX	
0x3022	Write FAR
0XXXXX	FAR MAJ Address
0XXXXX	FAR MIN Address

# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

Bitstream Data	Description
0x30A1 0x0001	Write CMD Register Command WCFG
0x5060 0XXXXX 0XXXXX	Write FDRI FDRI MSB Value FDRI LSB
0XXXXX : 0XXXXX	First Configuration Data : Last Configuration Data
0XXXXX 0XXXXX	32-bit CRC MSB Value 32-bit CRC LSB Value

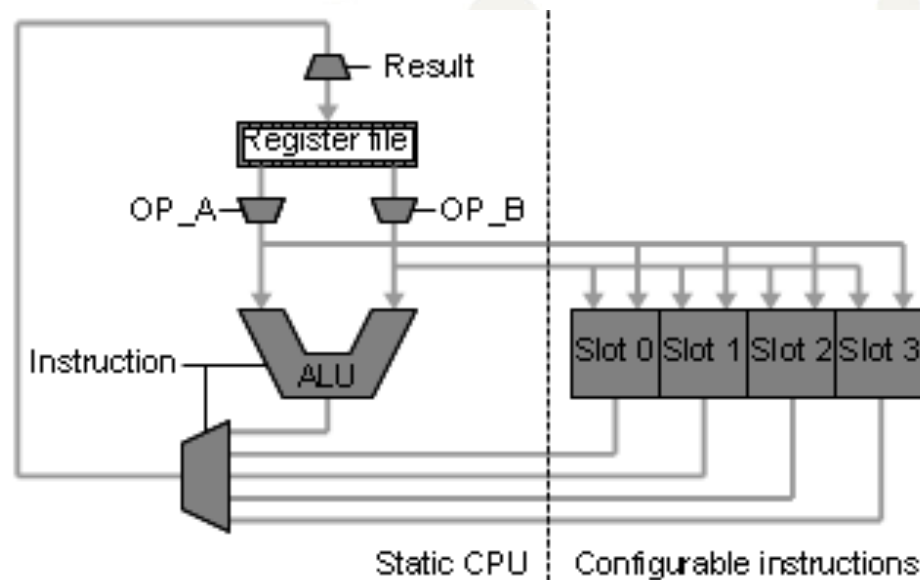
# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

Bitstream Data		Description
if	0x3022 0XXXX 0XXXX	Write Next FAR Address FAR MAJ Address FAR MIN Address Loop back to Write FDRI
else	0x30A1 0x0003	Write CMD Register Command LFRM
	0x3002 0XXXX 0XXXX	Write CRC Check Register 32-bit CRC MSB Value 32-bit CRC LSB Value
	0x30A1 0x000D	Write CMD Register Command DESYNC
	0x2000 : 0x2000	NOP : NOP



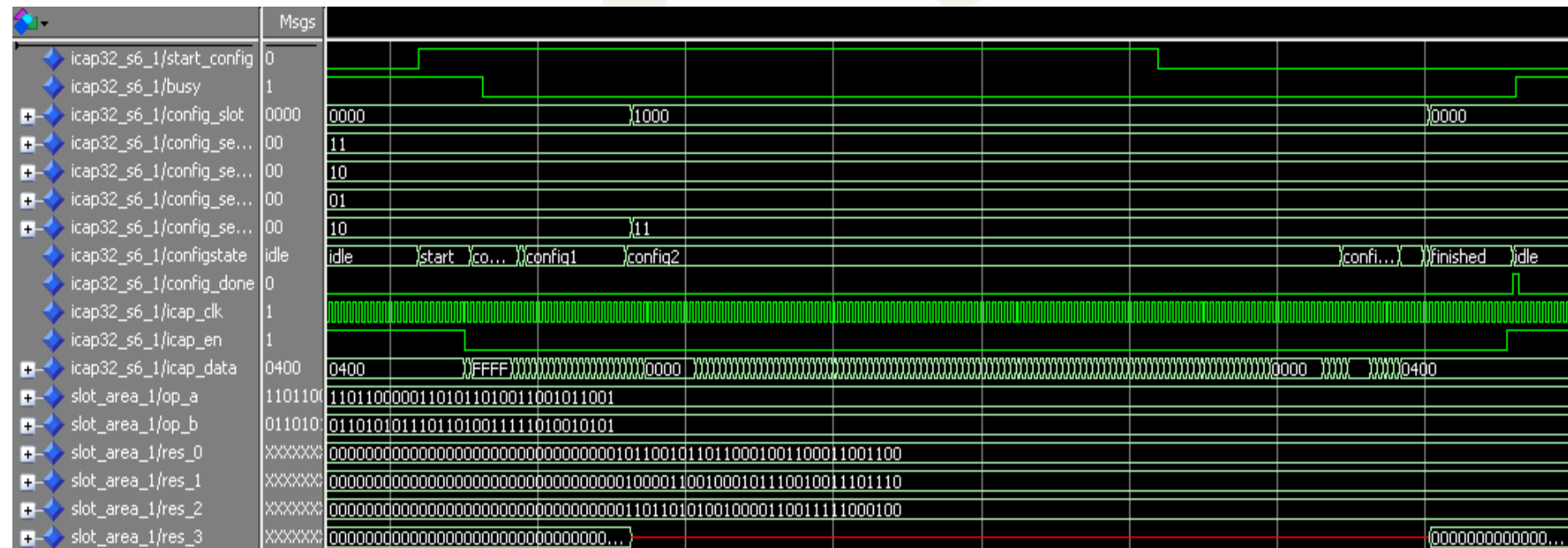
# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Case Study
  - CPU with Reconfigurable Instruction Set Extension



# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Simulation :



# Examples of Errors Found in Case Study

- Isolation being too late during reconfiguration and too early reconnection after reconfiguration (injected "X" from the reconfigurable region to the static part)
- Timing and proper reset of the newly incoming reconfigurable module.

# Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

## Summary:

- Simulation framework for functional modeling and verification of partial run-time reconfiguration in VHDL at the RTL
- Cycle-accurate modeling
- Uses real bitstreams
- Supports Island-based and Slot-based reconfiguration styles
- Supports module relocation