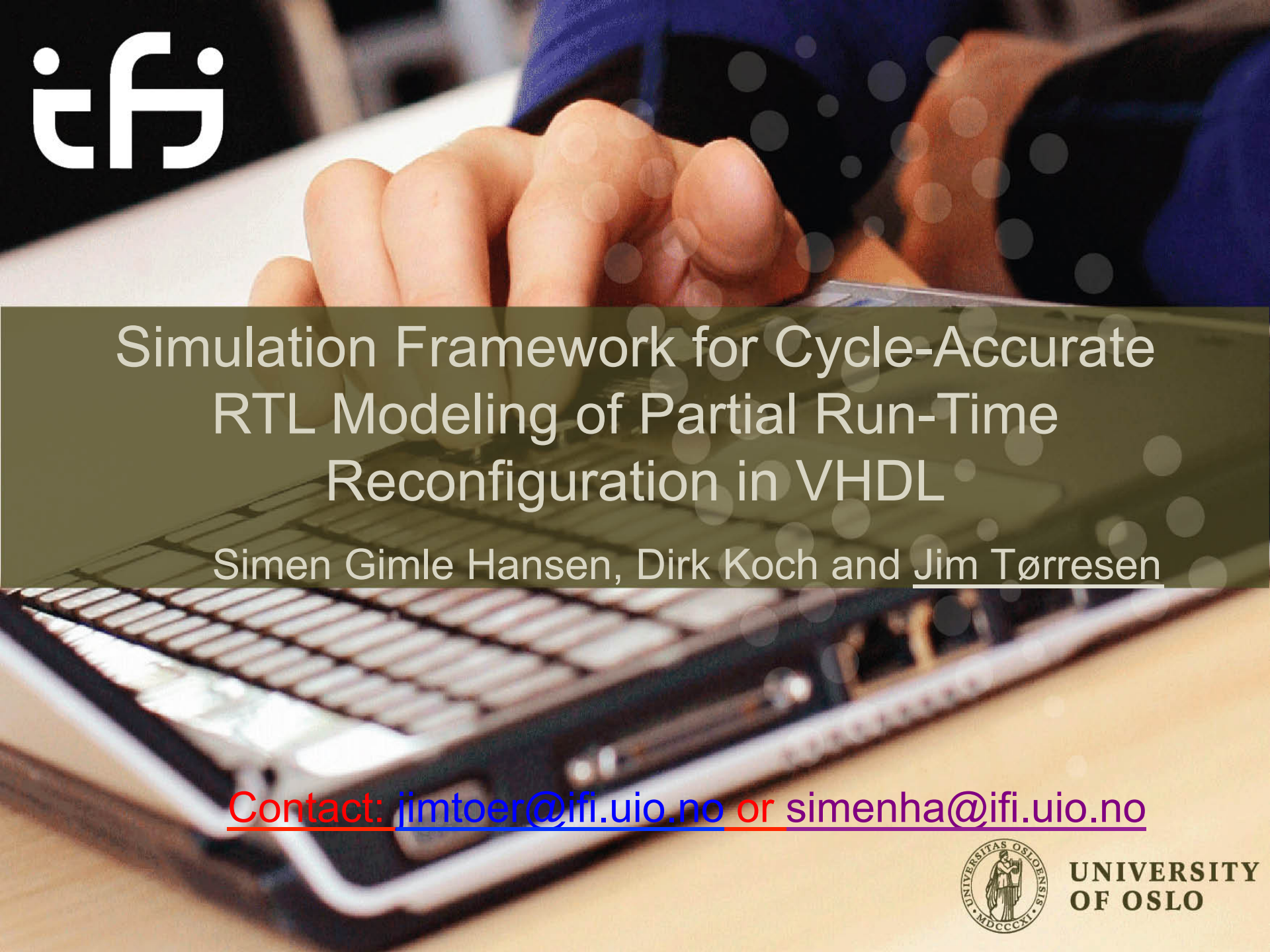

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

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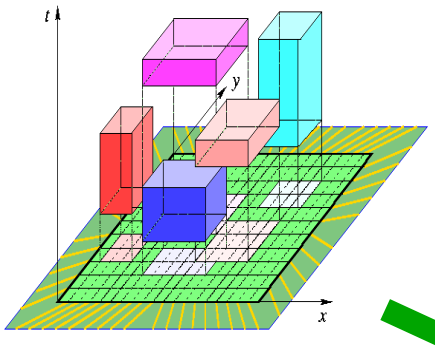
UNIVERSITY OF OSLO

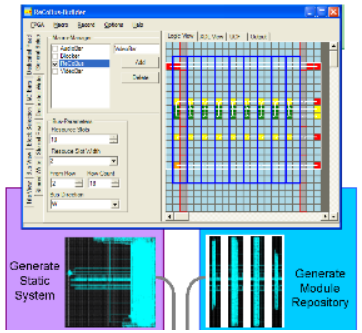
Context Switching Reconfigurable Hardware for Communication Systems (COSRECOS)



Methodologies
- Temporal module placement
- Analysis
- Partial reconfiguration

Documentation
- Tutorials
- Labs
- Design examples

Applications & reconfigurable systems



Tools
- Floorplanning & constraining
- Bitstream assembly
- System generation

OS4RC
- HW/SW interfaces & drivers
- Management
- Diagnosis

Context Switching Reconfigurable Hardware for Communication Systems (COSRECOS)

People PhD students Alexander Wold, Simen G. Hansen and Christian Beckoff
Postdoc Dirk Koch
Project manager Jim Torresen

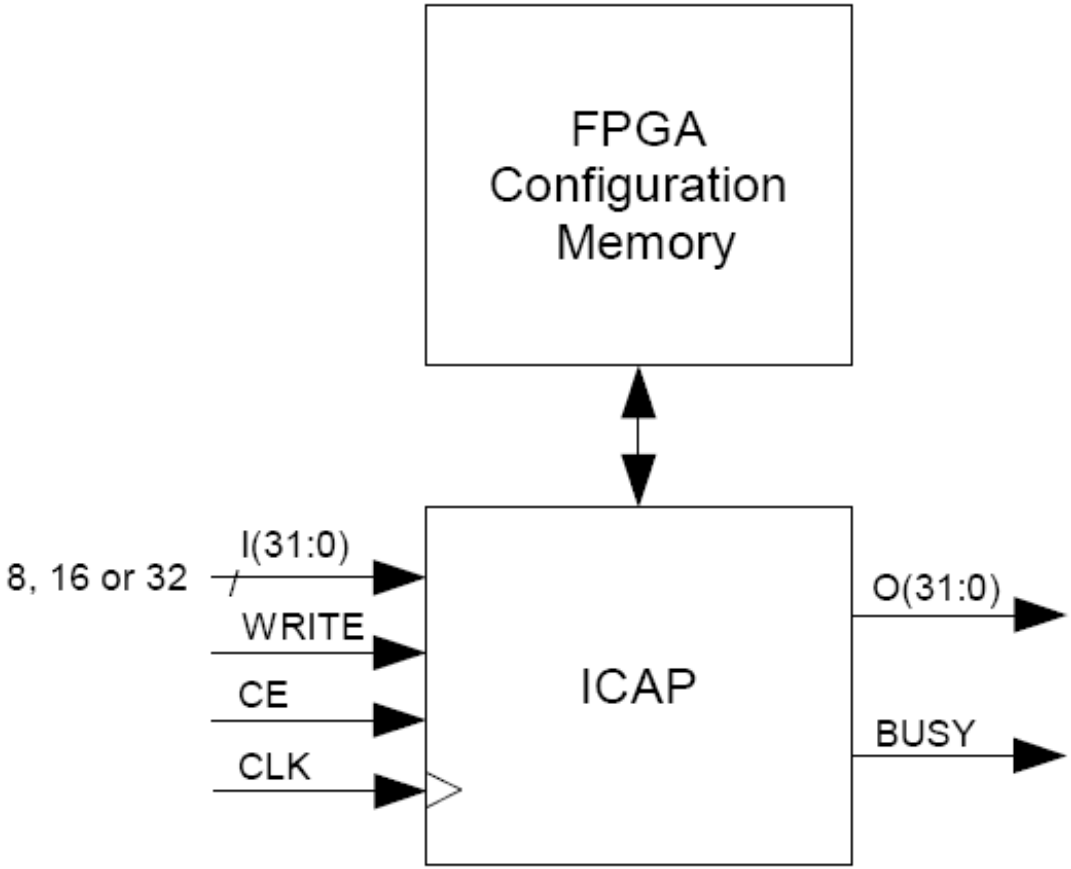
Website (Google for ``COSRECOS´´)
http://www.mn.uio.no/ifi/english/research/projects/cosrecos/

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Partial Run-Time Reconfiguration
  - Slow adaptation in industry
    - Lack of good design tools and design flows
    - No easy way to simulate
    - Simulation is important for product development
- This paper proposes:
  - A simulation framework for cycle-accurate functional modeling and verification of partial run-time reconfiguration at the Register Transfer Level (RTL) in VHDL

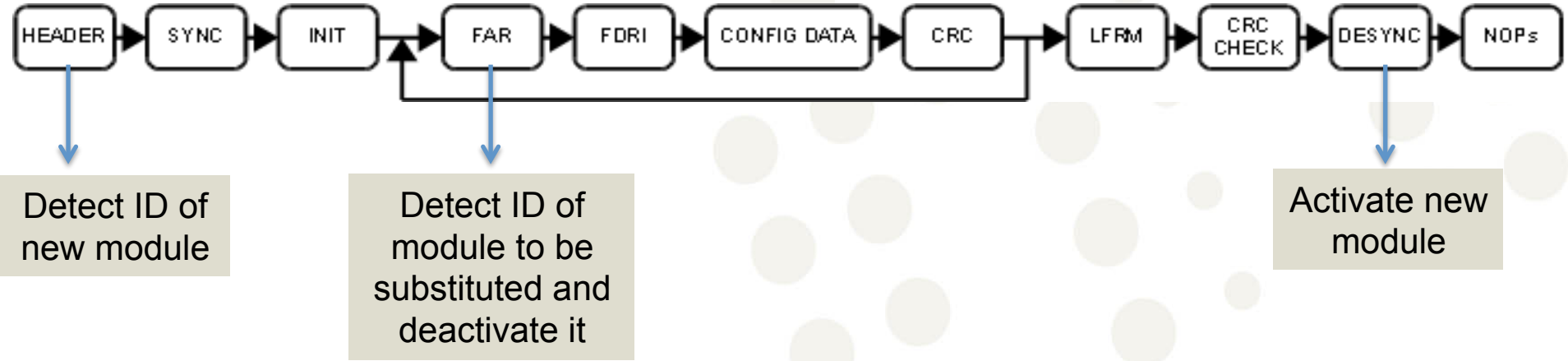
Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Xilinx ICAP (Internal Configuration Access Port) port :



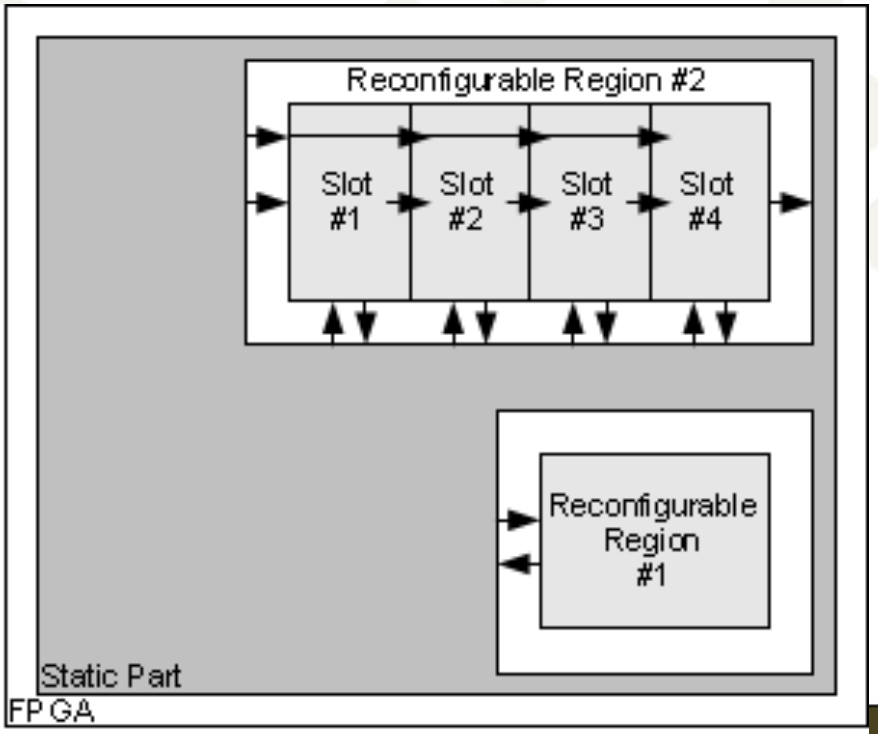
Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Xilinx bitstream format :



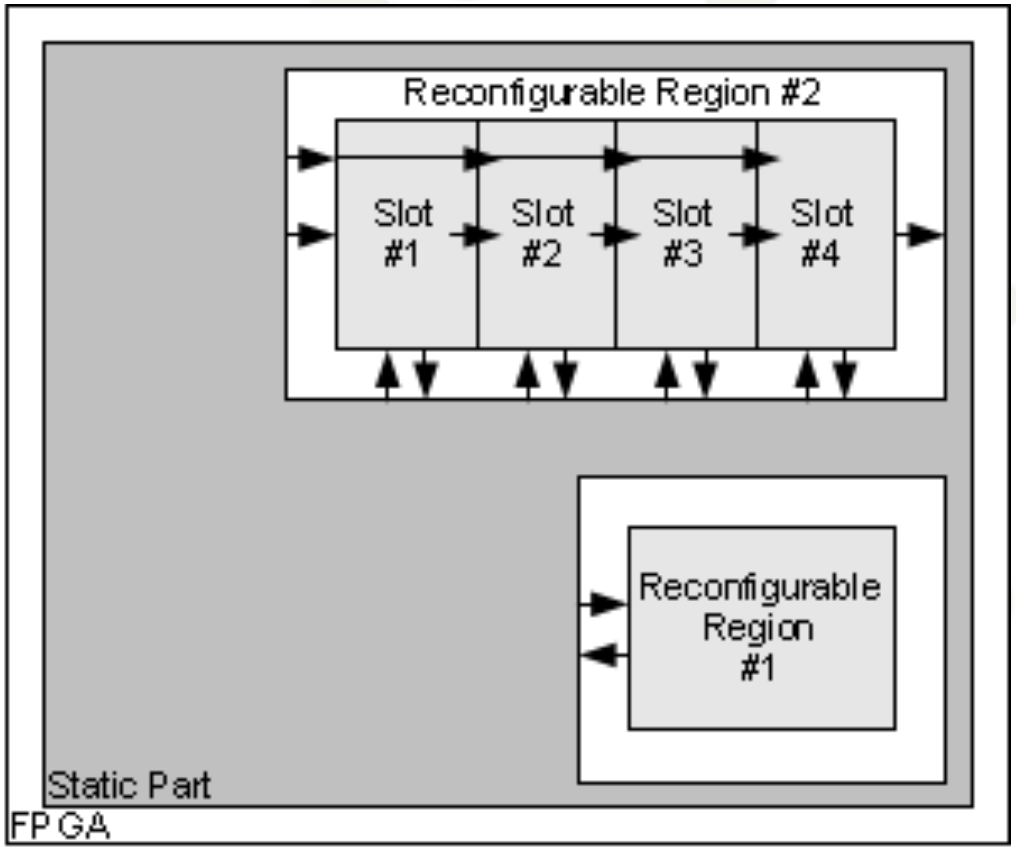
Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Simulation Framework Features:
  - Using real bitstreams
  - Support for Island-based and Slot-based partial reconfiguration styles:
  - Support for module relocation



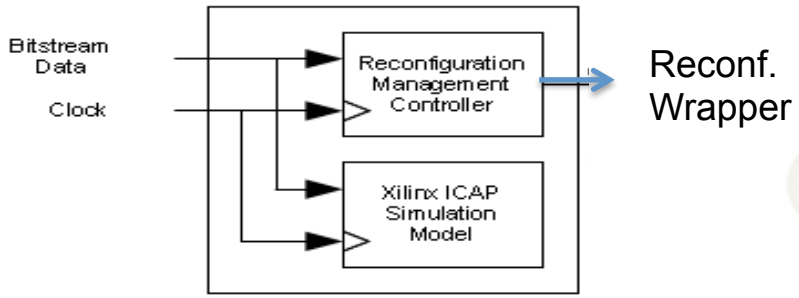
Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Partial reconfiguration styles :



Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

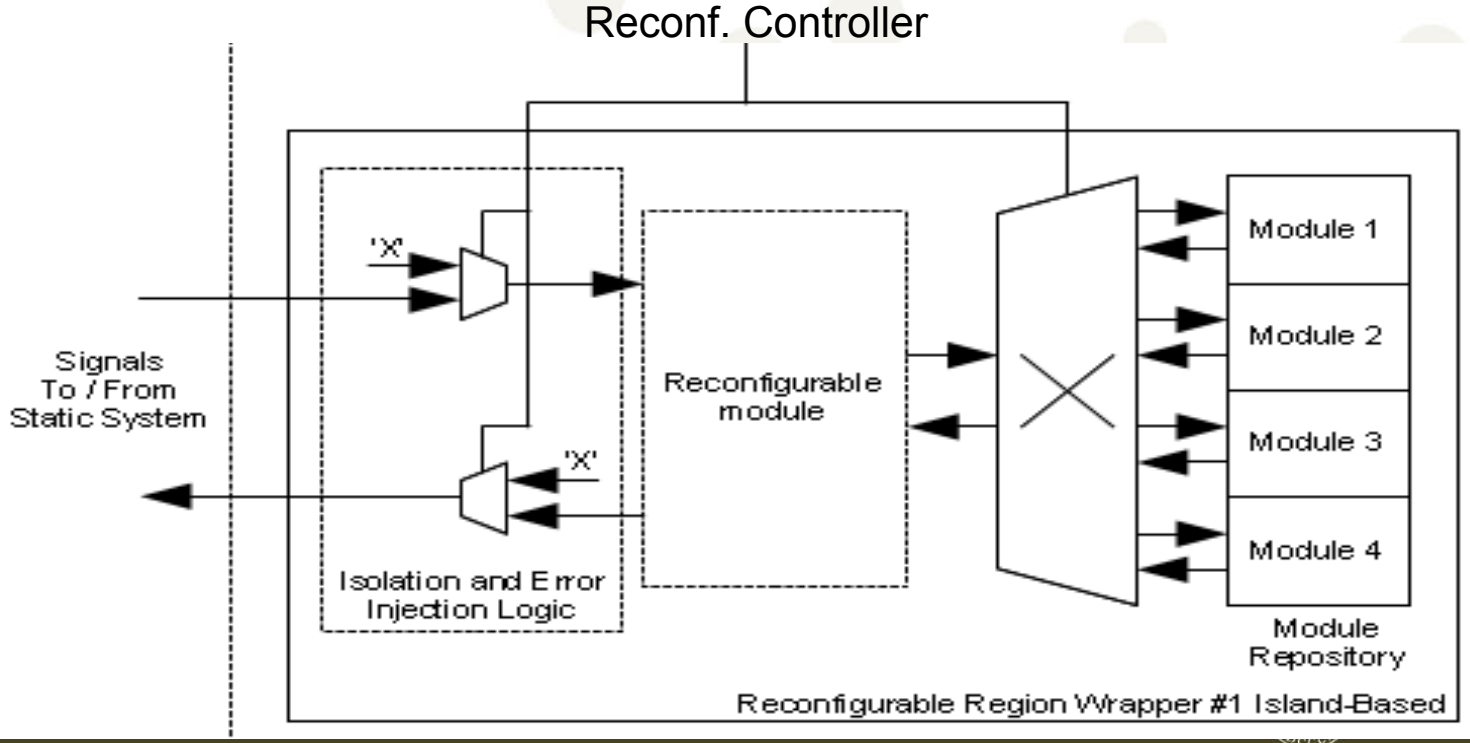
- Reconfiguration Controller
  - Parses and tracks the bitstream



  - Cycle-accurate based on extracted timing information (Xilinx Chipscope)
  - Keeps track of active and deactivated modules

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfigurable Region Wrapper
  - Module Repository
  - Crossbar Multiplexer
  - Isolation and Error Injection Logic



Collecting Reconfiguration Timing Data:

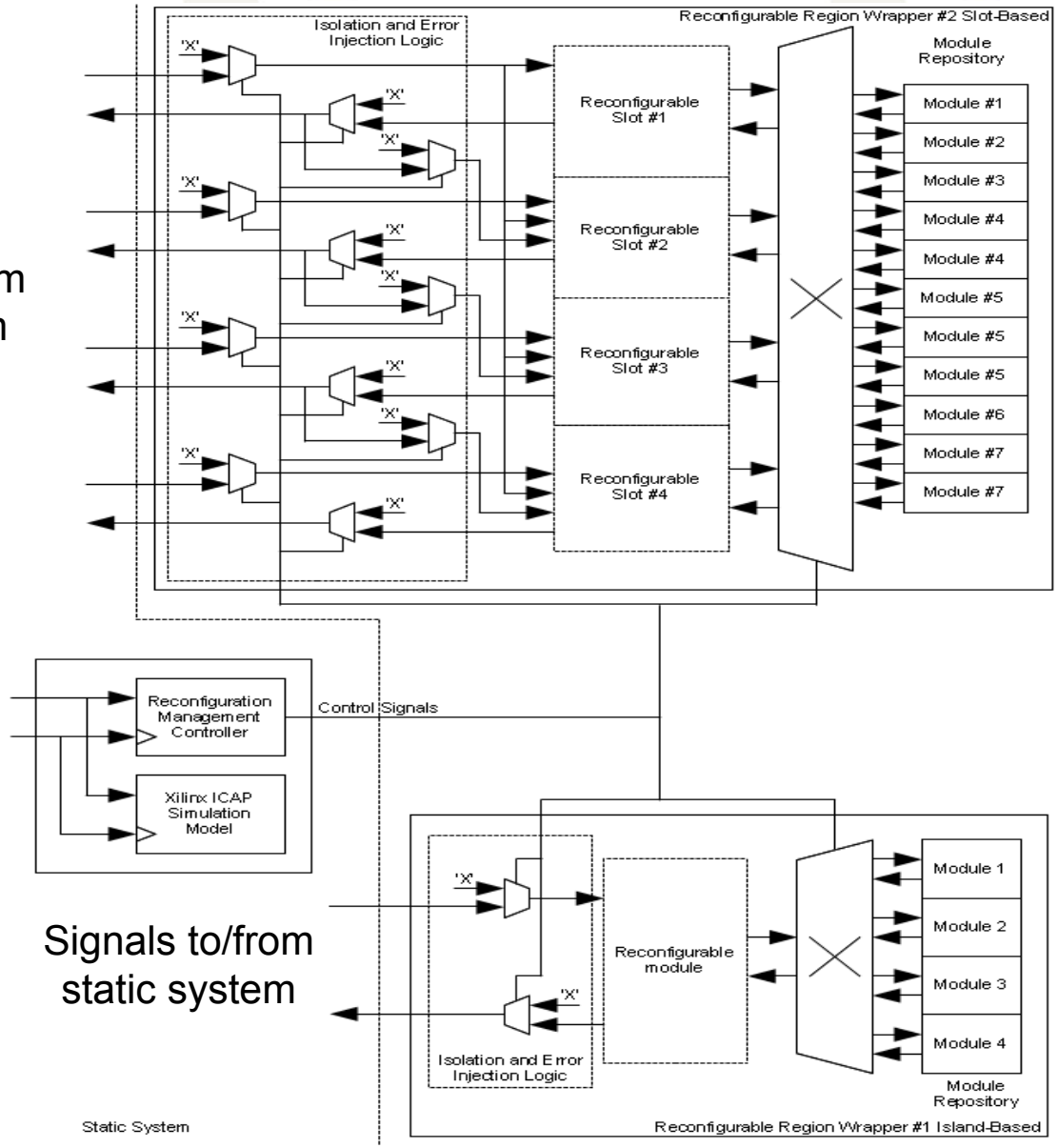
- Cycle-accurate RTL Modeling achieved by extracting actual timing data from physical device using Chipscope (Digilent Atlys Spartan-6 XC6SLX45)
- Different logic resource types investigated (CLBs, DSP48, BRAM)
- BRAMs found to have ”worst case timing” for deactivation and reactivation

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfiguration Controller
  - Controls the activation and deactivation of incoming and outgoing reconfigurable modules
  - Controls the Crossbar Multiplexer and Isolation and Error Injection Logic in the Reconfigurable Region wrapper
  - Supports :
    - Island-based and Slot-based reconfiguration styles
    - Multiple reconfiguration region
    - Module relocation

Signals to/from static system

Configuration bitstream



Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Reconfiguration sequence :

Bitstream Data	Description
0xNNFF	Module identifier NN
0xFFFF : 0xFFFF	Dummy word : Dummy word
0xAA99	SYNC MSB Word
0x5566	SYNC LSB Word
0xXXXX : 0xXXXX	Initialization commands
0x3022 0xXXXX 0xXXXX	Write FAR FAR MAJ Address FAR MIN Address

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

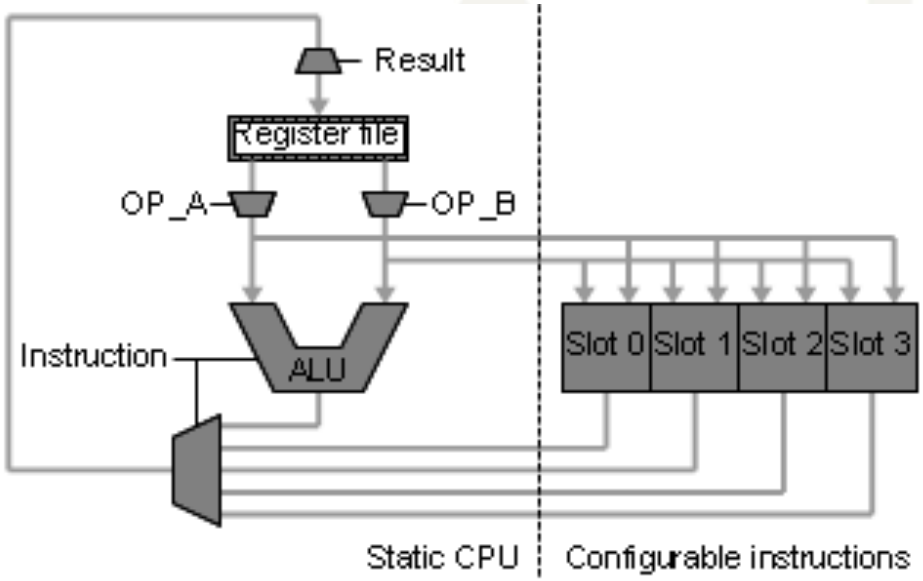
Bitstream Data	Description
0x30A1 0x0001	Write CMD Register Command WCFG
0x5060 0xXXXX 0xXXXX	Write FDRI FDRI MSB Value FDRI LSB
0xXXXX : 0xXXXX	First Configuartion Data : Last Configuartion Data
0xXXXX 0xXXXX	32-bit CRC MSB Value 32-bit CRC LSB Value

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

Bitstream Data		Description
if	0x3022	Write Next FAR Address
	0xXXXX	FAR MAJ Address
	0xXXXX	FAR MIN Address
		Loop back to Write FDRI
else	0x30A1	Write CMD Register
	0x0003	Command LFRM
	0x3002	Write CRC Check Register
	0xXXXX	32-bit CRC MSB Value
	0xXXXX	32-bit CRC LSB Value
	0x30A1	Write CMD Register
	0x000D	Command DESYNC
	0x2000	NOP
	:	:
	0x2000	NOP

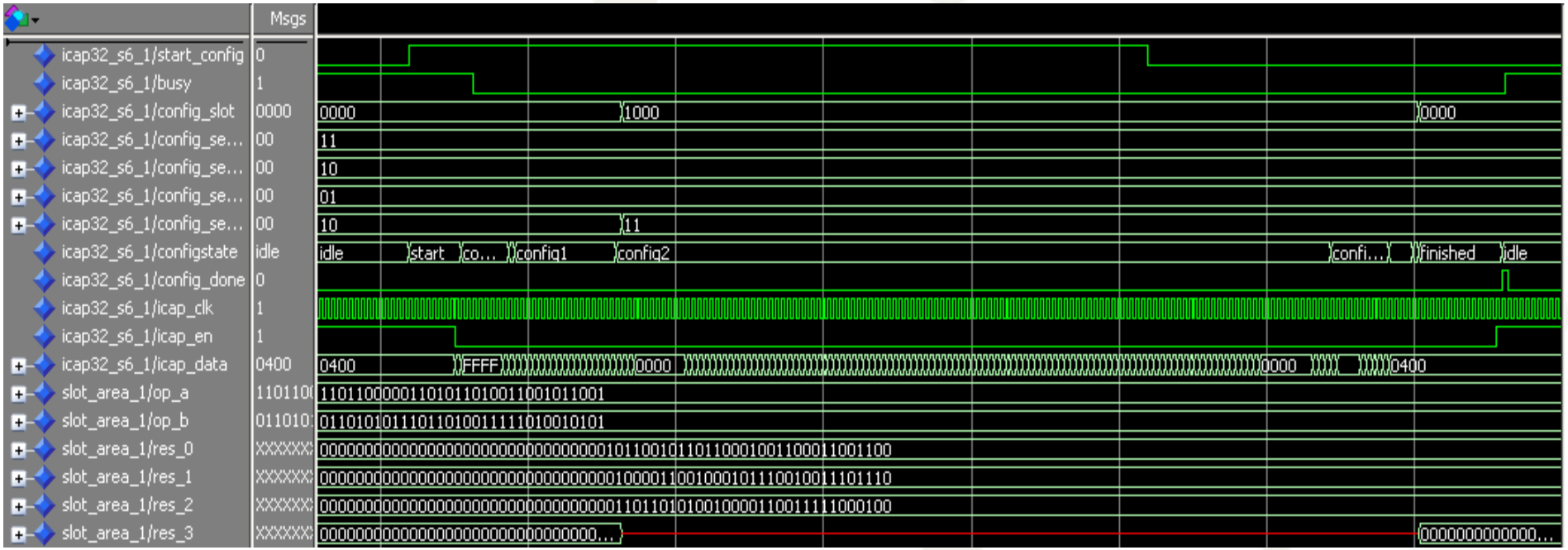
Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Case Study
  - CPU with Reconfigurable Instruction Set Extension



Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

- Simulation :



Examples of Errors Found in Case Study

- Isolation being too late during reconfiguration and too early reconnection after reconfiguration (injected ”X” from the reconfigurable region to the static part)

- Timing and proper reset of the newly incoming reconfigurable module.

Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL

Summary:

- Simulation framework for functional modeling and verification of partial run-time reconfiguration in VHDL at the RTL
- Cycle-accurate modeling
- Uses real bitstreams
- Supports Island-based and Slot-based reconfiguration styles
- Supports module relocation